MOTOROLA

1980

SWITCHMODE APPLICATION MANUAL

SWITCHMODE*
APPLICATION
MANUAL

After a brief introduction to the SWITCHMODE* power supply concept, the designer will find in this APPLICATION MANUAL the description of main active component characteristics in SMPS, and how to use them.

This manual also includes a collection of application notes and data sheets of the main semiconductor components that Motorola designed for switchmode applications and available from your nearest sales office or Motorola distributor.

We think this manual will be a valuable tool for designers.

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Printed in Switzerland — 1980

TABLE OF CONTENTS

INTRODUCTION TO THE SWITCHMODE POWER SUPPLY CONCEPT

A - GENERAL DESCRIPTION

To reduce the size, weight and power dissipation of LSI Equipment, particulary in microprocessor based units and TV, most designers are turning to switching power supplies. The resulting volume production, particulary of semiconductors, is reducing switcher prices so much that their advantages are now available to all users.

Another boost to switching supply development, especially dc/dc converters is coming from the relay to transistor change over in telephone switching. The advantages are considerable. Because these DC sources control their outputs with switching rather than linear transistors they can deliver 60% to 90% efficiencies. Because of their $\simeq$ 20 KHZ and higher switching rates, filters and transformers need only be a fraction of the size and weight required by linear supplies.

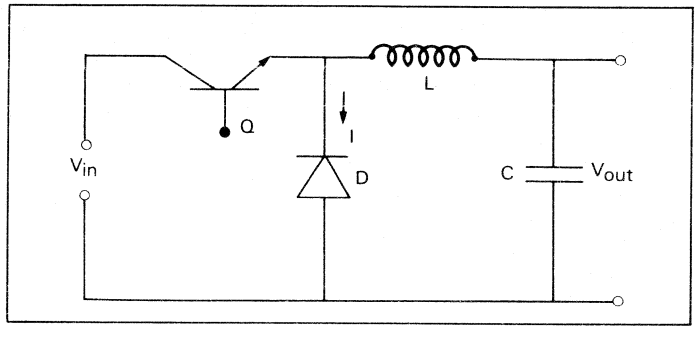
At powers levels above 100 to 200 watts, switching supplies are smaller and more efficient than their series regulated conterparts. However, they are also considerably more complex, requiring pulse-width-modulated drive signals for their switching power transistors, as well as special filter components and shielding.

B - PRINCIPLE OF OPERATION

THE SWITCHING REGULATOR THEORY

The principe of operation and the method by wich conversion at high efficiencies can be achiev using switching regulators can be demonstrated by analyzing the basic configuration of a switchi voltage regulator (fig. 1)

FIG 1



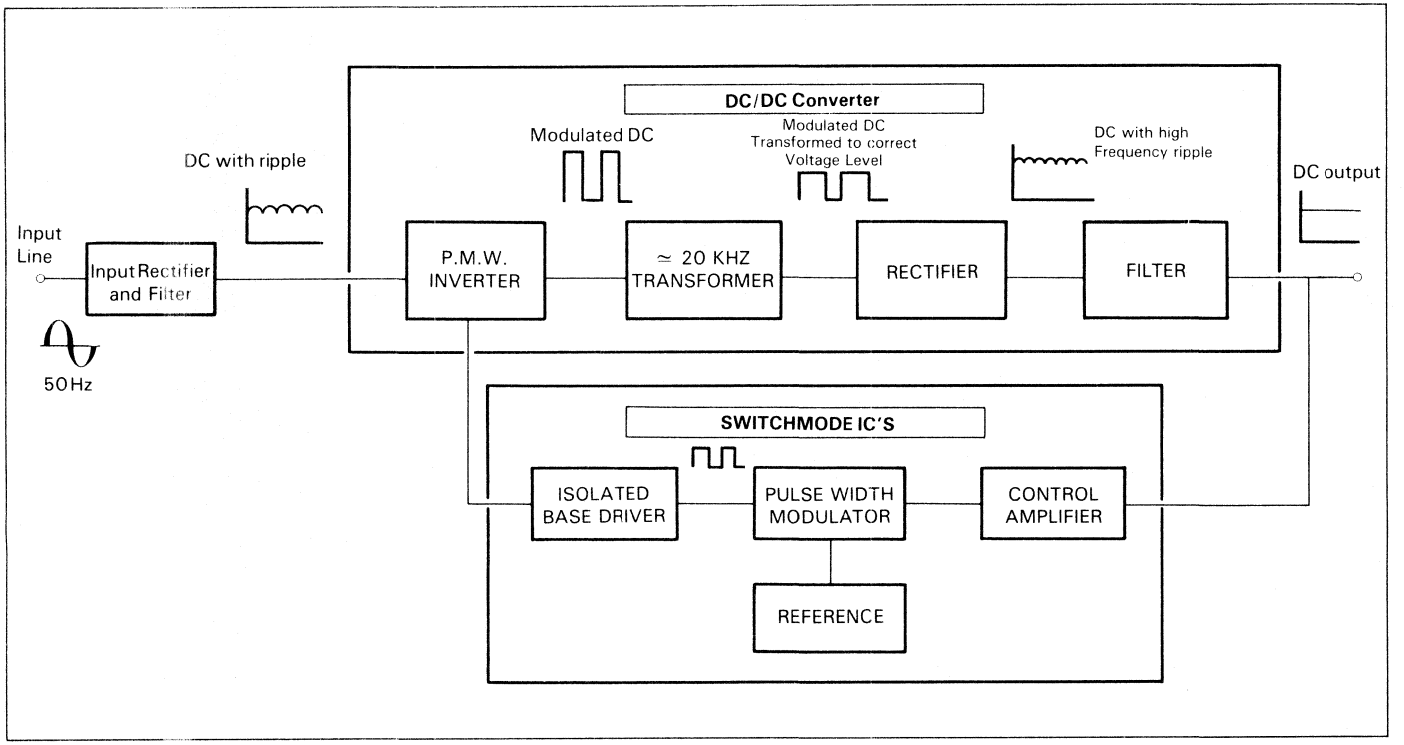
Q is the switch transistor which is turned on and off by the regulators control circuitry at a frequen and duty cycle required to maintain the desired output. Because this transistor is always in the satu ted state when it is conducting, or otherwise completely non-conducting the power dissipated in t switch is much lower than that dissipated in a series regulator, whose pass transistor is continou operated in the linear region. The diode (D) is the catch diode and provides a continuous current pa for the inductor (L) when the switch (Q) turns off. During the time that Q is turned on (ton) the inp of the LC filter causing the current (I) to increase; when Q is turned off the energy stored in the indu tor maintains the current flow to the load throug D. The LC filter will average the voltage seen at input and deliver that voltage to the output load.

$$Vout = Vin \frac{(ton)}{ton + toff} = Vin \frac{ton}{T}$$

Therefore, by controlling the duty cycle ton/T, changes in the input voltage can be compensated for. If Vin increases, the control circuit will cause a corresponding reduction in the duty cycle and thereby maintain a constant Vout.

THE SWITCHING SUPPLY BASICS

When operating from on AC input (off-line), a switching supply rectifies and filters the input AC into DC with an acceptable ripple. Transistor switches chop this DC voltage into a series of rectangular waves, which are transformed to the required voltage level by either an inductor or a transformer. Once voltage-adjusted, the rectangular wave is rectified and filtered into the final output. To ensure that the output is indeed at the required voltage level, a modulation-control circuit senses the output voltage and compares it to a reference. With the result of the comparison, a modulation control adjust the rectangular wave's ON to OFF ratio so that the output voltage stays within its prescribed limits. (See switching supply basic diagram.)



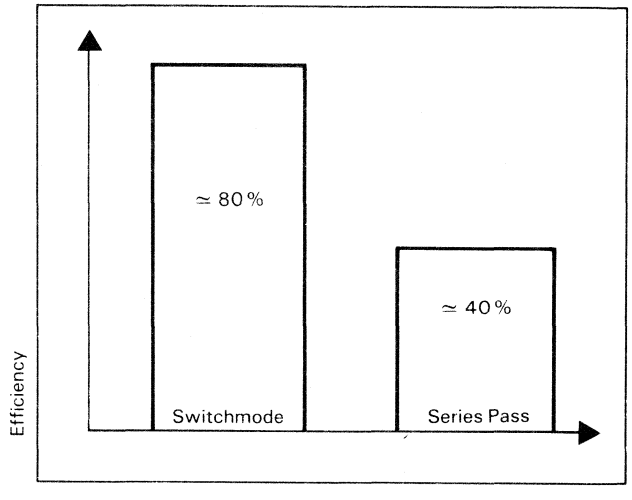
SWITCHING SUPPLY BASIC DIAGRAM

C - ADVANTAGES / DISADVANTAGES

ADVANTAGES

Efficiency

Power losses are much higher for the linear supply because of the continuous operation of the series pass regulating transistor in its active region. Consequently its power efficiency is relatively poor 10% to around 50%. In the switching supply, though, the regulating transistor is either saturated or cutoff. Power losses are held to a minimum, and power efficiency is very good, ranging anywhere from approximately 60% to better than 90%.



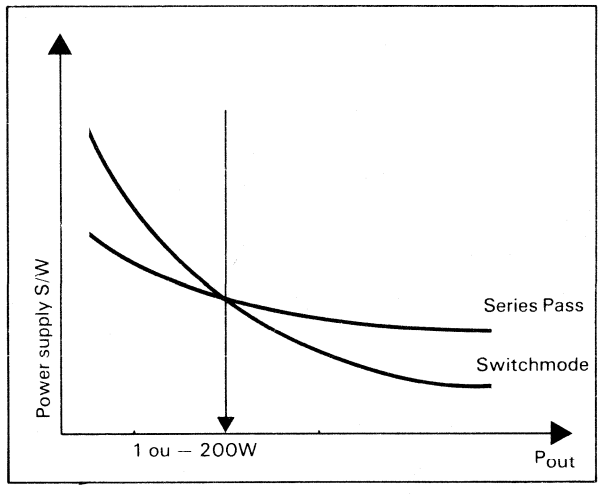
For P_{out} = 500 watts

— Series Pass consumption = 750 watts
— Switchmode consumption = 125 watts

= **625 watts Saved**

Cost

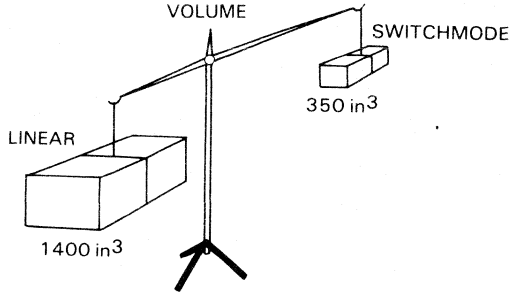
At the 100 w level, switching supplies cost more to build than series pass supplies, but at 200 w the figure is reversed. The parts cost covers only the electronic components and heat sinks. Because "switchmode" costs drop faster, they are more economical than series pass regulators at high power levels and cost about the same at the 200 w level. A couple of years ago, this break-even point was at the 500 w level.



1978 – 200 W
1980 – 100 W
1982 – 50 W

Volume / weight

Because of the use of a 50 HZ transformer for isolation between the line and load the serie pass system have a disadvantage of large size and weight. The switchmode regulators, however, operate above audio frequency and use small 20 KHZ power transformer. Because of the present emphasis or energy conservation efficiency, and small size the future appears bright for these switching supplies.



Feature	Series Pass	Switchmode
Size Weight	1400 in^3 10 kg	360 in^3 2 kg

Adjustable frequency

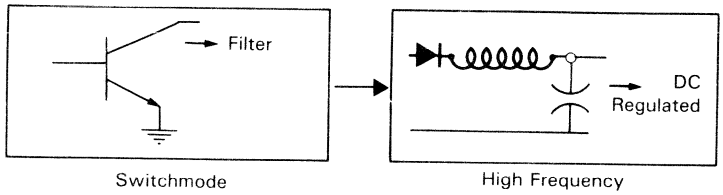
Switchmode allow to adjust the frequency from 1 to 300 KHZ (following the product choosen and customer application).

DISADVANTAGES

Noise

Because of its fairly high switching frequency 20 to 100 HKZ the switchmode version may be troubled not only by noise on its output but also by noise induced or conducted into the AC input lines.

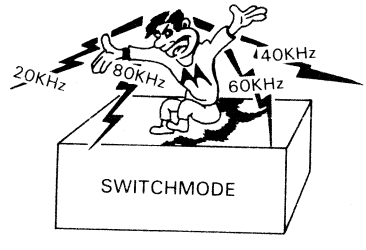
Typical ripple for a serie pass is around 5 mV instead of 20 to 60 mV for a switchmode Solution is a high frequency filter.

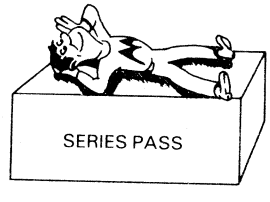


Switchmode

High Frequency
Filter and Rectifier

NOISE





Transient response

Briefly the transient response is the time required for the output voltage to return within its regulation limits when there is an aprupt change in either the line voltage or load current. For a serie pass this transient response is in a range of some micro-seconds instead of some milli-seconds for the switchmode due to high frequency power pulse. The trend for the next generation of switchmode is faster response with use of feed forward compensation circuits.

D - BASIC SWITCHMODE CONFIGURATIONS

BASIC

The material given in this section is intended to acquaint the designer with the basic switching transistor configurations used in P.W.M. Power supplies. Required rectifier, Transistors and control, Integrated linear circuits specifications for the most commonly utilized configurations are shown in the next pages. It should be noted that the products advised are idealized, in that the effects of leakage inductance voltage spikes, stray circuit capacitance snubber networks, clamp diode overshoots, diode reverse recovery and saturation voltages have been neglected.

The implementation of switching power supplies by the non-specialist is becoming increasingly easy due to the availability of Power devices and control IC'S especially developed for this purpose by the semiconductor manufacturer. Probably the simplest switching regulator is the **flyback converter** (also called a blocking oscillator or ringing choke). Using the least amount of magnetic and semiconductor devices, it is the cheapest. Another advantage is a wide range of output voltage. Flyback converters are widely used for up to a few hundred watts of output.

Power output is limited to several hundred watts because in flyback converters, inductor cores are driven in only one direction. **So Forward converters** are used for higher Power and lower voltage outputs more often than Flyback circuit.

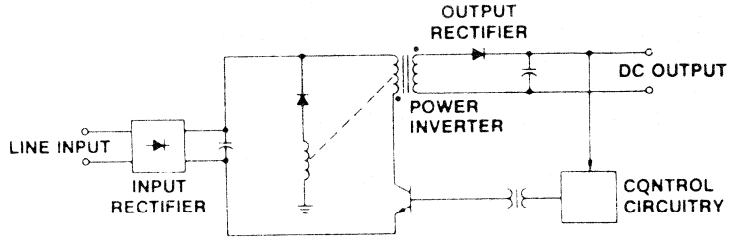
Push pull converter transformer can be operated in a single ended, half-wave bridge of full-wave — bridge mode. Single-ended half — wave bridge circuits use at least two transistor switches while a full bridge must have four (of course each transistor can be paralleled for more current capacity. All three versions use two flywheel diodes, and the usual voltage stress considerations apply to the bridge transistors).

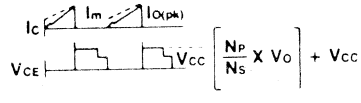
— push pull converters are sometimes subject to latchin and cross current condition. Latching means that the converter switches remain in one state, no matter what the driving circuit does.

BASIC FLYBACK CONFIGURATION

$P_O \doteq I_{C(OP)}\ V_{in}/6$

- NO FILTER INDUCTANCE
- LOW POWER MULTIPLE OUTPUT SYSTEMS
- REFERENCE EB-52

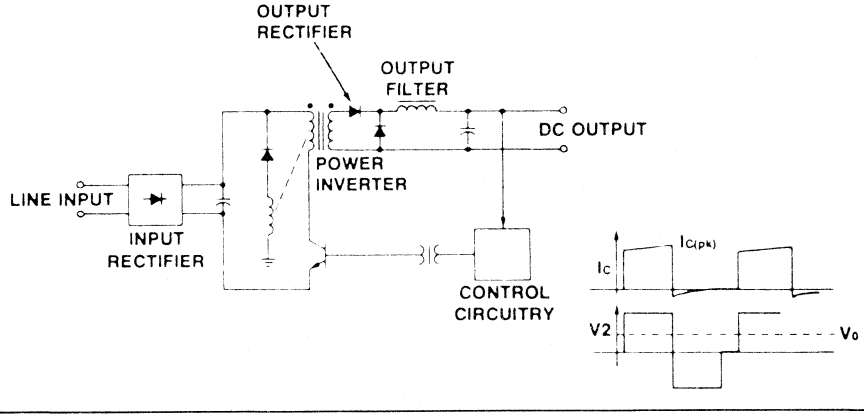




BASIC FORWARD CONVERTER

$P_O \doteq I_{C(OP)}\ V_{in}/3$

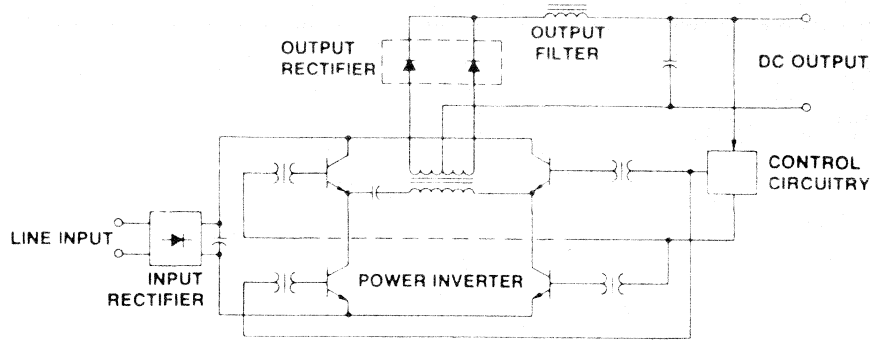
- HIGHER OUTPUT POWER THAN FLYBACK
- LOWER OUTPUT RIPPLE THAN FLYBACK



BASIC FULL-BRIDGE CONFIGURATION

$P_O = I_{C(OP)} V_{in}/1.5$

- SIMILAR TO HALF-BRIDGE
- HIGHER OUTPUT POWER



SWITCHMODE TRANSISTOR REQUIREMENTS

Vm = 220 VAC
OR 120 VAC WITH DOUBLER

Po = 250W
5V/50A

D.C. = 40% SINGLE TRANSISTOR
D.C. = 80% MULTIPLE TRANSISTORS

CIRCUIT TYPE	IC(OP)	VCEO(SUS)	VCEV	SYMMETRY CORRECTION NECESSARY?	ISOLATED?
FLYBACK	8A	400V	850V	NO	YES
FORWARD	4A	400V	850V	NO	YES
PUSH-PULL	2A	400V	850V	YES	YES
HALF-BRIDGE	4A	400V	450V	NO	YES
FULL-BRIDGE	2A	400V	450V	NO	YES
SERIES CHOPPER	2A	400V	450V	NO	NO

FLYBACK VERSUS FORWARD

FLYBACK

- INEFFICIENTLY USES TRANSISTOR'S CAPABILITY
- SIMPLE BASE DRIVE CIRCUITRY
- SUITED FOR LOW POWER APPLICATIONS
- SUITED TO VARIABLE FREQUENCY CONTROL

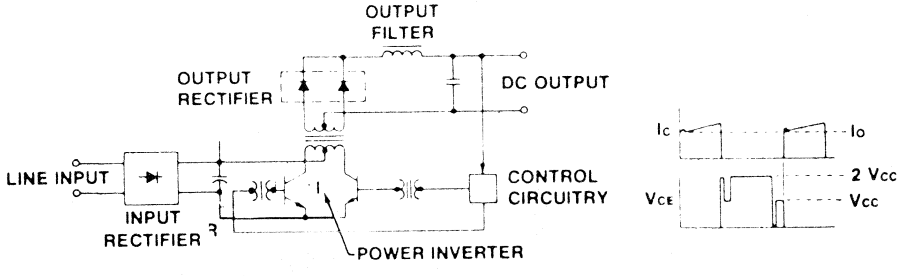
FORWARD

- EFFICIENTLY USES TRANSISTOR'S CAPABILITY
- MORE COMPLEX BASE DRIVE CIRCUITRY
- SUITED FOR HIGH POWER APPLICATIONS
- SUITED TO PWM CONTROL (DUTY CYCLE CONTROL)

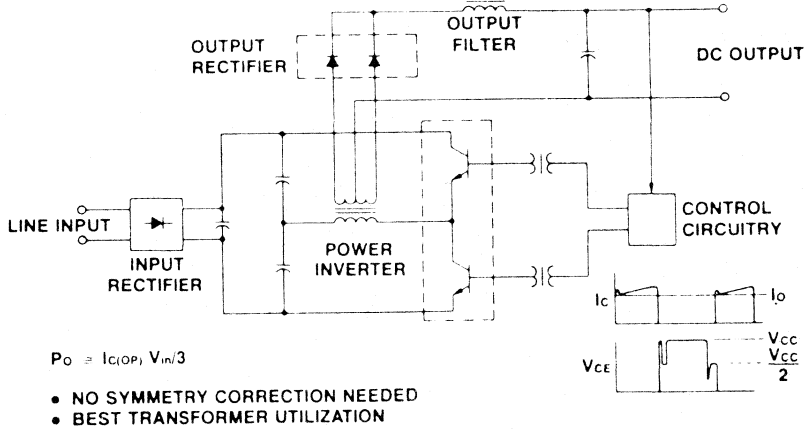
BASIC PUSH-PULL CONFIGURATION

$P_O \quad I_{C(OP)}\ V_{in}/1.5$

- BETTER TRANSFORMER UTILIZATION
- HIGHER FREQUENCY RIPPLE THAN FORWARD CONVERTER
- REFERENCE AN-737A



BASIC HALF-BRIDGE CONFIGURATION



$P_O = I_{C(OP)}\ V_{in}/3$

- NO SYMMETRY CORRECTION NEEDED
- BEST TRANSFORMER UTILIZATION
- HIGH FREQUENCY RIPPLE
- REFERENCE AN-767, EB-78

POWER SWITCHING TRANSISTORS

A - Switchmode Power Transistors-Principles

INDUCTIVE SWITCHING AT TEMPERATURE

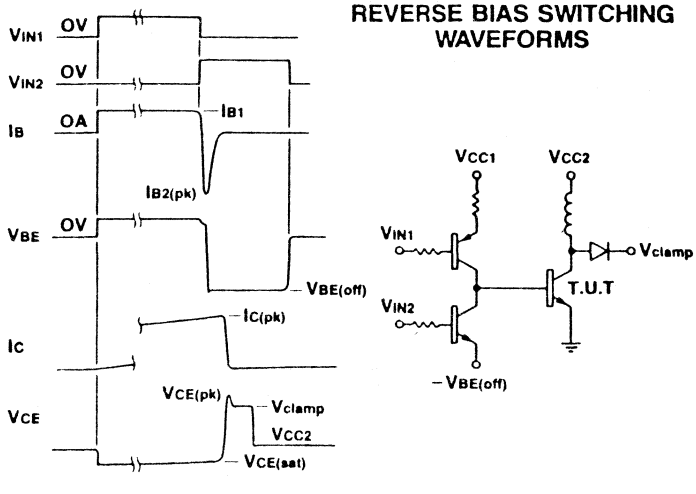
Resistive switching times and transition frequency are often used as a basis of comparison between products however these do not always relate to actual performance which will be achieved at elevated temperatures with inductive loads and changes in base drive. The reverse bias switching waveforms and inductive switching measurements illustrate the definitions now used by MOTOROLA.

SWITCHING TIME
RULES OF THUMB

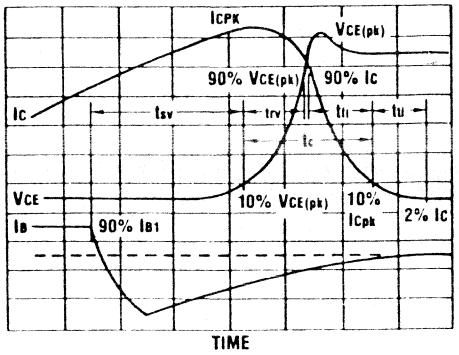
1. RESISTIVE $t_f \propto \frac{h_{FE\ (PK)}}{f_T}$
2. RESISTIVE $t_f \cong 1.5-2X$ INDUCTIVE t_f
3. RESISTIVE $t_s \cong$ INDUCTIVE t_s
4. CROSSOVER TIME (t_c) $\cong$ RESISTIVE t_f
5. OFF TIMES @ 100°C $\cong$ 1.5 – 3X OFF TIMES @ 25°C

IMPLICATION OF #5:

TRANSISTORS WHICH ARE MATCHED AT 25°C CAN BE AS MUCH AS 2:1 DIFFERENT FROM EACH OTHER @ 100°C



INDUCTIVE SWITCHING MEASUREMENTS



t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% $V_{CE(pk)}$
t_{rv} = Voltage Rise Time, 10 — 90% $V_{CE(pk)}$
t_{fi} = Current Fall Time, 90 — 10% I_C
t_{ti} = Current Tail, 10 — 2% I_C
t_c = Crossover Time, 10% $V_{CE(pk)}$ to 10% I_C

TURN-OFF CHARACTERISTICS UNDER REVERSE BIAS

"STORAGE TIME" (t_s OR t_{sv}) DECREASES WITH INCREASIN REVERSE BIAS VOLTAGE $V_{BE(off)}$ AND CURRENT $I_{B2(pk)}$. STORAGE TIME IS GENERALLY INDEPENDENT OF THE TYP OF LOAD, RESISTIVE OR INDUCTIVE, FOR A GIVEN COLLECTOR CURRENT.

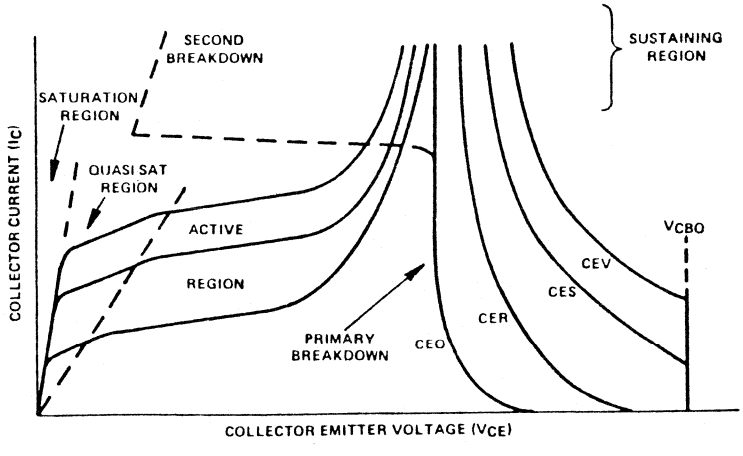
"FALL TIME" (t_f OR t_{fi}) DECREASES WITH INCREASING REVERSE BIAS VOLTAGE AND CURRENT UNTIL $I_{B2(pk)}$ APPROACHES $I_{C(pk)}$. INDUCTIVE FALL TIMES ARE SOMEWH FASTER THAN RESISTIVE TIMES FOR SIMILAR CONDITION

SAFE OPERATING AREA

Before considering SOA's the various definitions of the breakdown voltage terms used must be clear.

The typical collector-emitter characteristics illustrate these terms.

TYPICAL COLLECTOR-EMITTER CHARACTERISTICS



A detailed discussion will be found in EN-101.

TURN-ON SOA

During turn-on Vceo (SUS) is a fundamental limitation to the boundaries within which the Vce/Ic locus must fall.

In practice, to allow for component tolerances, potential product ageing and to achieve a low reject rate at final test and high field reliability, the equipment designer should keep well away from the limit lines on data-sheets.

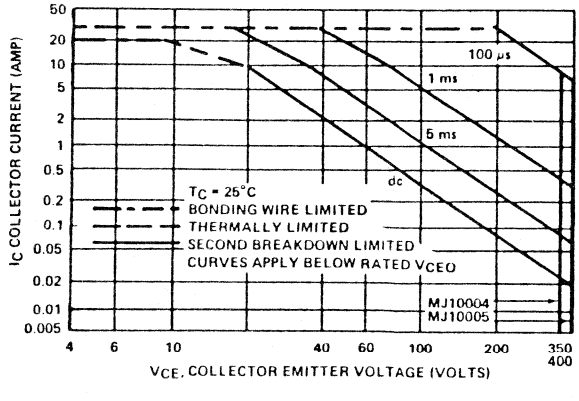
TURN-ON CONSTRAINTS

1. $V_{CEO(sus)}$ IS A FUNDAMENTAL LIMITATION

2. I_{B1} RISE TIME SHOULD BE LESS THAN Ic RISE TIME

3. ADEQUATE FORCED GAIN

FORWARD BIAS SAFE OPERATING AREA



TURN-OFF SOA (RBSOA)

RBSOA will be examined, operation in an avalanche E s/B condition is not recommended from a reliability point of view with high voltage products.

The turn-off switching times will depend on off drive levels and shapes, faster switching will change the type of stress in the RBSOA.

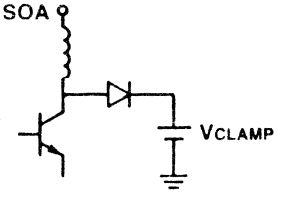
Among the RBSOA characteristics shown, it is not often appreciated that many reliability problems have been related to transient conditions during the equipment turn-on when all junctions are "cold" and drive, load and switching conditions can vary significantly from normal running.

Snubbing and/or active clamps should be used to control the shape of the turn-off load line.

For more details see AN-785 and AN-786 which are included in this book.

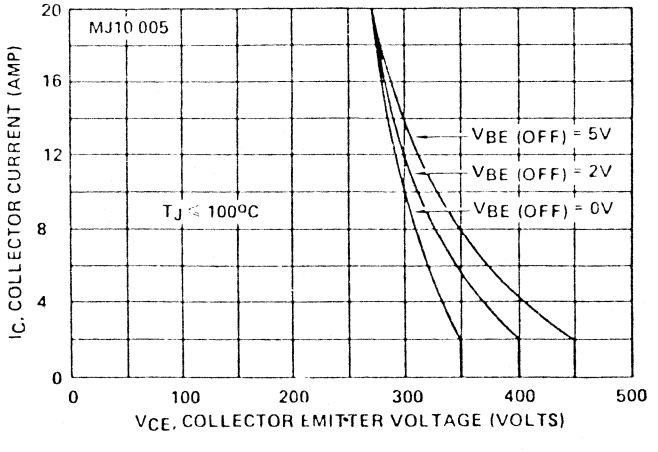
REVERSE BIAS OPERATION

1. COLLECTOR-BASE JUNCTION MAY BE AVALANCHED
2. USUALLY SPECIFIED WITH UNREALISTIC LEVELS OF OFF DRIVE
3. $E_{S/B}$ DECLINES AS OFF DRIVE INCREASES

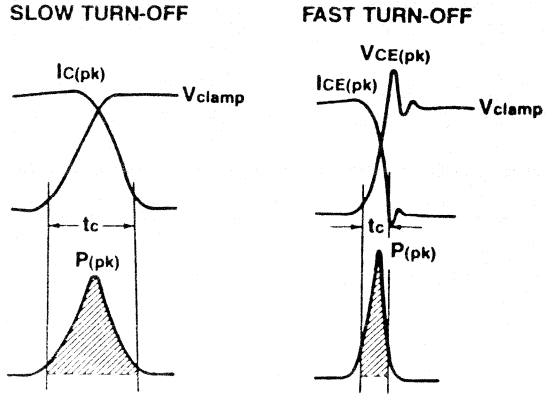


1. COLLECTOR-BASE JUNCTION IS NOT AVALANCHED
2. SPECIFIED WITH REALISTIC LEVELS OF OFF DRIVE
3. RBSOA INCREASES AS OFF DRIVE INCREASES

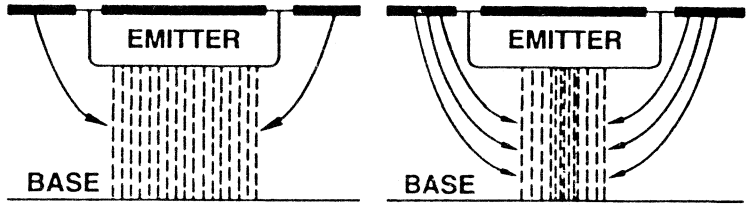
HIGH CURRENT DARLINGTON RBSOA



CLAMPED INDUCTIVE TURN-OFF ENERGY RELATIONSHIP



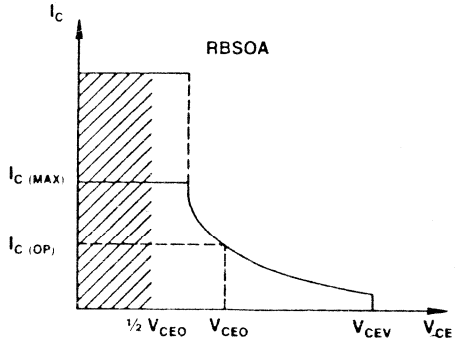
RBSOA CURRENT CROWDING



$V_{BE(OFF)}$ = OV

$V_{BE\ (OFF)}$ = 5V

SNUBBING



HIGH VOLTAGE TRANSISTORS HAVE SUBSTANTIAL CAPABILITY TO HANDLE CURRENT SPIKES AT VOLTAGES BELOW ≈ .75V_{CEO}

RBSOA CHARACTERISTICS

1. DECREASES WITH INCREASING IB1

   IMPLICATION: GREATEST STRESS CAN OCCUR AT LOW VALUES OF IC WITH FIXED IB

   SOLUTIONS:

   A. PROPORTIONAL BASE DRIVE
   B. BAKER CLAMP

2. GREATEST STRESS OCCURS AT PEAK VCE OVERSHOOT

   IMPLICATION: GREATEST STRESS CAN OCCUR AT OPERATING CONDITIONS WHICH MINIMIZE FALL TIME - NOT NECESSARILY FULL LOAD OR HIGH TEMPERATURE
   FASTER SWITCHING NEEDS MORE SNUBBING

3. THE RBSOA CURVE IS AN INSTANTANEOUS LIMITATION.

4. FUNDAMENTAL LIMITATION AT VCEV

   IMPLICATIONS:

   A. STRESS BEYOND VCEV WILL CAUSE DEVICE FAILURE
   B. RBSOA CAPABILITY EXISTS UP TO VCEV

5. RBSOA IS A COMPLEX FUNCTION OF OFF DRIVE

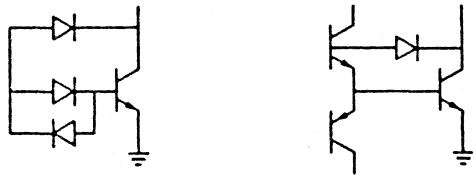
   IMPLICATION: TENDER AREAS MAY EXIST AT OFF DRIVE LEVELS SIGNIFICANTLY DIFFERENT FROM SPECIFIED CONDITIONS

BAKER CLAMP

This anti saturation circuit is of greatest benefit to simple transistor switches but in critical applications can also be used with advantage for darlingtons.

Care must be taken to specify diodes with suitable switching characteristics.

BAKER CLAMP

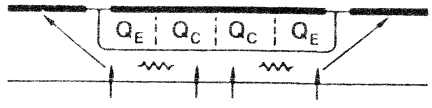


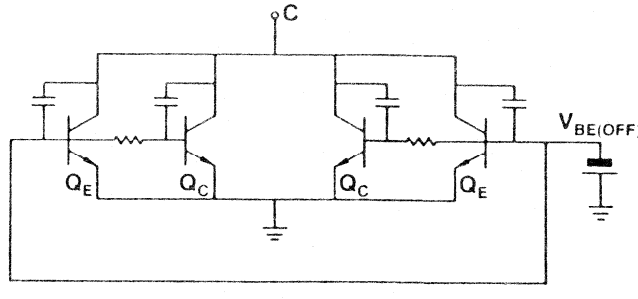
1. IMPROVES STORAGE TIME
2. IMPROVES CROSSOVER TIME
3. IMPROVES RBSOA
4. INCREASES STATIC BUT NOT DYNAMIC SAT VOLTAGE
5. IMPROVES PARALLEL PERFORMANCE

dv/dt

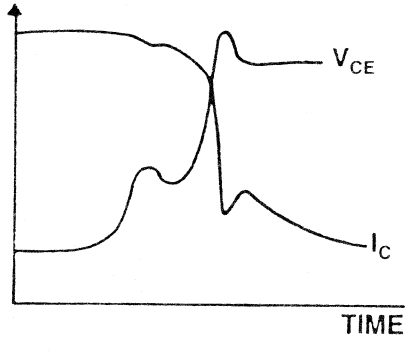
For both discrete transistors and darlingtons dv/dt induced "glitches" in the switching can be a source of a reliability hazard. The mechanism is explained in the model shown where the distributed Rbb and collector to base capacitance may cause a reinjection of base current during turn off of the total transistor and an excess dissipation in the part of the device which is turning on again.
For darlingtons especially in "totem pole" configuration circuits, the question of transients on the collector can be more critical because of the inherently higher current gain.

dV/dt MODEL





dV/dt LIMITATIONS



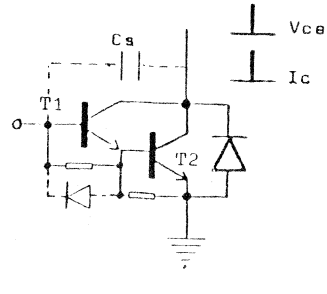
RELEVANT PARAMETERS

1. ON DRIVE
2. OFF DRIVE
3. COLLECTOR CURRENT

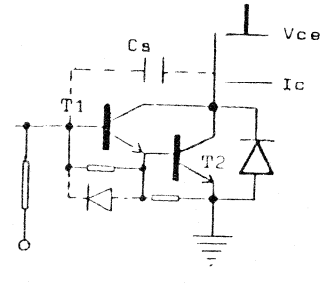
IMPLICATION OF #1:

A dV/dt LIMITED V_{CE} WAVEFORM CAN USUALLY BE CLEANED UP BY USING A BAKER CLAMP

Vbe off



NO Vbe OFF



Vbe OFF > -3V

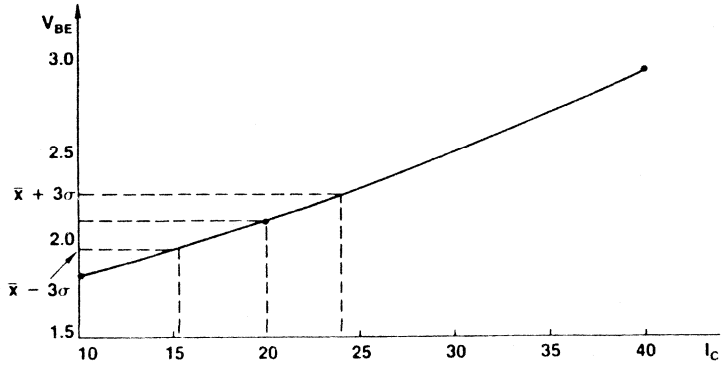
PARALLEL OPERATION

Darlingtons have been shown to be more easily paralleled than discretes.

It can be seen that for darlingtons in direct parallel (equal VBE) 95% of devices will be within a range of 15 to 24 Amps Ic (20 Amps nominal). Unequal switching times can be a problem as shown, emitter ballasting with a transformer can overcome this. Use of a base clamp or driver mounted in Darlington connection with the paralleled devices will reduce considerably the dispersion in switching times.

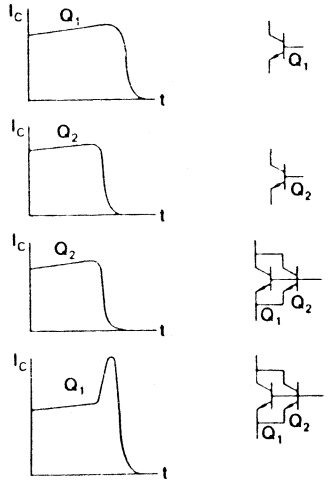
ON-STATE MATCHING

40A-400V DARLINGTON

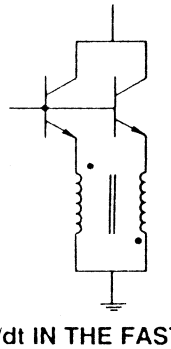


COLLECTOR CURRENT (AMPERES)

TURN-OFF WAVEFORMS



EMITTER BALLAST



NEGATIVE di/dt IN THE FASTER TRANSI
CAUSES ITS OFF BIAS TO BE REDUCEI
THE OFF BIAS OF THE SLOWER TRANS
TO BE INCREASED

EMITTER-BASE AVALANCHE

Evaluations so far have showed that for both discretes and darlingtons, a slight reduction (25%) of low current hfe occurs early in life thereafter no degredation has been observed on life tests switching inductive loads.

The effect of E.B. avalanche on switching will be seen later. (For details see AN-803 which is included in this book.)

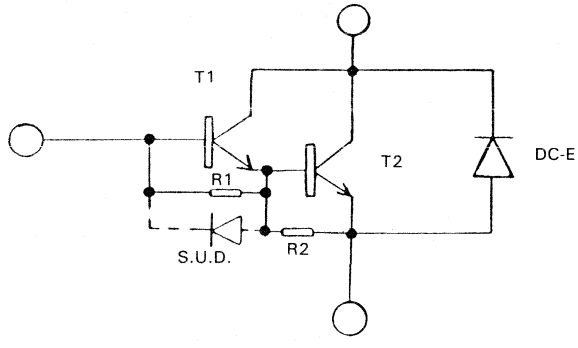
OBSERVATIONS OF EMITTER-BASE AVALANCHE

SWITCHMODE TRANSISTORS HAVE BEEN TAKEN INTO E-B AVALANCHE BREAKDOWN TO IMPROVE SWITCHING PERFORMANCE. LONG TERM LIFE TESTS TO DATE HAVE SHOWN NO MAJOR DEVICE DEGRADATION. SOME DECLINE OF LOW CURRENT h_{FE} HAS BEEN OBSERVED, BUT VERY LITTLE CHANGE AT OPERATING LEVELS.

B - Switchmode Darlingtons

APPLICATIONS

- MOTOR CONTROL
- SOLENOID DRIVER
- C.R.T. DEFLECTION
- SWITCHING REGULATORS
- STATIC INVERTERS
- ULTRASONIC GENERATORS
- AUTOMOTIVE IGNITION



Monolithic on the chip are the darlington connected transistors and temperature stabilising resistors to provide a minimum protection against thermal runaway. A collector emitter "freewheel" or "damper" diode is also monolithic on chip. In some products a diode is included across the base-emitter of T1 to allow a rapid extraction of the stored charge in T2 during turn-off, this diode is often a "hybrid" separate chip within the package though may, in some cases, be monolithic.

The range of products available covers a wide range of potential applications in cars, computers, T.V. sets and industrial power control. These devices are fabricated using epitaxial collector, double diffused or triple diffused technologies both with glass passivated mesas.

FEATURES

The darlington configuration features are shown, the result is a product which is less critical to overdrive and temperature variations (principaly because T2 cannot be overdriven) and which offer economies on a component and system basis which becomes more and more obvious, especially at higher currents.

A comparison of discrete and darlington devices shows clearly the darlington advantages. The higher Vce SAT is an often quoted as a disadvantage but as in many circuits a baker clamp (antisaturation diodes) may be used this difference becomes less apparent.

One parameter not often recognised is the DYNAMIC Vce SAT, this can be an important contributor to "on losses" especially in circuit configurations with a square wave type of current.

The dynamic saturation loss is caused by current crowding to the edge of the emitter fingers during turn on under the influence of the high collector-base electric field and forward bias base-emitter junction.

The lower peak gains of transistors used in the darlington also improve turn off switching times.

SWITCHMODE DARLINGTON FEATURES

I — TEMPERATURE STABIILITY IS EQUIVALENT TO DISCRETES

II — THE DARLINGTON CONFIGURATION ALLOWS LOWER PEAK GAIN IN THE INDIVIDUAL TRANSISTORS

III — LOWER PEAK GAIN IMPROVES DYNAMIC PERFORMANCE :

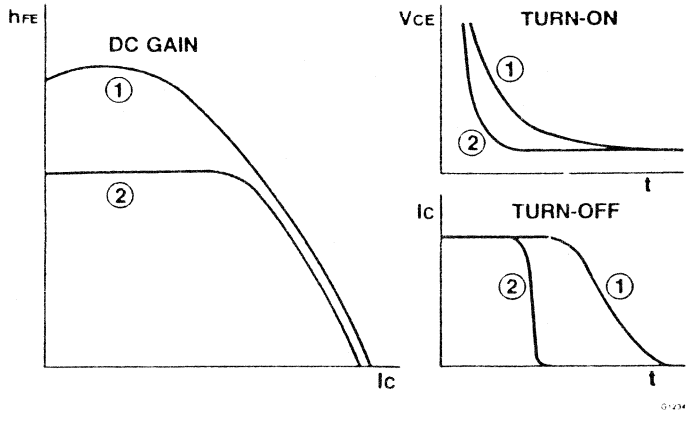
- A. FASTER OFF TIMES
- B. LOWER DYNAMIC SAT

IV — REQUIRE LESS SILICON FOR EQUIVALENT PERFORMANCE AT HIGH CURRENTS

V — AS A RULE OF THUMB HAVE :

- A. MORE SPEED AND GAIN
- B. HIGHER SATURATION.

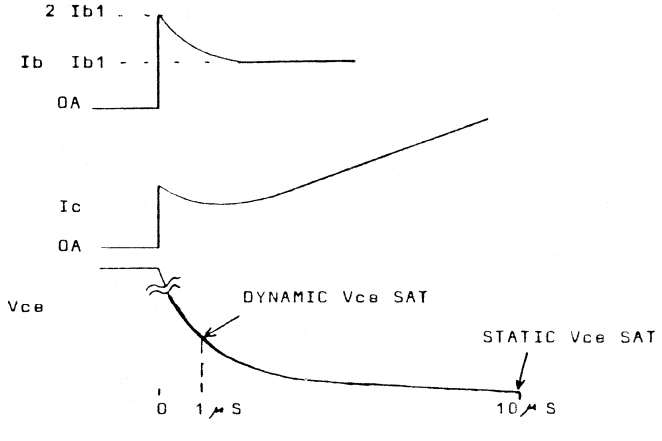
STATIC VS. DYNAMIC PERFORMANCE



DARLINGTON — DISCRETE COMPARISON

CHARACTERISTIC	MJ10009 500V/20A DARLINGTON	MJ13335 500V/20A DISCRETE
h_{FE} @ 10A/5V	50	9
V_{CE} (sat) @ 10A	1.4V	.8V
t_{sv} @ 100°C	1.5μsec	2.5μsec
t_c @ 100°C	.4μsec	.8μsec
DYNAMIC V_{CE} (sat) @ 1μsec	5V	10V
GUARANTEED RBSOA @ 10A	375V	400V
SILICON CONTENT	46k mils²	65k mils²

DYNAMIC SATURATION



COLLECTOR-EMITTER DIODE

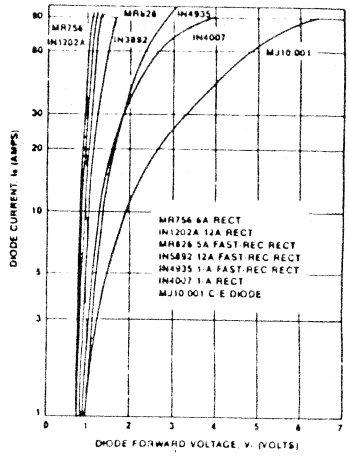
This diode can be very usefull in many circuits, it is capable of handling the same peak currents as the transistor but with relatively high forward voltages.

The characteristics are shown in the curves.

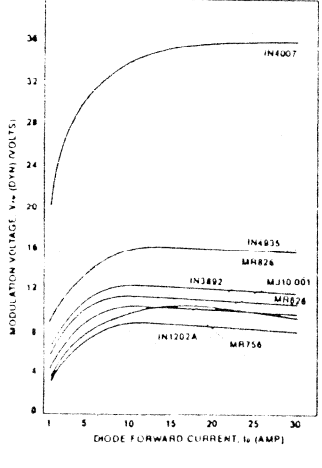
The devices are fast forward recovery but are relatively slow in reverse recovery compared with fast recovery rectifier diodes.

Note that fast recovery diodes are not often fast in forward recovery which is an important requirement in snubbing or clamp applications.

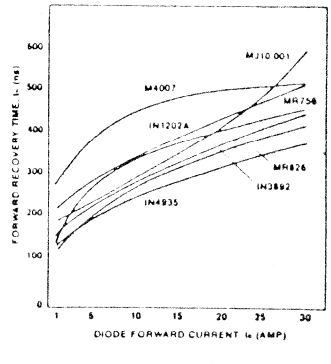
THE FORWARD-VOLTAGE CHARACTERISTICS OF C.E. DIODES COMPARED WITH C.E. DISCRETE DIODES THAT ARE OFTEN USED AS LOAD CLAMPS.



TETRONIX TYPE 576
CURVE TRACER.
176 HIGH-CURRENT FIX-
TURE 300μs PULSE.



FORWARD-SWITCHING MODULATION VOLTAGE (A) AND FORWARD-RECOVERY TIME (B) — THE TWO MOST IMPORTANT CHARACTERISTICS OF DIODES USED FOR SNUBBING — COMPARE VERY FAVORABLY WITH THE DISCRETE DIODES.



C - Drive Circuit Comparisons

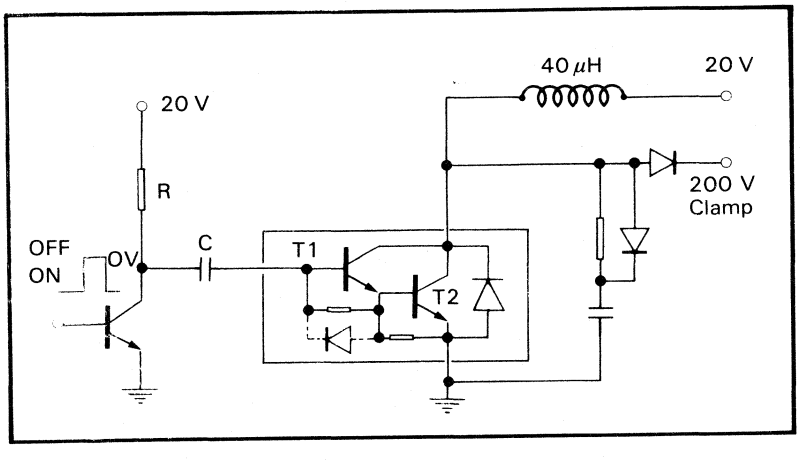
The drive circuits will be evaluated using the MJ10001 and BUT13 which are similar products except the BUT13 includes a speed-up diode. The principles of operation are also applicable to discrete transistors.

CIRCUIT 1

The simple drive circuit is capable of excellent results for fixed periods and P.R.F.'s such as C.R.T. deflection. Power is dissipated in the driver transistor during the OFF period.

The results show the product without speed up diode to be fastest due to rapid switch off of T1 with E.B. avalanche and extraction of T2 stored charge via this avalanched junction. The speed-up diode of the BUT13 limits VBE OFF of T1 to $< 1V$ slowing T1 and consequently T2 turn off.

Note the data sheet typical parameters are dramatically different for the MJ10001 due to the change in drive conditions.



FEATURES

I_{B1} OVERSHOOT
$V_{CE\ SAT}$ UNCONTROLLED
NO V_{BE} OFF
R.C $\gg T_{ON}$

RESULTS (NS)

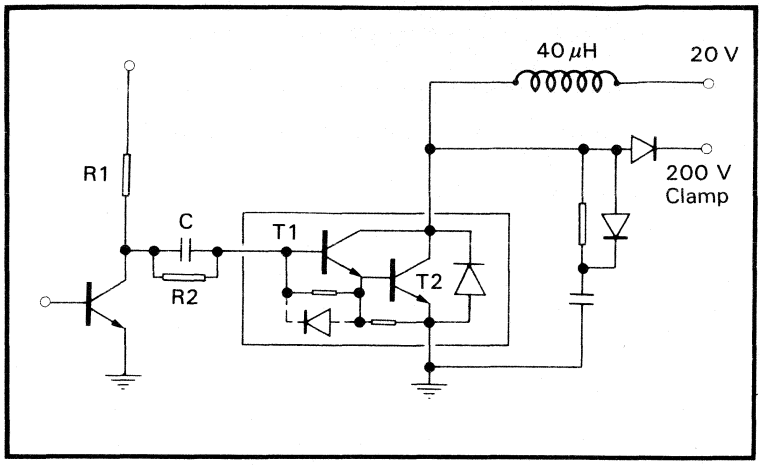
	T_{SV}	T_{FI}
MJ10001	400	40
DATA SHEET TYP.	1500	1100
BUT 13	600	100
(S.U.D.)		
DATA SHEET TYP.	600	150

The relatively low clamp voltage was used to avoid damaging devices while experimenting with these circuits.

In practice the snubber circuit and clamp, if any, should be optimised depending on the load-lines achieved.

CIRCUIT 2

This variation of circuit 1 includes R2 which smooths the IB2 waveforms. This results for the values used in an equal performance for the two products, the BUT 13 Tf being considerably improved due to the IB2 in T2 being reduced, compared with circuit 1, to an optimum value.



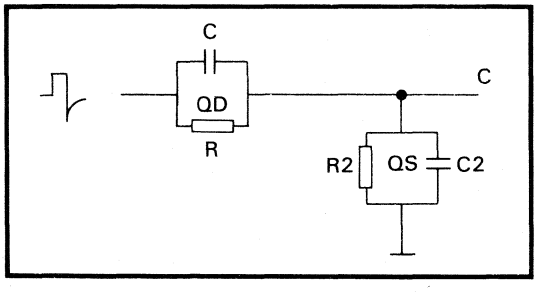
FEATURES

I_{B1} OVERSHOOT
$V_{CE\ SAT}$ UNCONTROLLED
NO V_{BE} OFF
R.C. ≫ T_{ON}

RESULTS (NS)

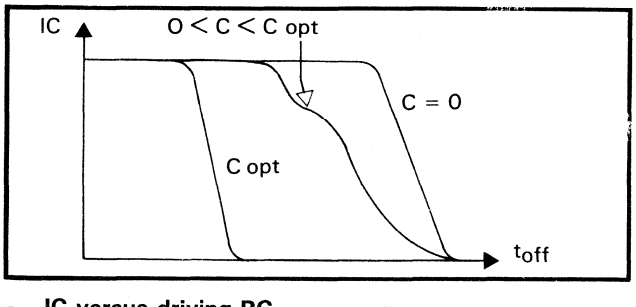
	T_{SV}	T_{FI}
MJ10001	600	40
BUT 13 (S.U.D.)	600	30

IMPORTANT REMARK FOR RC CIRCUIT



— **Symbolic representation for driving circuit and Darlington.**

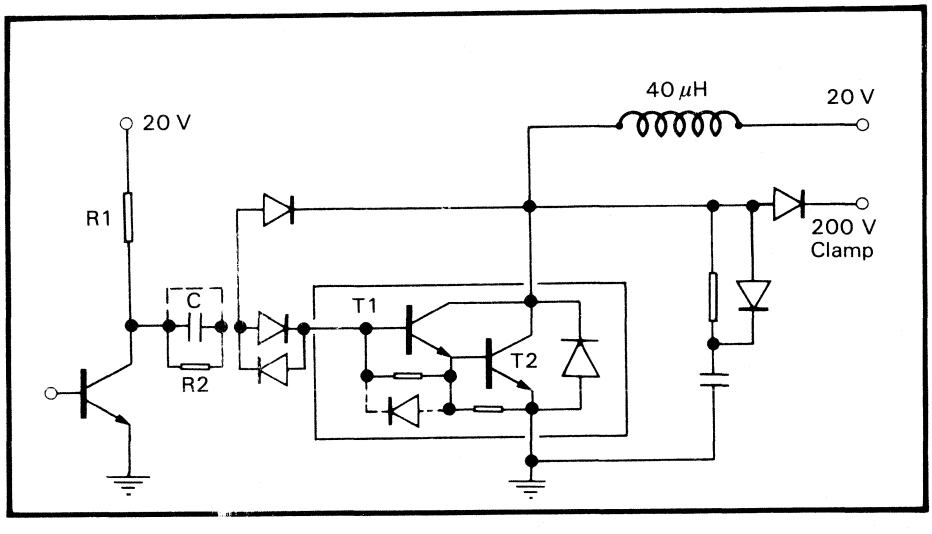
When we cut off the Darlington, the storage charge QS must be removed by the external circuit QD. If QD is less than QS, we obtain the curve shape as shown below. We must always check if QD > QS. For high voltage power Darlingtons R2.C2 ≃ 10 to 15 micro seconds.



— **IC versus driving RC**

CIRCUIT 3

This is equivalent to circuit 2 but with a baker clamp added. Looking at the results, we see again equal performance for the two products and that the addition of the antisaturation diodes reduces Ts by 30%. We can also see the effect of removing the C, R2 network on the BUT13, in the same circuit the MJ10001 would be very much slower due to the lack of turn off drive.



FEATURES

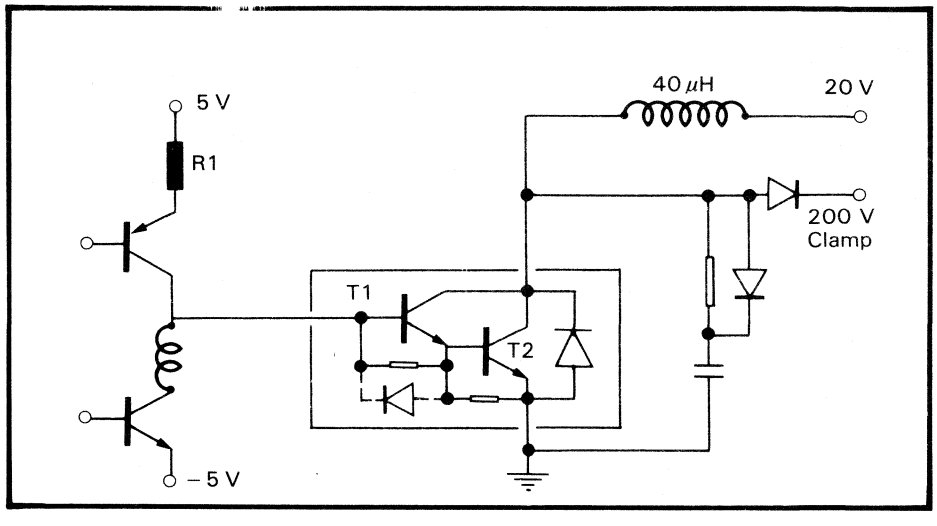
I_{B1} OVERSHOOT (WITH C)
$V_{CE\ SAT}$ CONTROLLED
NO V_{BE} OFF

RESULTS (NS)

	T_{SV}	T_{FI}
MJ10001	400	50
BUT 13	400	50
(S.U.D.)		
BUT 13 WITHOUT R2/C	700	100

CIRCUIT 4

This circuit is similar to that used for data sheet characterisation, a small inductor has been added in the IB2 path to improve Tf. The results show that, due to the lack of avalanche in E-B of T1 for the MJ10001, the Ts and Tf are high caused by the slow extraction of stored charge in T2. The BUT13 shows a clear advantage thanks to the speed-up diode.



FEATURES

NO I_{B1} OVERSHOOT
$V_{CE\ SAT}$ UNCONTROLLED
$\frac{dI_{B2}}{dT}$ CONTROLLED
V_{BE} OFF

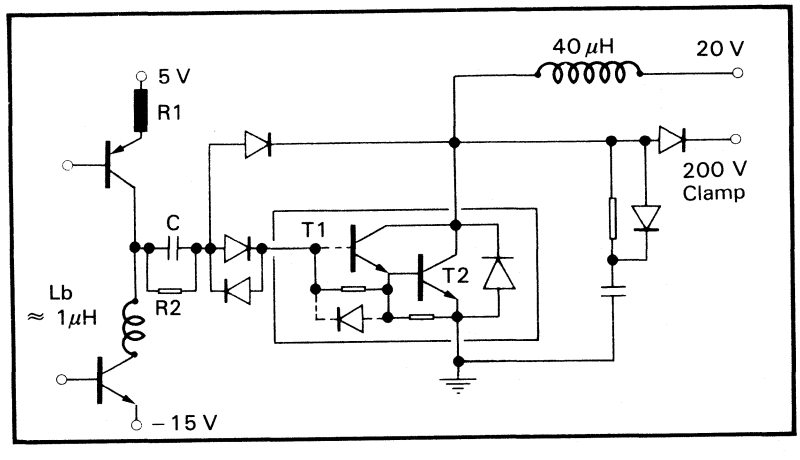
RESULTS (NS)

	T_{SV}	T_{FI}
MJ10001	3000	750
BUT 13 (S.U.D.)	1200	70

CIRCUIT 5

This type of circuit offers all possible features. The off drive supply is increased to −15 V. The results are similar to circuit 1 however circuit 5 may be used with widely varying periods and P.R.F.'s. R2 should be maintained greater than 5π to avoid drawing excess continuous current through the monolithic base emitter resistors during the off period.

The components may be optimised for Ts or Tf and the results are excellent.



FEATURES

I_{B1} OVERSHOOT

$\frac{dI_{B2}}{dT}$ CONTROLLED

$V_{CE\ SAT}$ CONTROLLED

V_{BE} OFF

RESULTS (NS)

	T_{SV}	T_{FI}
MJ10001 (OPTIMUM TF)	400	60
BUT 13	580	50
MJ10001 (OPTIMUM TS)	200	120
BUT 13	400	100

CONCLUSION

Hopefully these comparisons of circuits will give you a starting point to design depending on the performance/cost objectives in your application.

Due to economic and performance advantages, switchmode darlingtons are now proven to be the best solution for power control in many applications. The recent introduction of products suitable for use on three phase main supplies and forthcoming introduction of some products in the SOT93 (TO-218, TO-3P) package to reduce mounting costs and facilitate paralleling for higher current controls will ensure a continuing rapid growth of applications for switchmode darlingtons.

D - SWITCHMODE power transistor application selector guide for line-operated SWITCHMODE power supplies

(20 to 50 kHz, 40 to 4000 watts)

INTRODUCTION

This guide offers the power supply design engineer an easy way to identify those Motorola SWITCHMODE Transistors most ideally-suited for his particular application. To use the five tables in this guide, the designer must first:

1. Determine which of five circuits he will be using (i.e., full-bridge, half-bridge, push-pull, forward or flyback).
2. Determine which of three line voltages he will be using (i.e., 120, 220, or 380 Vac).
3. Determine the output power capability needed by his design (the table covers the area of 40 to 4000 watts).

Tables 1 through 3 list devices by $V_{CEO\ (sus)}$ for use in bridge circuits at either 120, 220 or 380 volts. Tables 4 to 6 list devices by V_{CEV} for use in the push-pull, forward and flyback circuits at either 120, 220 or 380 volts. Within each table, the devices are grouped by the output power capability of that circuit, and the equivalent operating current level is also noted. Schematics of these circuits include references to available Motorola literature.

NOTE: MOTOR CONTROL

Many of the devices and the principles of operation discussed for switchmode power supplies apply to motor control systems using pulse width modulation techniques.

Particularly usefull are the MJ10000 series and BUT series of high power darlingtons which incorporate a free-wheel diode. The BUT16 and BUT36 are specifically designed for applications on the 3 phase 380 V mains supply. The BUT36 is capable of switching 30 Amps and 1 KV with fall times around 1μ sec.

Minimum Device Voltage Rating recommended for these three Circuits:
See Tables 1, 2 and 3, for recommended Devices.

Vin Vac	Vceo (sus) Vdc
120	200
220	400
380	600

FIGURE 1 — BASIC HALF-BRIDGE CONFIGURATION

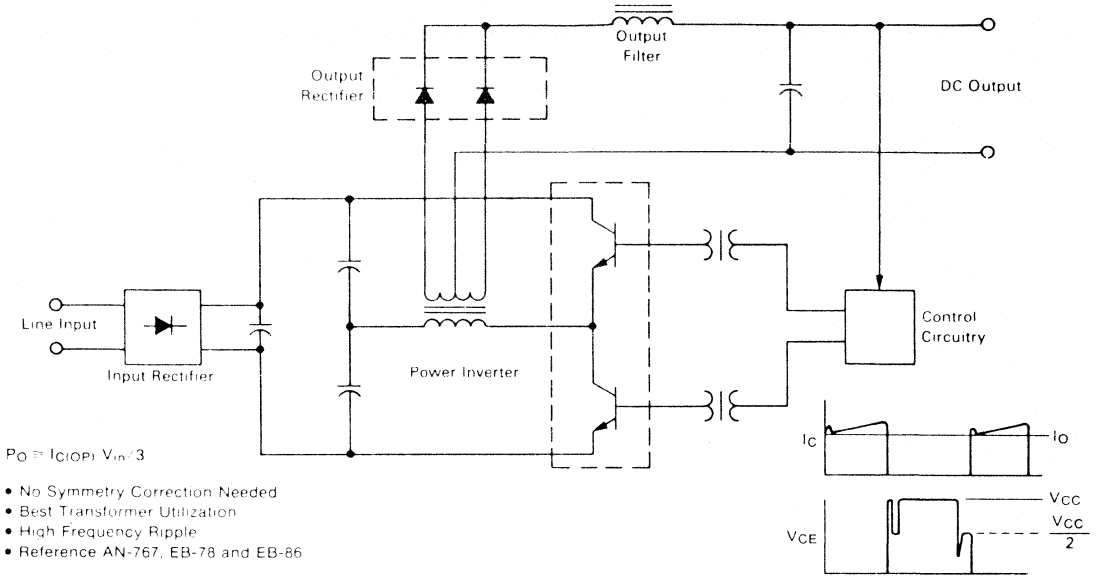
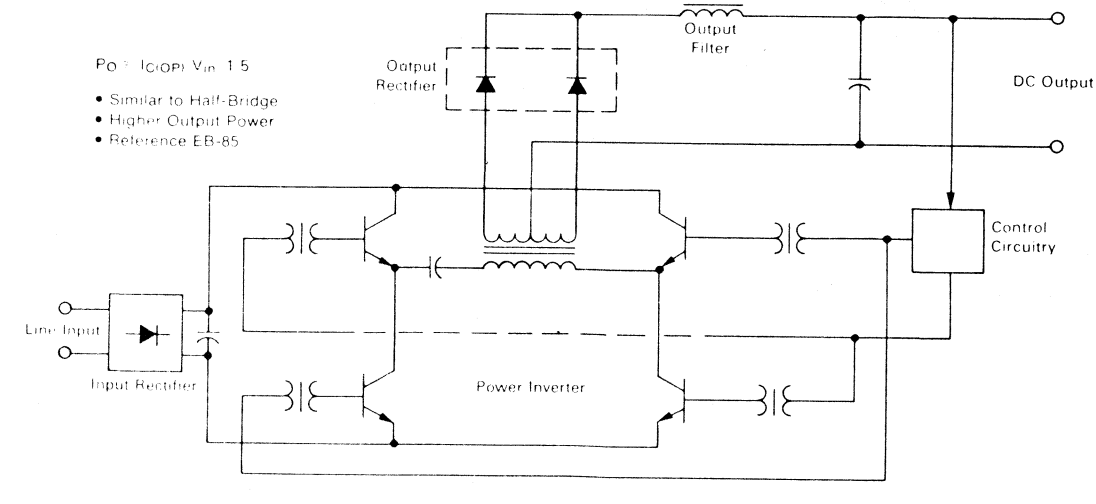


FIGURE 2 — BASIC FULL-BRIDGE CONFIGURATION



Minimum recommended Device Voltage Rating for these three Circuits:
See Tables 4, 5 and 6, for recommended Devices.

Vin Vac	Vcev Vdc
120	450
220	850
380	1400

FIGURE 3 — BASIC FORWARD CONVERTER

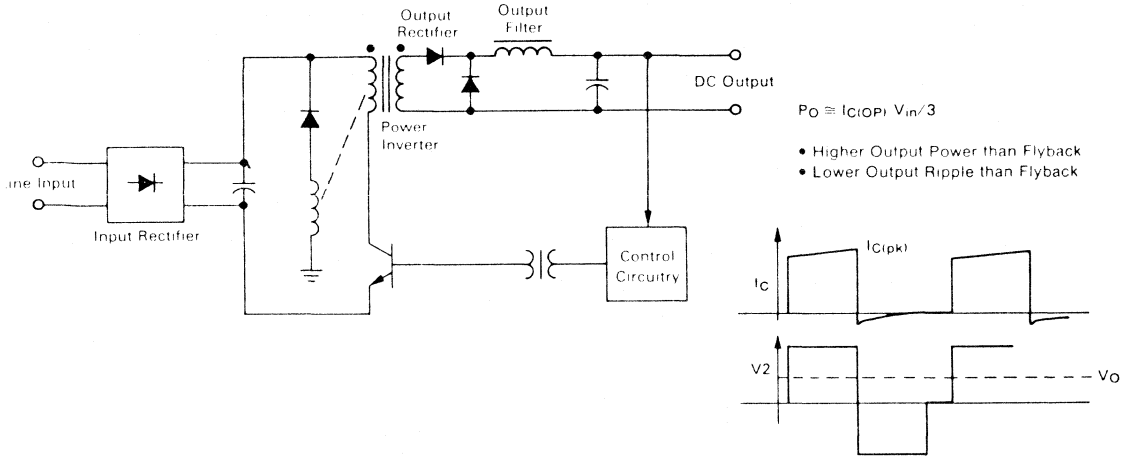


FIGURE 4 — BASIC PUSH-PULL CONFIGURATION

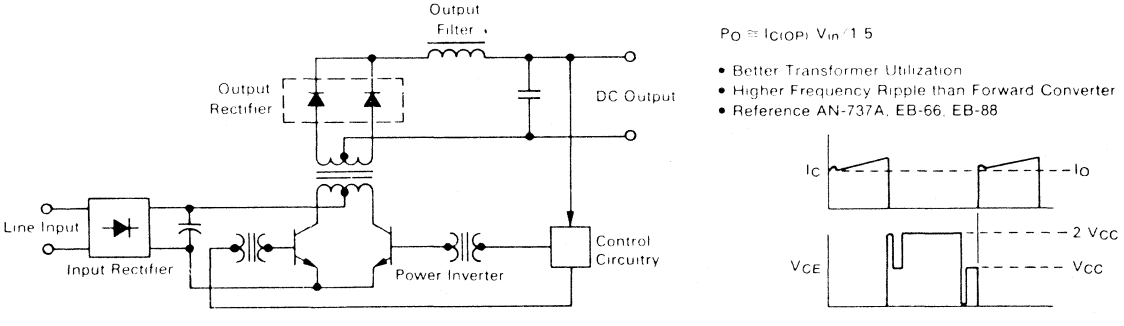


FIGURE 5 — BASIC FLYBACK CONFIGURATION

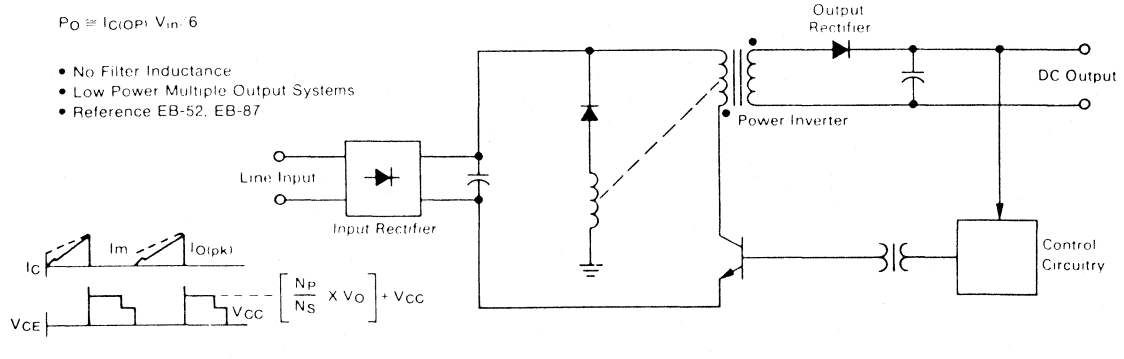


TABLE 1

CIRCUIT: Half and full* bridge (Fig. 1 & 2)

LINE VOLTAGE: 120 V_{RMS}

DEVICE BV_{CEO} RATING $\geqslant$ 200 V

POWER OUTPUT *(Watts)	IC OP (Amps)	METAL TO-66, TO-3	PLASTIC TO-126, TO-220	DARLINGTON TO-3
40	1	MJ4360	MJE13002	
80	2	MJ4380	MJE13004	
120	3	2N6542 MJ4400		
200	5	2N6544 MJ13014	MJE13006	MJ10006
320	8	MJ13014	MJE13008	
400	10	MJ13330 2N6546		MJ10004
800	20			MJ10015

*NOTE: Power output ratings are for half bridge (Fig. 1), Multiply by 2 for full bridge (Fig. 2).

TABLE 2

CIRCUIT: Half and full* bridge (Fig. 1 & 2)

LINE VOLTAGE: 220/240 V_{RMS}

DEVICE BV_{CEO} RATING $\geqslant$ 400 V

POWER OUTPUT *(Watts)	IC OP (Amps)	METAL TO-66, TO-3	PLASTIC TO-126, TO-220	DARLINGTON TO-3
80	1	MJ4361	MJE13003	
160	2	MJ4381	MJE13005	
240	3	MJ4401 2N6543		
400	5	2N6545 MJ13015	MJE13007	MJ10007
640	8	MJ13333	MJE13009	MJ10013
800	10	2N6547 MJ13333		MJ10005 MJ10008 BUT13
1600	20			MJ10015 BUT33

*NOTE: Power output ratings are for half bridge (Fig. 1), Multiply by 2 for full bridge (Fig. 2).

TABLE 3

CIRCUIT: Half and full* bridge (Fig. 1 & 2)

LINE VOLTAGE: 380 V_{RMS}

DEVICE BV_{CEO} RATING $\geqslant$ 600 V

POWER OUTPUT *(Watts)	IC OP (Amps)	METAL TO-3	DARLINGTON TO-3
240	2	MJ8500	
360	3	MJ8502	
600	5	MJ8504	
1000	8		BUT15
1200	10		MJ10014
2000	16		BUT35

*NOTE: Power output ratings are for half bridge (Fig. 1), Multiply by 2 for full bridge (Fig. 2).

TABLE 4

CIRCUIT: Forward, Push-Pull and Flyback* (Fig. 3, 4 and 5)

LINE VOLTAGE: 120 V_{RMS}

DEVICE BV_{CEV} RATING $\geqslant$ 450 V

POWER OUTPUT *(Watts)	IC OP (Amps)	METAL TO-66, TO-3	PLASTIC TO-126, TO-220	DARLINGTON TO-3
40	1	MJ4360	MJE13002	
80	2	MJ4380	MJE13004	
120	3	2N6542 MJ4400		
200	5	2N6544	MJE13006	MJ10006
320	8		MJE13008	
400	10	MJ13332 2N6546		MJ10004 BUT13
800	20			BUT33 MJ10015

*NOTE: Power output ratings are for forward converter (Fig. 3),
Multiply by 2 for push-pull (Fig. 4),
Divide by 2 for flyback (Fig. 5).

TABLE 5

CIRCUIT: Forward, Push-Pull and Flyback* (Fig. 3, 4 and 5)

LINE VOLTAGE: 220/240 V_{RMS}

DEVICE BV_{CEV} RATING $\geqslant$ 850 V

POWER OUTPUT *(Watts)	IC OP (Amps)	METAL TO-66, TO-3	PLASTIC TO-220 (800 V)	DARLINGTON TO-3
160	2	MJ4381 MJ8500	MJE13005A	
240	3	2N6543 MJ4401 MJ8502		
400	5	2N6545 MJ8504	MJE13007A	
600	8		MJE13009A	BUT14
800	10	2N6547		
1200	16			BUT34

*NOTE: Power output ratings are for forward converter (Fig. 3),
Multiply by 2 for push-pull (Fig. 4),
Divide by 2 for flyback (Fig. 5).

TABLE 6

CIRCUIT: Forward, Push-Pull and Fly Back* (Fig. 3, 4, 5)

LINE VOLTAGE: 380 V_{RMS}

DEVICE B_{VCEV} RATING $\geqslant$ 1400 V

POWER OUTPUT *(Watts)	IC OP (Amps)	METAL TO-3	DARLINGTON TO-3
250	2	MJ8501	
400	3	MJ8503	
600	5	MJ8505	
1000	8		BUT16
2000	16		BUT36

*NOTE: Power output ratings are for forward converter (Fig. 3),
Multiply by 2 for push-pull (Fig. 4),
Divide by 2 for flyback (Fig. 5).

HIGH VOLTAGE SWITCHING DARLINGTONS (NPN)

Vces / Ic	400	450	475	500	550	600	650	700	850	100	1400	APPROX Pd Tc = 25°C	PACKAGE
7	BU522*	BU522A*	BU522B*									75	TO-220
8												80	TO-3
10	BU323P BU323*	MJ10002+ MJ10006	BU323A*	MJ10003+ MJ10007	MJ10012*		MJ10013	MJ10014				175	SOT-93 TO-3
16											BUT16	100	TO-3
20		MJ10000+ MJ10004		MJ10001+ MJ10005			MJ10008	MJ10009		BUT15		175	TO-3
25									BUT14			175	TO-3
28						BUT13						175	TO-3
32											BUT36	200	TO-3(C197)
40										BUT35		250	TO-3(C197)
50						MJ10015		MJ10016	BUT34			250	TO-3(C197)
56						BUT33						250	TO-3(C197)

* AUTOMOTIVE IGNITION TYPES (NO SPEED UP DIODE)
+ NO SPEED UP DIODE.

HIGH VOLTAGE SWITCHING TRANSISTORS

(Vces ⩾ 650 V) (NPN-MESA) N.B.: + with integrated damper diode

Ic \ Vces	650	700	750	800	850	900	1000	1500	1700	APPROX Pd Tc = 25°C	PACKAGE
1.5		MJE13003 MJ4361			MJE13003A					40 40	TO-126 (REVERSE) TO-66
2.5								MJE12007 BU205		65	TO-220 TO-3
3 to 4		2N3902 MJ4381 MJE13005	BU126		BUX46 MJE13005A					100 75 75	TO-3 TO-66 TO-220
5 to 6	2N6542 MJ4400	MJ3030		BUX82 BU326 BU426	2N6543 MJ4401	BU326A BU426A	BUX83	BU208 BU208A BU500 BU208D+ BU800 +	BU209 BU209A	100 113 100	TO-3 SOT93 TO-66
8	2N6544	MJE13007 2N6308		BUX80	MJE13007A 2N6545 BUX47		BUX81			80 175	TO-220 TO-3
10				BUY69B			BUY69A			100	TO-3
12		MJE13009			MJE13009A		BUX48A			100 125	TO-220 TO-3
15	2N6546				2N6547 BUX48					175	TO-3
20	MJ13332	MJ13333	MJ13334	MJ13335						175	TO-3

HIGH VOLTAGE SWITCHING TRANSISTORS
(Vces ⩽ 600 V) (NPN-MESA) (PNP-PLANAR)

Ic \ Vces	200	225	275	300 NPN/PNP	350	375	400	450	475	500	600	APPROX Pd Tc = 25°C	PACKAGE
1					TIP47		TIP48	TIP49		TIP50		40	TO-220
1	PNP 175V 2N6420	2N3738	2N3583 / 2N6420	2N3891/ 2N5345/								35	TO-66
1.5											MJE13002 MJ4360	40	(TO-126 (REVERSE) TO-66
2			PNP2N6211		PNP 2N6212	2N3584/ 2N6421	PNP 2N6213			2N3585/ 2N6422/ 2N4240	2N6423	35	TO-66
4					2N6497 MJE51T		2N6498 MJE52T	2N6499 MJE53T			MJE13004 MJ4380	80 80 75 75	TO-220 TO-220 TO-220 TO-66
5	MJ410		2N6233 (250V)	2N6234 MJ411	2N6235					BUX45 MJ3029		50 120	TO-66 TO-3
7					BU407 (330V)		BU406					60	TO-220
8			PNP MJ6502		PNP MJE5850		PNP MJE5851	PNP MJE5852 BUX44 PNP MJ6503		BUX15 2N6306	MJE13006 2N6307	80 150 125	TO-220 TO-3 TO-3
10							ESM16A BUX43 MJ413 MJ423	ESM16 ESM16B BUX14		MJ13014 BUY69C	MJ13015	150	TO-3
12											MJE13008	100	TO-220
15		2N6249		2N6250		2N6251	BUX13			BUV25		150 to 250	TO-3
20							MJ13330	MJ13331 BUV24				175 250	TO-3
30							BUV23					250	TO-3

HIGH FT DRIVERS AND SWITCHING TRANSISTORS ⩽ 200 V BVceo (PLANAR)

Bvceo / Ic	60	75	80	90	100	120	125	140	150	160	175	200	APPROX Pd Tc = 25°C	PACKAGE
	NPN/PNP		NPN/PNP		NPN/PNP	NPN/PNP			NPN/PNP		NPN/PNP			
1											2N3580 / 2N6420		35	TO-66
1.5	BD137 / BD138		BD139 / BD140										10	TO-126
2							2N5050		2N5051			2N5052	40	TO-66
4	BD787 / BD788		BD789 / BD790 MJE240/ MJE250 MJE241/ MJE251 MJE242/ MJE252		BD791 / BD792 MJE243 / MJE253 MJE244 / MJE254								15	TO-126
7			2N5427 2N5428		2N5429 2N5430								40	TO-66
7.5	2N3445 2N3447		2N3446 2N3448										115	TO-3
8						MJE15028 / MJE15029			MJE15030 / MJE15031				50	TO-220
15												BUX41		TO-3
25					2N6338	2N6339	BUV10 BUV10N	2N6340 TEA6340	2N6341 TEA6341				200	TO-3
20		2N5039		2N5038			BUX40			BUX41N BUV11N		BUV11	140	TO-3
30				BUX39									125	TO-3
40										BUV21N		BUV21	250	TO-3
50					2N6274	2N6275	BUV20	2N6276	2N6277				250	TO-3(C197)

HIGH VOLTAGE SWITCHING TRANSISTORS (PLANAR)

Vceo / Ic	150	160	180	250		300		350		APPROX Pd Ta / Tc = 25°C	PACKAGE
	NPN	NPN	NPN	NPN [1]	PNP	NPN	PNP	NPN	PNP		
0.1				BF787	BF790	BF788	BF791	BF789	BF791	2 Ta	DUOWATT
0.1		BF457		BF458		BF459				12.5 Tc	TO-126
0.5						MPSU10	MPSU60			1 Ta	UNIWATT
0.5				BF460 BF757	BF760	BF461 BF758	BF761	BF462 BF759	BF762	2 Ta	DUOWATT
0.5				BD157 2N5655		BD158 2N5656 MJE340 BD232	MJE350	BD159 2N5657		20 Tc	TO-126
1	BF466		BF467	BF468						2 Ta	DUOWATT

HIGH FT DARLINGTONS (PLANAR)

Vceo / Ic	40		45		60		80		APPROX Pd Ta Tc = 25°C	PACKAGE
	NPN	PNP	NPN	PNP	NPN	PNP	NPN	PNP		
2	BD411 BD412	BD413 BD414							2 Ta	TO-202
2	MPSU45	MPSU95							1 Ta	UNIWATT
4			BD775	BD776	BD777	BD778	BD779	BD780	15 Tc	TO-126

HIGH FT DRIVERS AND SWITCHING TRANSISTORS (PLANAR)

Vceo / Ic	20		30		40		45		60		80		100		APPROX Ta Pd Tc = 25°C	PACKAGE
	NPN	PNP	NPN	PNP	NPN	PNP	NPN	PNP	NPN	PNP	NPN	PNP	NPN	PNP		
1.5							BD135	BD136	BD137	BD138	BD139	BD140			10 Tc	TO-126
2	BD505	BD506	BD507 MPSU01	BD508 MPSU51	BD509 BD515 MPSU01A	BD510 BD516 MPSU51A			BD517 BD525 MPSU05	BD518 BD526 MPSU55	BD519 BD527 MPSU06	BD520 BD528 MPSU07	BD529 MPSU57	BD530 MPS457	1 Ta	UNIWATT
2									BD415 BD385	BD416 BD386	BD417 BD387	BD418 BD388	BD419 BD389	BD420 BD390	2 Ta	DUOWATT
4	BD361 BD361A	BD362 BD362A					BD785	BD786	BD787	BD788	BD789 MJE240 MJE241 MJE242	BD790 MJE250 MJE251 MJE252	BD791 MJE243 MJE244	BD792 MJE253 MJE254	15 Tc	TO-126
5			MJE200 (25 V)	MJE210 (25 V)											15 Tc	TO-126

MOTOR CONTROL

Many of the devices and the principles of operations discussed for switchmode power supplies apply to motor control systems using pulse width modulation techniques.

Particularly usefull are the MJ10000 series and BUT series of high power darlingtons which incorporate a free-wheel diode. The BUT16 and BUT36 are specifically designed for applications on the 3 phase 380 V mains supply. The BUT36 is capable of switching 30 Amps and 1 KV with fall times around 1 μsec.

SWITCHMODE REGULATION CONTROL AND PROTECTOR CIRCUITS

LINEAR IC'S

MC 3420
TL 494 / TL 495
μA 78S40

MC 3423
MC 3524 / MC 3525

A - REGULATION CONTROL CIRCUITS

As described above the switchmode IC'S provide the pulse width Modulation (PWM) control for the supply. Devices such as the MC 3420, TL 494 or μA 78S40 have several sections:

DC Supply section

This section specifies the maximum ratings for the supply voltage (min and max) and the max supply current.

Reference section

A stable reference voltage (band gap principle) is generated primarily for internal use. However, it is also available externally for use in setting the dead time and for use as a reference for the external control loop error amplifier. This reference voltage is guaranted with a min/max value. The line and load regulations and the change with temperature (delta) are also specified.

Oscillator section

Depending on device type, the frequency of the oscillator section may be set from 1 to 300 KHZ (TL 494) with an external resistor and capacitor. Even with variations in line voltage and temperature the ramp frequency remains stable to within approximatively from 2% to 4%.

Pulse width modulation section

The P.W.M. is a comparator of the oscillator section (used as reference) and external V control. The level of the V control determines the output pulse width or duty cycle.

The triangular wave generated by the oscillator, is compared by the Internal comparator to the external control voltage applied. The result is a P.W.M. wave where pulses appear alternately at the two outputs.

Dead time comparator section

An additional comparator has been included to allow independant adjustement of system dead time or maximum duty cycle. This dead time is obtained for prevention of inverter switching transistor cross conduction at high duty-cycle due to storage time delays. Normally the max and min input threshold voltage are controlled at zero and maximum duty cycle.

Pulse steering flip-flop section

A toggle flip-flop functions as phase splitter, producing complementary pulse trains that are out of phase by 180° for controlling multiple transistor switching supplies. The clock signal for the flip flop is derived by "AND ing" the output of the P.W.M. comparator and a signal from the ramp generator circuit. This "AND" gate ensures that the swichmode outputs truly alternate.

The inhibit input current at low and high state are controlled as in the "fonctional table".

Output section

The output transistors are open collector devices capable of sinking up to 50 to 200 mA (depending on type) and blocking up to 40 V. They may be operated separately for push pull control. The last generation in development (μA 78S40) incorpores a power section and is able to deliver 1500 mA max.

MC 3420

SWITCHMODE REGULATOR CONTROL CIRCUIT

The MC3520/3420 is an inverter control unit which provides all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

These devices are designed to supply the pulse width modulated drive to the base of two external power transistors. Other applications where these devices can be used are in transformerless voltage doublers, transformer coupled dc-to-dc converters and other power control functions.

The MC3520 is specified over the military operating range of −55°C to +125°C. The MC3420 is specified from 0°C to +70°C.

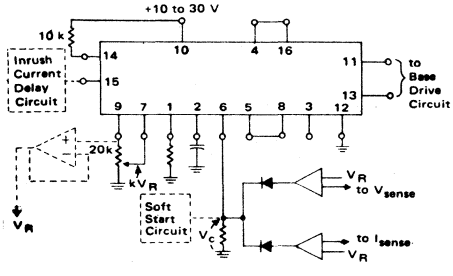
- Includes Symmetrical Oscillator
- On Chip Pulse Width Modulator, Voltage Reference, Dead Time Comparator, and Phase Splitter
- Output Frequency Adjustable (2 kHz to 100 kHz)
- Inhibit and Symmetry Correction Inputs Available
- Controlled Start-Up
- Frequency and Dead Time are Independently Adjustable (0% to 100%)
- Can be Slaved to Other MC3420s
- Open Collector Outputs
- Output Capability 50 mA (Max.)
- On Chip Protection Against Double Pulsing of Same Output During Load Transient Condition

THE CIRCUIT

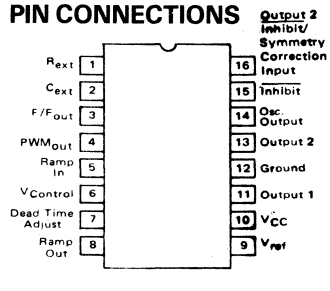
This product operates from a power supply voltage of 10 to 30 V, internally generating a reference voltage of approximatively 7.8 V that is stable to within ±0,02%/°C. The ramp generator produces a symetrical triangular waveform ramping between 2,4 V and 6 V; this output is connected to a pulse width modulation comparator which receives also the Vcontrol information. The level of the Vcontrol determines the output pulse width or duty cycle.

For to prevent output voltage overshoots and magnetizing current imbalances in the power transformer primary a soft start circuit is included.

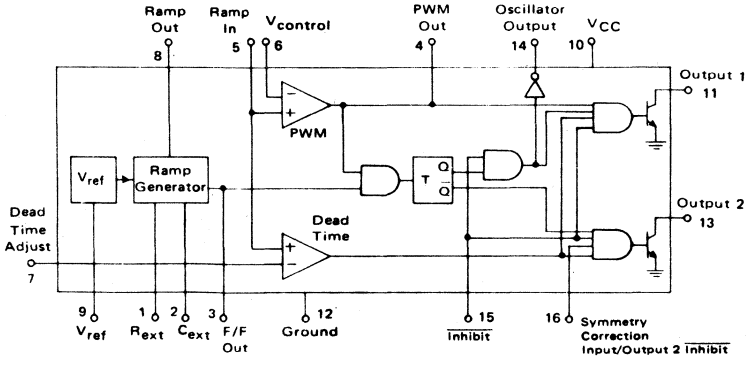
TYPICAL APPLICATION



PIN CONNECTIONS



BLOCK DIAGRAM



TL 494 / TL 495

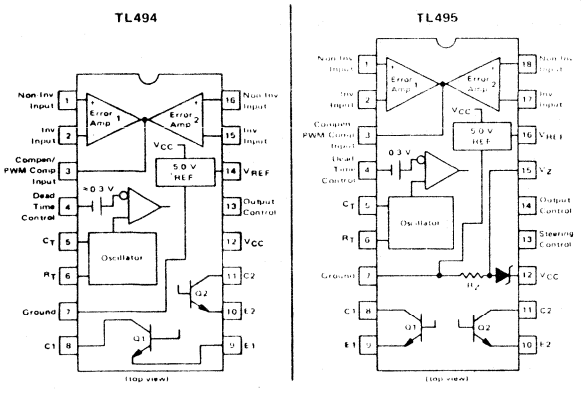
SWITCHMODE
PULSE WIDTH MODULATION
CONTROL CIRCUITS

The TL494 and TL495 combine the best feature of existing PWM control circuits and add other on-chip functions. These devices provide, on a single monolithic chip, all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

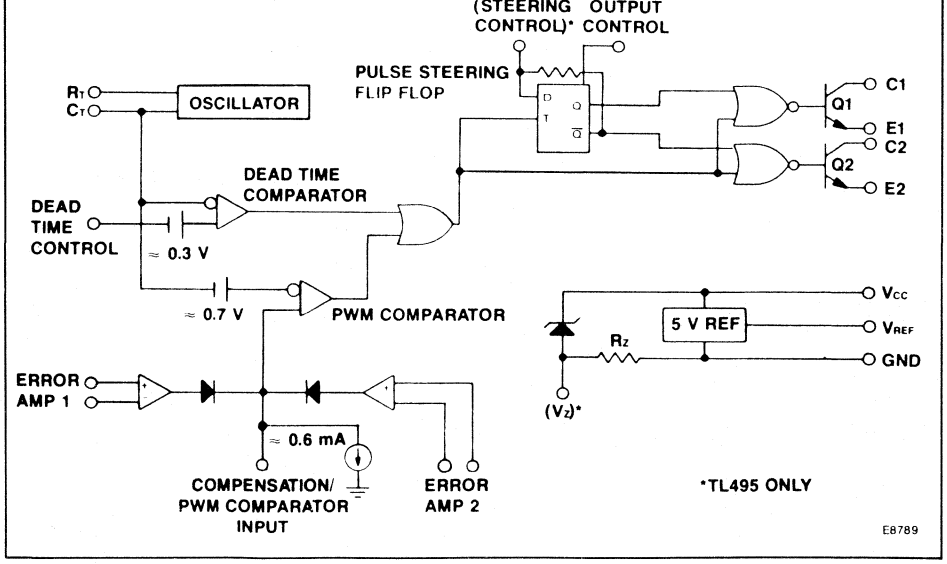
The TL494M/495M are specified over the military operating range of −55°C to +125°C. The TL494C/495C are specified from 0°C to +70°C.

- Uncommitted Output Transistors Capable of 200 mA Source or Sink
- On-Chip Error Amplifiers
- On-Chip 5 V Reference
- Internal Protection from Double Pulsing of Outputs with Narrow Pulse Widths or with Supply Voltages below Specified Limits
- Dead Time Control Comparator
- Pulse-Steering Flip-Flop and Output Control Circuitry
- Easily Synchronized (Slaved) to Other Circuits
- On-Chip 39 V Zener for High Voltage (V_{IN} > 40 V) Applications (TL495 only)
- Output Steering Control Pin Overrides Internal Pulse Steering Flip-Flop (TL495 only)

PIN CONNECTIONS



TL494 BLOCK DIAGRAM



μA 78S40

GENERAL DESCRIPTION

The μA78S40 is a Monolithic Regulator Subsystem consisting of all the active building blocks necessary for switching regulator systems. The device consists of a temperature-compensated voltage reference, a duty-cycle controllable oscillator with an active current limit circuit, an error amplifier, high-current, high-voltage output switch, a power diode and an uncommited operational amplifier. The device can drive external npn or pnp transistors when currents in excess of 1.5 A or voltages in excess of 40 V are required. The device can be used for step-down, step-up or inverting switching regulators as well as for series pass-regulators. It features wide supply voltage range, low standby power dissipation, high efficiency and low drift. It is useful for any stand-alone, low part-count switching system and works extremely well in battery operated systems.

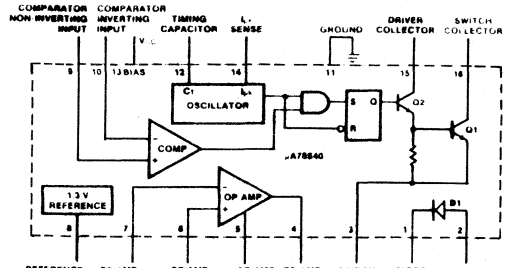
- Step-Up, Step-Down or Inverting Switching Regulators
- Output Adjustable from 1.3 to 40 V
- Peak Currents to 1.5 A Without External Transistors
- Operation from 2.5 TO 40 V Input
- Low Standby Current Drain
- 80 DB Line and Load Regulation
- High gain, High Current, Independent op Amp

THE CIRCUIT

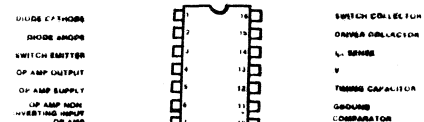
One of the main advantages of this circuit is the output transistor capable of 1500 mA or Voltage in excess of 40 volts. The 1.245 voltage reference has a line regulation of 0.04mV/V. The common mode voltage range operable from both the negative rail and above the positive rail.

The μA 78S40 operates from a power supply voltage of 2.5 V to 40 V. If we look at the block diagram we can see that in a single low cost dip the μA 78S40 incorporates those functions common to all customs. Frequency PWM control schemes for switching supplies. The chip is a mixture of both linear and digital circuitry its linear functions include an oscillator, a voltage reference, a comparator, an operational amplifier, two output driver transistors. In the digital section is a flip flop which serves as a phase splitter, its driving output transistors.

BLOCK DIAGRAM



PIN CONNECTIONS

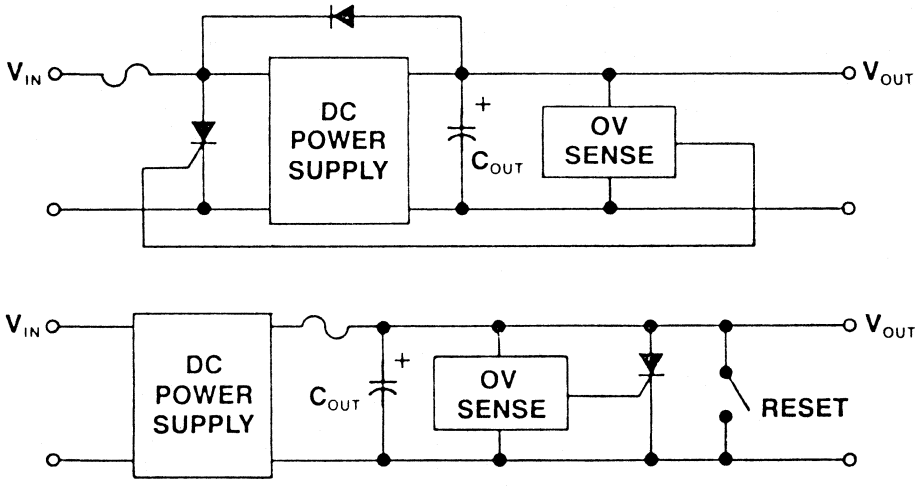


B - VOLTAGE PROTECTOR CIRCUITS

Motorola has developed separate IC'S for the over and under voltage protection of Power supplies.

These circuits protect sensitive Electronic circuitry from over/under voltage transients or regulator failures when used in conjunction with an external "crow bar" SCR. The sense the over/under voltage condition and quickly "crow bar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker. The protection voltage threshold are adjustable and these circuits can be programmed for minimum duration of over/under voltage condition before tripping for noise immunity — for more details, see AN 789.

TYPICAL CROWBAR OVP CIRCUIT CONFIGURATIONS



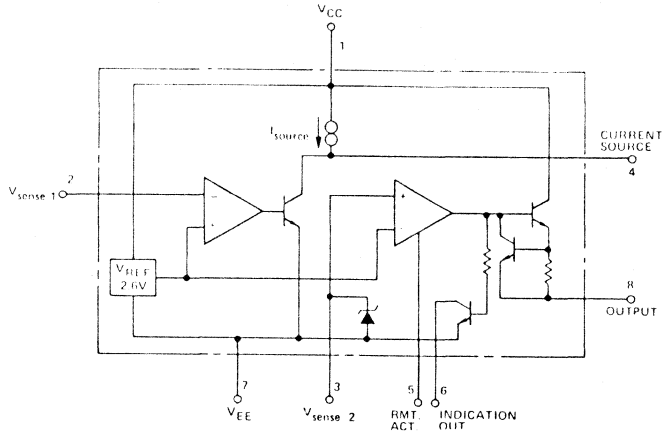
The circuits are:

MC 3423/3523 : over voltage protector
MC 3424/3524 : over/under voltage protector (16 pins version)
MC 3425 : over/under voltage protector (8 pins version)
(+ low cost)

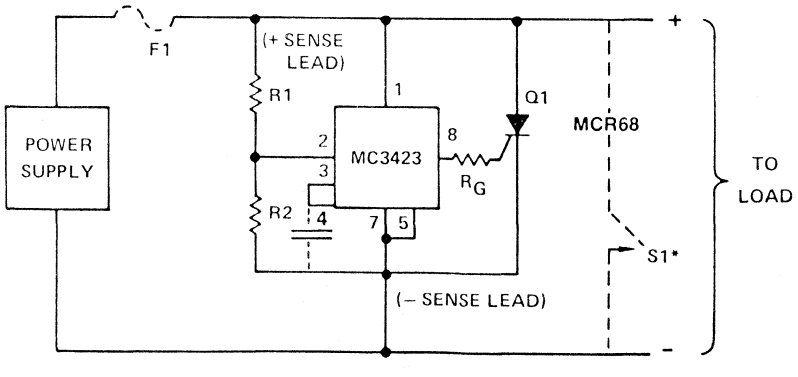
MC 3423 OVER VOLTAGE SENSING CIRCUIT

- MIN. OVERVOLTAGE DURATION BEFORE TRIP ADJUSTABLE FROM 1μS TO 1MS WITH EXTERNAL CAPACITOR (0 TO .1μF)
- REMOTE ACTIVATION INPUT (CMOS, TTL, DTL COMPATIBLE)
- ACTUATION INDICATION OUTPUT
- AVAILABLE IN PLASTIC (0°C TO 70°C) OR CERAMIC (−55°C TO 125°C) MINI-DIP PKGS
- SECOND SOURCED BY T.I.

MC 3423 EQUIVALENT CIRCUIT



MC 3423 TYPICAL APPLICATION



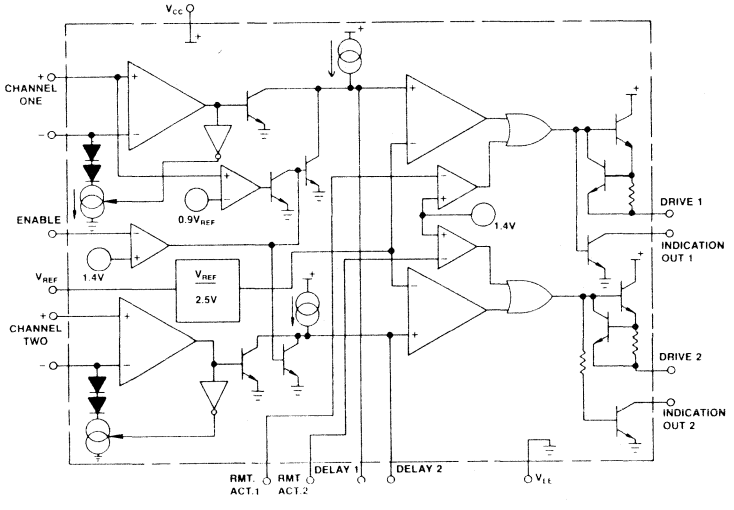
$$TRIP = V_{REF}\left(1+\frac{R1}{R2}\right) \approx 2.6V\left(1+\frac{R1}{R2}\right)$$

R2≤10KΩ FOR MINIMUM DRIFT

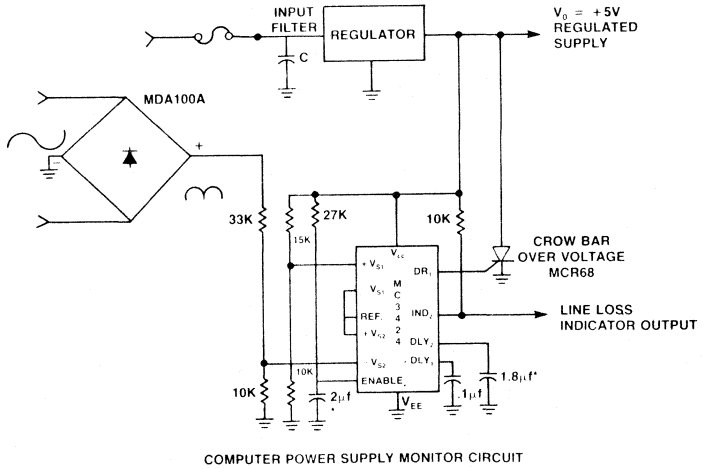
MC3424/MC3524 POWER SUPPLY SUPERVISORY CIRCUIT

- TWO INDEPENDENT INDICATOR OUTPUTS CAPABLE OF SINKING 30 MA.
- MINIMUM OVER AND UNDER VOLTAGE DURATION BEFORE TRIP ADJUSTABLE FROM 1μS TO 1ms WITH EXTERNAL CAPACITOR (0 — .1μF)
- SEPARATE REMOTE ACTIVATION INPUTS (CMOS, TTL, DTL COMPATIBLE) FOR EACH CHANNEL.
- ENABLE INPUT (CMOS, TTL, DTL COMPATIBLE) FOR CONTROL OF EITHER CHANNEL 2 OR BOTH CHANNELS DEPENDING ON CHANNEL 1 INPUT CONDITIONS.
- EACH CHANNEL CAN BE OPERATED CLOSED LOOP WITH GAIN OR UNITY GAIN — STABILIZED AT THE DELAY PIN.
- AVAILABLE IN 16 PIN PLASTIC (0° TO 70°C) OR CERAMIC (55°C TO 125°C) DIP PACKAGES.

MC 3424 / MC 3524 EQUIVALENT CIRCUIT



MC 3424 TYPICAL APPLICATION



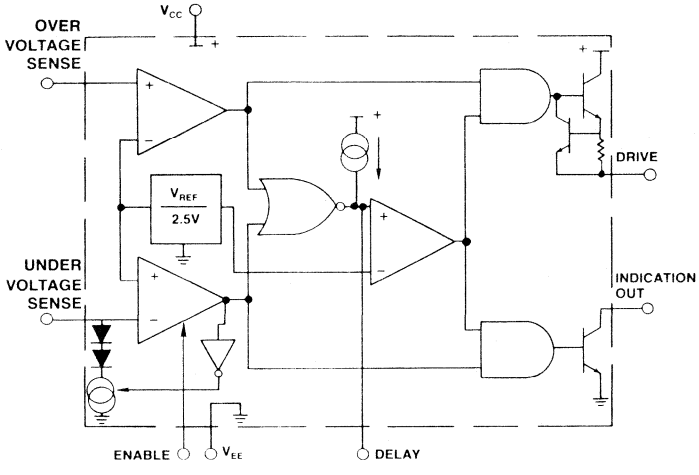
COMPUTER POWER SUPPLY MONITOR CIRCUIT

*18msec DELAY

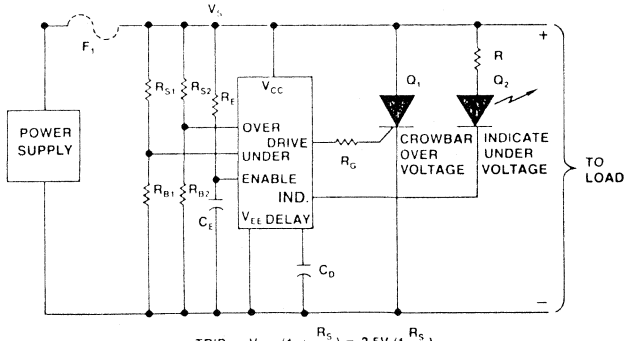
MC3425/MC3525 OVER-UNDER VOLTAGE SENSING CIRCUIT

- DEFICATED OVER AND UNDER VOLTAGE COMPARATORS REFERENCED TO 2.5V
- OVER VOLTAGE DRIVE OUTPUT CAPABLE OF SOURCING 300 mA AT A SLEW RATE OF 200 – 400 mA/μS FOR TRIGGERING A CROWBAR SCR
- UNDER VOLTAGE INDICATOR OUTPUT CAPABLE OF SINKING 30 MA
- MINIMUM OVER – UNDER VOLTAGE DURATION BEFORE ACTIVATION ADJUSTABLE FROM 1μS TO 1ms WITH EXTERNAL CAPACITOR (0 TO .1μF)
- ENABLE INPUT, CONTROLLING UNDER VOLTAGE COMPARATOR (CMOS, TTL, DLT COMPATIBLE)
- PROGRAMABLE HYSTERISIS OF UNDER VOLTAGE COMPARATOR
- AVAILABLE IN PLASTIC (0°C TO 70°C) OR CERAMIC (–55°C TO 125°C) MINI-DIP PKG.

MC 3425 / MC 3525 EQUIVALENT CIRCUIT



MC 3425 TYPICAL APPLICATION



$$TRIP = V_{REF}\left(1 + \frac{R_S}{R_B}\right) = 2.5V\left(1 \frac{R_S}{R_B}\right)$$

R_B 10K FOR MINIMUM DRIFT

$$R_E = \frac{T}{C_E \mathrm{Ln}\left(\frac{V_S}{V_S - V_E}\right)}$$

$$C_D = \frac{I_S T_D}{V_{REF}} = \frac{200\ \mu A\ T_D}{2.5V}$$

POWER

RECTIFIERS

INTRODUCTION

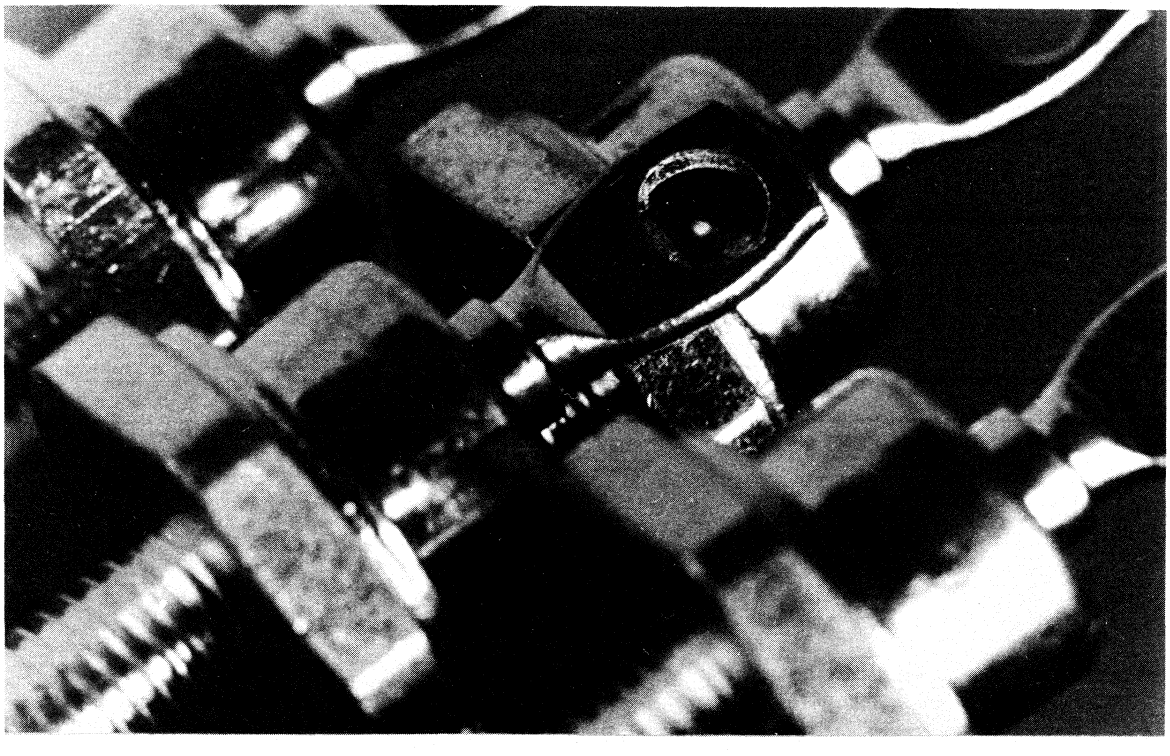
The basic problem concerning power supply is that a significant amount of power available at the input to the power supply is dissipated by rectifying element in supplies using conventional silicon rectifiers, thus reducing the efficiency of the supply. MOTOROLA fast/soft recovery and schottky rectifiers have been developed to provide fast recovery time, low forward drop and low power loss.

The use of a barrier metal as in schottky diode, reduces the band gap well below that of conventional p-n junctions. The resulting low forward drop is one of the major advantage of the schottky device, but it is also accompanied by an increase in reverse current according to the law of the junction (see § A).

Because the reverse power dissipation is not negligeable and increase with temperature a proper attention must be devoted to the thermal design to avoid thermal runaways (§ A.V and B.IV.).

As discussed in the § B the knowledge of the rectifier operating condition used in the main switchmode configuration will allow the choice of an optimal product among our device family (see § C).

TABLE OF CONTENTS



A.I. JUNCTION STRUCTURE

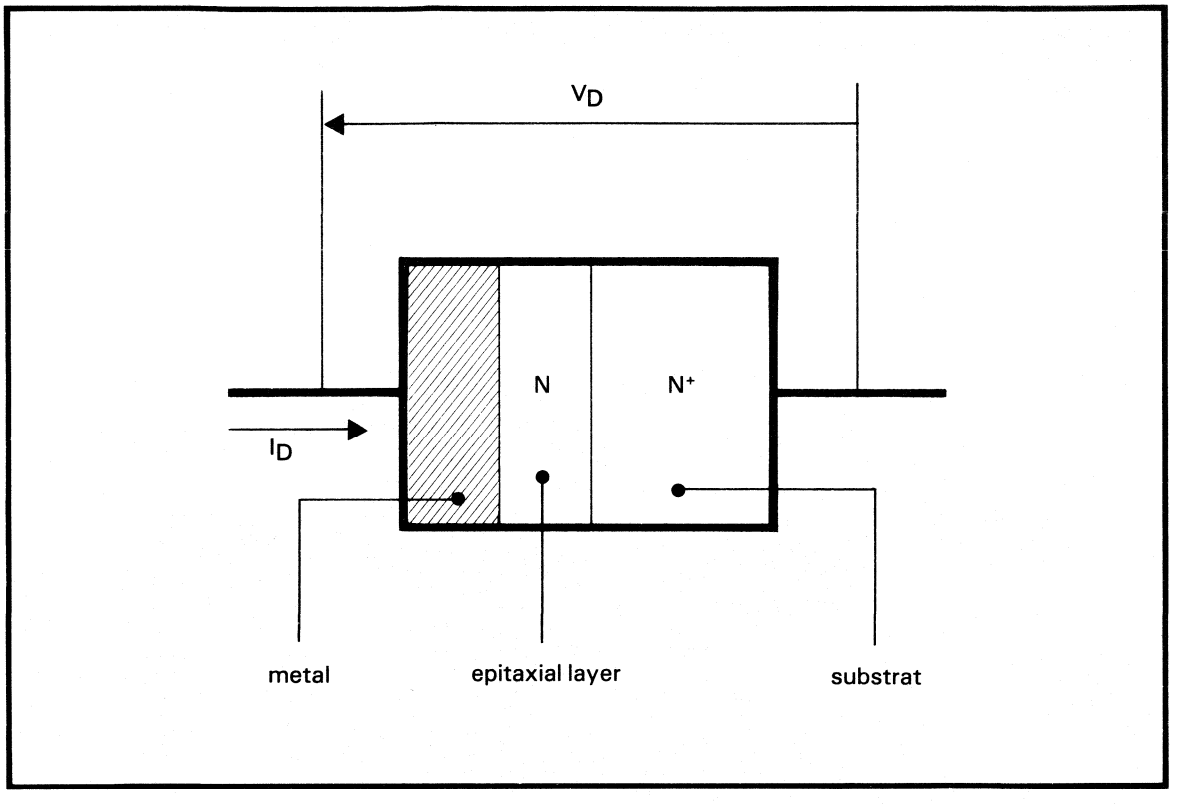


FIGURE 1

A schottky diode consists of a junction of semiconductor material which is epitaxially grown N type on a N^+ substrate, and a metal layer which plays the role of a P^+ region. In theory the metal – N metal interface can be considered as a typical P^+N junction.

In such a structure of metal – N, the current which flows thru the diode is by majority carriers, while in the PN junction, conduction is by minorities carriers. The life of the majority carriers is such shorter then that of the minority carriers which is the most important advantage of this structure. Compared to a classical PN junction, the reverse recovery time of a schottky diode is pratically zero.

It is therefore the nature of the metal – N junction which assures the very low reverse recovery times. Contrarily the gold doped fast recovery diode's time are quite dependant on process quality and control. For the schottky diode, the reverse recovery time is negligible in principal, therefore it is not specified as a device parameter.

The actual structure used for MOTOROLA schottkys is shown below in cross section.

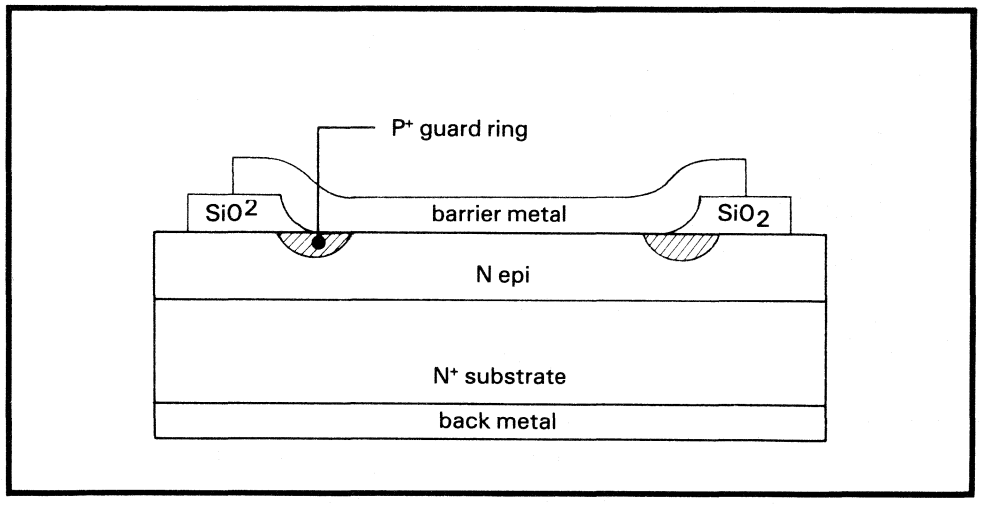
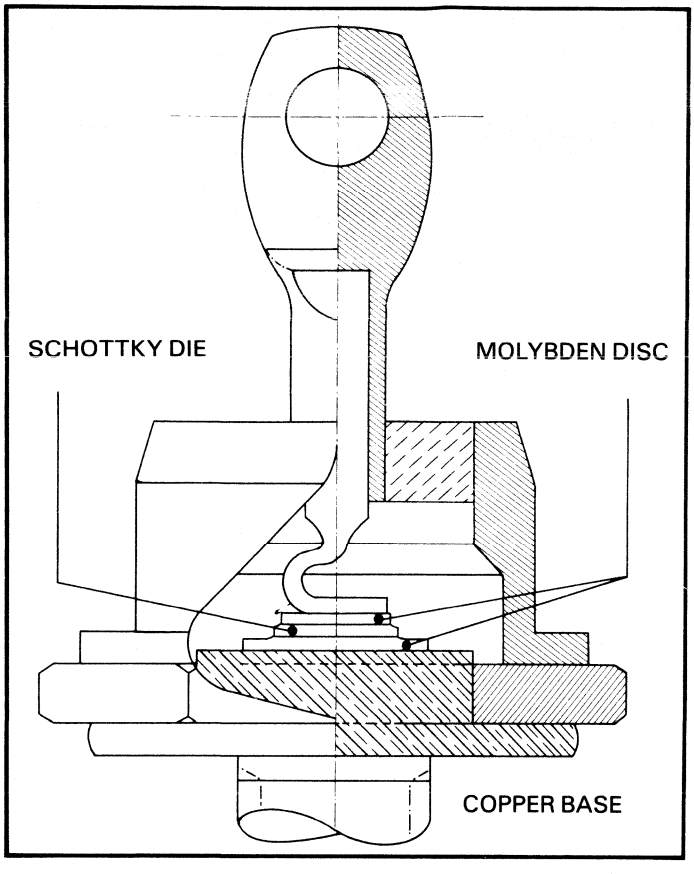


FIGURE 2

MOTOROLA schottky employ a special P^+ guard ring as shown in fig. 2. This guard ring is very effective in reducing field concentration edge effects between the metal – N junction which reduces reverse breakdown voltage. In reverse bias, the radius of curviture from the PN junction depletion is much larger then the schottky alone would have at the edge of the metal contact. Thus the field concentration is reduced and the breakdown voltage is increased by the PN guard ring. Electrically the PN junction is in parallel with the schottky junction and should also serve as a transient suppressor in applications of reverse bias. That is the PN junction avalanches before the "schottky" junction.

MOTOROLA SCHOTTKY RECTIFIERS



A PERFORMING STRUCTURE

A TOP LEVEL HIGH QUALITY PROCESS

- "ZERO DEFECT" WAFER SELECTION
- ION IMPLANTED P^+ ANNULAR RING
- TRIPLE LAYER FRONT GOLD METALLIZATION
- 100% DICE PROBED
- "SANDWICHES" ASSEMBLY WITH MOLYBDENUM DISCS
- TEMPERATURE STABILIZATION BAKE
- 100% ELECTRICAL AND VISUAL "SANDWICHES" TEST
- AFTER ASSEMBLY 100% TEMPERATURE STORAGE AND TEMPERATURE CYCLING PER MIL STD COND B
- 100% FINAL TEST WITH TEMPERATURE GUARANTEE
- CONTINUOUS LINE AUDIT AND RELIABILITY PROGRAM

A.II. FORWARD CHARACTERISTICS

In a metal – N diode the current density, J, of the junction can be expressed as:

$$J = Js \exp\left(\frac{qV}{KT} - 1\right)$$

II-1 $$J = Js \exp\left(\frac{qV}{KT}\right) \text{ when } V > 0.1 \text{ Volt}$$

where Js is the satured current density expressed as:

II-2 $$Js = RT^2 \exp\left(\frac{-q\varnothing B}{KT}\right)$$

where: R = Richardson constant
= 120 A/cm² × (°K)²

T = absolute temperature (°K)

K = Bolzman's constant
= 8.62 × 10^{-5} eV/°K

q = electron charge
= 1.6 × 10^{-19} coul.

∅B = barrier height (eV)

The **barrier height**, ∅B, represents the energy barrier level for charge transfer at the metal – N interface. For a voltage applied in excess of this energy level, the junction will allow the flow of charge. Therefore the barrier height, ∅B, is a very important parameter. ∅B is dependent on the physical quality of the metal – N interface and the type of the metal used as indicated in Table I.

METAL	∅B (eV)
Pt	0.87
Mo	0.59 to 0.68
Ni Pt	0.65 to 0.75
Ni	0.60
Cr	0.55 to 0.65

Therefore it is the physical metal-Si interface which causes the principal difficulties in the industrial fabrication of a schottky diode. If it is not closely controlled, the variations in $\varnothing B$ can drastically change the most important forward and reverse characterizations.

Application example

a) Procedure for calculating the satured current density, Js, for chrome and nickel platinium metals.

$$Js = RT^2 \exp \frac{-q \varnothing B}{KT}$$

where $R = 120$
$KT/q = 26$ mV (room temperature)

For the nickel platinum, $\varnothing B = 0.7$ ev

$$Js = 120 \times (300)^2 \times \exp \frac{-q \varnothing B}{KT}$$

$$= 1.08 (10^7) \times 2.03 (10^{-12})$$

$$= 2.19 (10^{-5}) \text{ A/cm}^2$$

$$Js = 0.02 \text{ mA/cm}^2$$

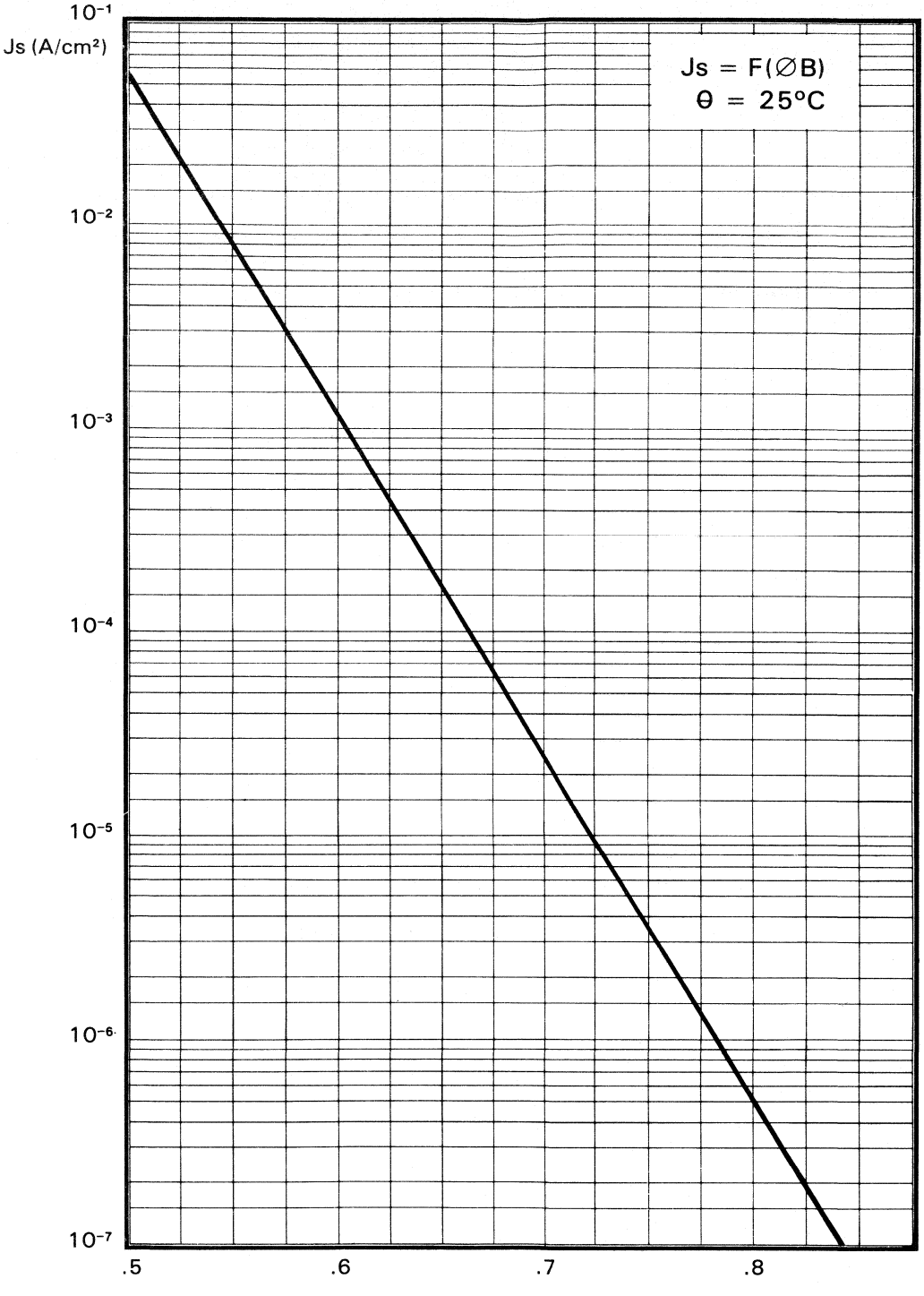
For the chrome, $\varnothing B = 0.6$ eV

$$Js = 1.08 (10^7) \times 9.5 (10^{-11})$$

$$= 9.7 (10^{-4}) \text{ A/cm}^2$$

$$Js = 1 \text{ mA/cm}^2$$

Therefore at 25°C, the nickel platinum's $Js = 0.02$ mA/cm² while the chrome exhibits $Js = 1$ mA/cm².


Js (A/cm²)
10⁻¹
10⁻²
10⁻³
10⁻⁴
10⁻⁵
10⁻⁶
10⁻⁷
Js = F(∅B)
θ = 25°C
.5
.6
.7
.8
(∅B Volts)
∅B (volts)

CURVE 1

The junction Cr-N has a saturation current in magnitudes of 50 times of that for Ni Pt – N. Curve 1 shows the typical values for Js as a function of ∅B (which is relative to the metal used) at 25°C.

b) **Procedure for calculating VF**

From equation II.I and II.2., VF can be expressed as:

II.3. $$VF = \varnothing B + \frac{KT}{q} \text{Ln} \frac{JF}{RT^2}$$

or at 25°C

$$VF_{mV} = (\varnothing B_{mV} - 600) + 26 \text{ Ln } JF \text{ (mA)}$$

For a given value of JF, the value of VF is directly dependent on the ∅B of the device.

Example – calculate VF for a JF = 4 A/cm² for chrome and nickel platinum:

Chrome – ∅B = 600 mV or VF = 26 Ln 4000
= 215 mV
Ni Pt – ∅B = 700 mV orVF = 315 mV

Therefore the Cr – Si junction exhibits a much better VF then the Ni Pt, on the order of 100 mV at a current density, JF = 4 A/cm².

To realize the actual VF on the schottky diode, the series resistance, Rs, in the epitaxial zone must be included, i.e.:

V_T = VF + V series
= VF + JF A Rs

Where: A = surface of the diode

Rs = series resistance $\frac{\rho \times e}{A}$

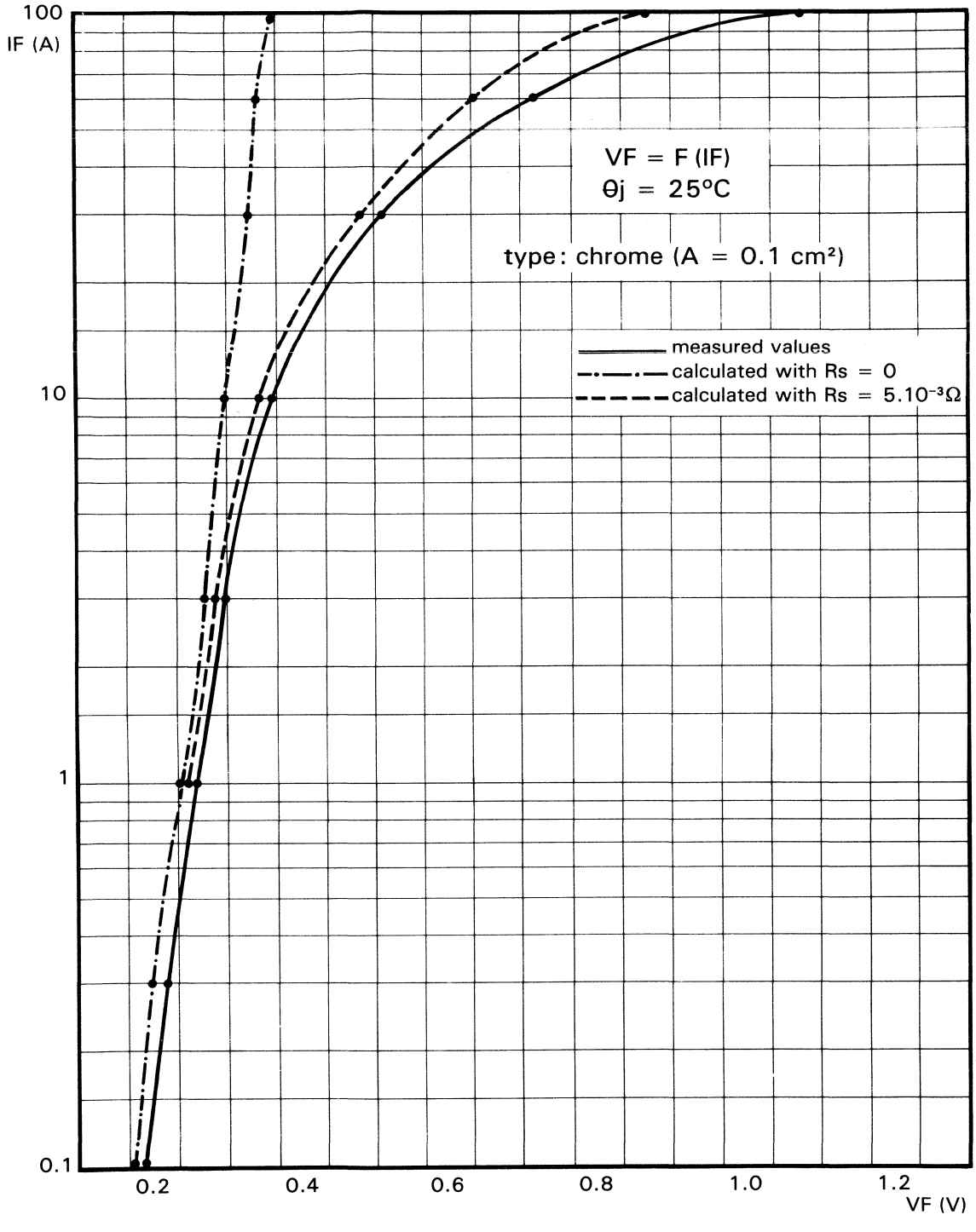
= epitaxial resistance

e = thickness

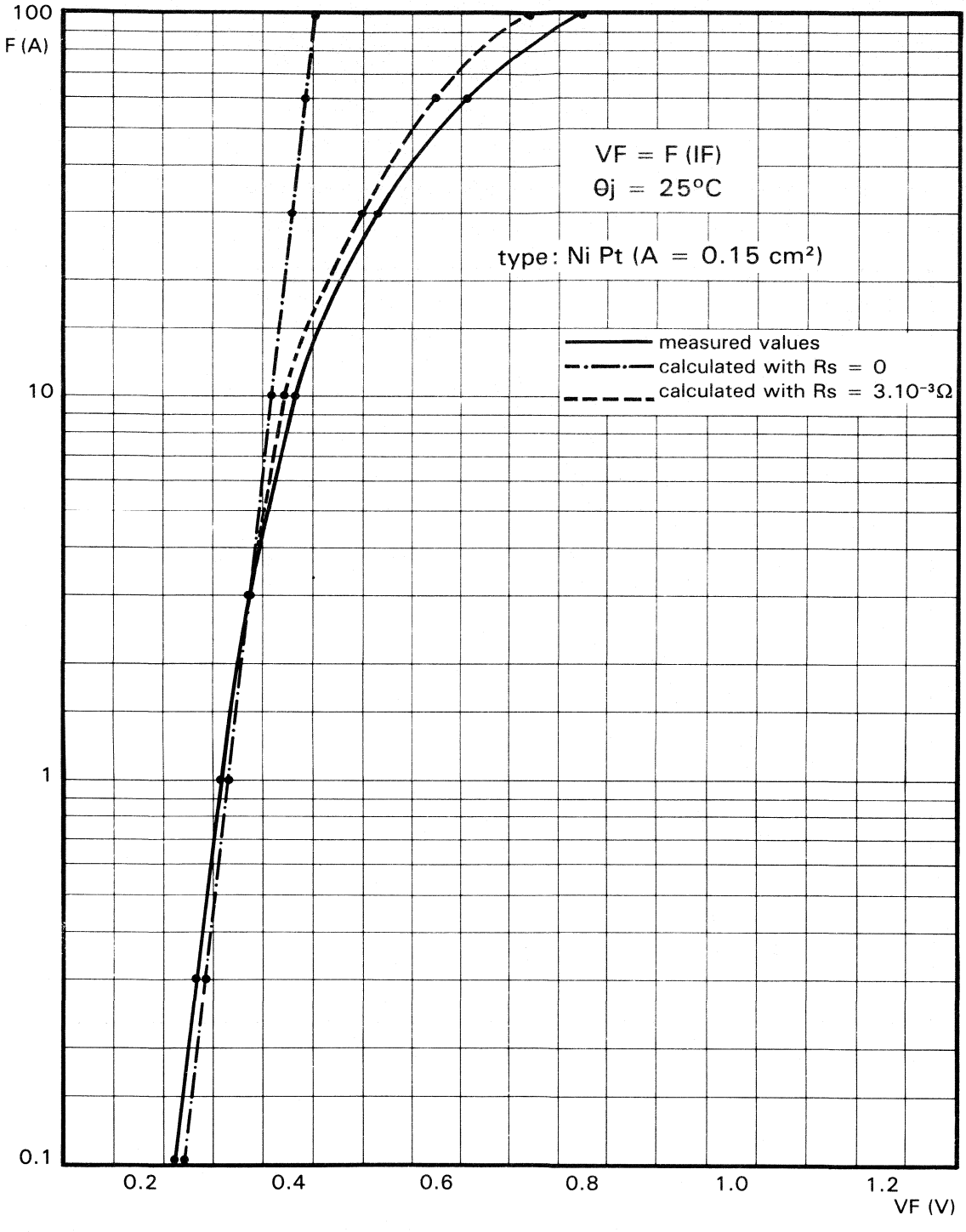
In practice, Rs is in the order of 10^{-3} Ohm and it will have negligible effects at current densitys in the order of Js = 10 A/cm².

Curves 2 and 3 contain theorical and measured values for MOTOROLA's chrome and Ni Pt Lines.

In comparing the schottky VF with std PN junctions the VF advantages can be seen in curve 4.


100
IF (A)
10
1
0.1
0.2
0.4
0.6
0.8
1.0
1.2
VF (V)
VF = F (IF)
θj = 25°C
type: chrome (A = 0.1 cm²)
measured values
calculated with Rs = 0
calculated with Rs = 5.10⁻³Ω

CURVE 2


100
F (A)
10
1
0.1
VF = F (IF)
θj = 25°C
type: Ni Pt (A = 0.15 cm²)
measured values
calculated with Rs = 0
calculated with Rs = 3.10⁻³Ω
0.2
0.4
0.6
0.8
1.0
1.2
VF (V)

CURVE 3

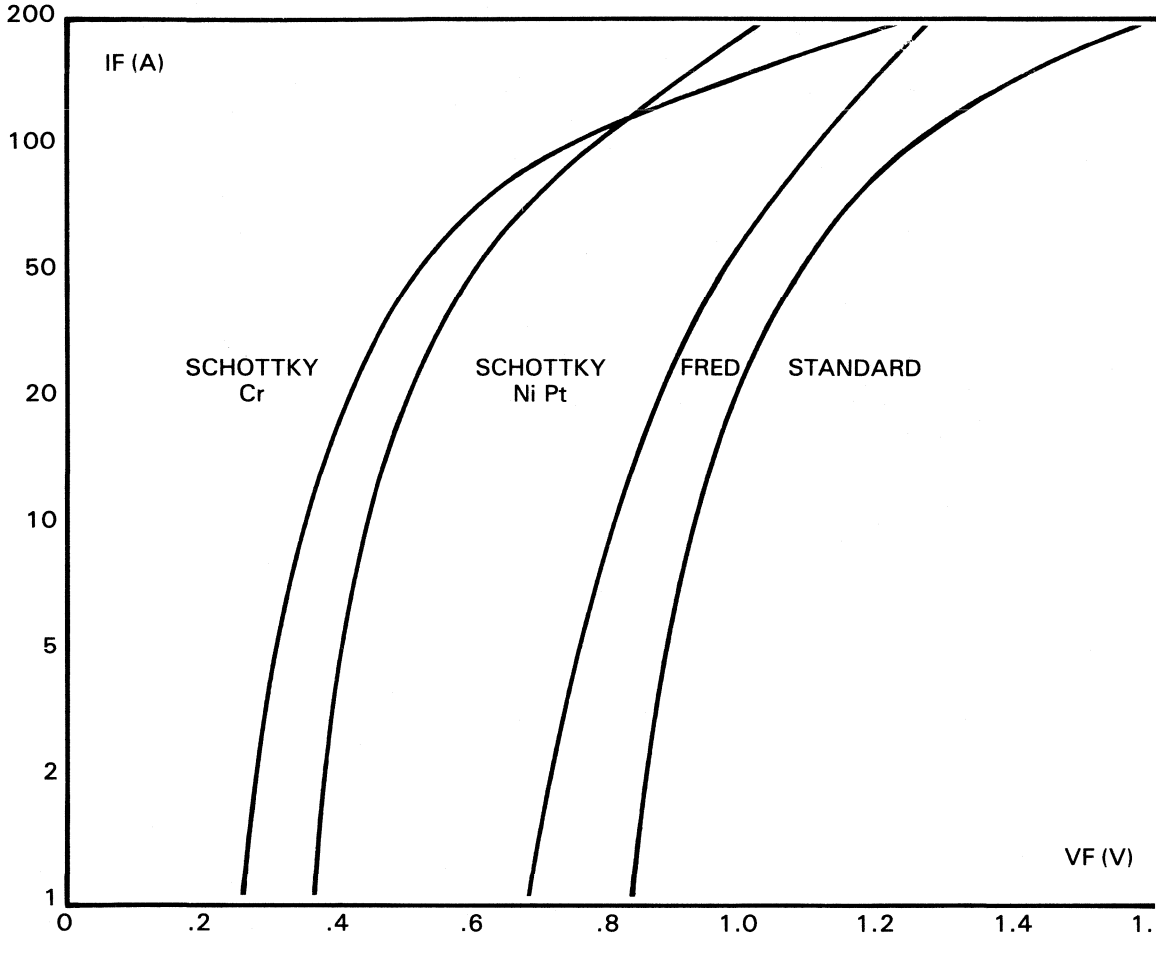


FIGURE 4: COMPARISON OF FORWARD VOLTAGE DROP FOR DIFFERENT TECHNOLOGIES
(THESE CURVES REFERED TO THE DIE AREA A = .16 mil²)

A.III. REVERSE CHARACTERISTICS

The equation $J = Js \exp\left(\frac{qV}{KT} - 1\right)$ is the relationship for the reverse voltage voltage-current characteristic.

For $V < 4\frac{KT}{q} = 0.1\ V$ 25°C, the inverse current is less than Js, but increases with V just to the point of the saturation current density, Js, at $V \geqslant 4\ KT/q$.

For $V > 4\frac{KT}{q}$, the applied reverse voltage provokes an increased electrical field at the metal – Si. This increase of electrical field lowers the potential barrier by an amount noted as $\Delta\ \varnothing B$, from which we inherit an increase in reverse current.

$$\Delta\ \varnothing B = \sqrt{\frac{qE}{4\pi\epsilon}}$$

and $$E = \sqrt{\frac{2q\ Nd\ VR}{\epsilon}}$$

where: Nd = concentration of impurities (donners) at/Cm^3
ϵ = dielectric constant 10^{-12} Farad/cm

There the reverse current density can be expressed as:

$$J_R = Js \exp \frac{q\ \Delta\ \varnothing B}{KT}$$

Example – for a dopage of Nd = 3 (10^{15}) at/cm^3

$$E = \sqrt{\frac{2 \times 1.6\ (10^{-19}) \times 3\ (10^{15})}{10^{-12}}} \times \sqrt{VR}$$

$$E = 3\ (10^4) \sqrt{VR}$$

and $$\Delta \varnothing B = \frac{1.6\,(10^{-19}) \times 3\,(10^{4})}{4\,\pi\,(10^{-12})} \times \sqrt[4]{VR}$$

$$\Delta \varnothing B = 0.019 \sqrt[4]{VR}$$

To retrieve the value of IR at VR = 5 V

$$\Delta \varnothing B = 0.019 \sqrt[4]{5} = 0.02\ V$$

$$JR = Js \exp \frac{q \Delta \varnothing B}{KT}$$

$$= Js \exp 28/26$$

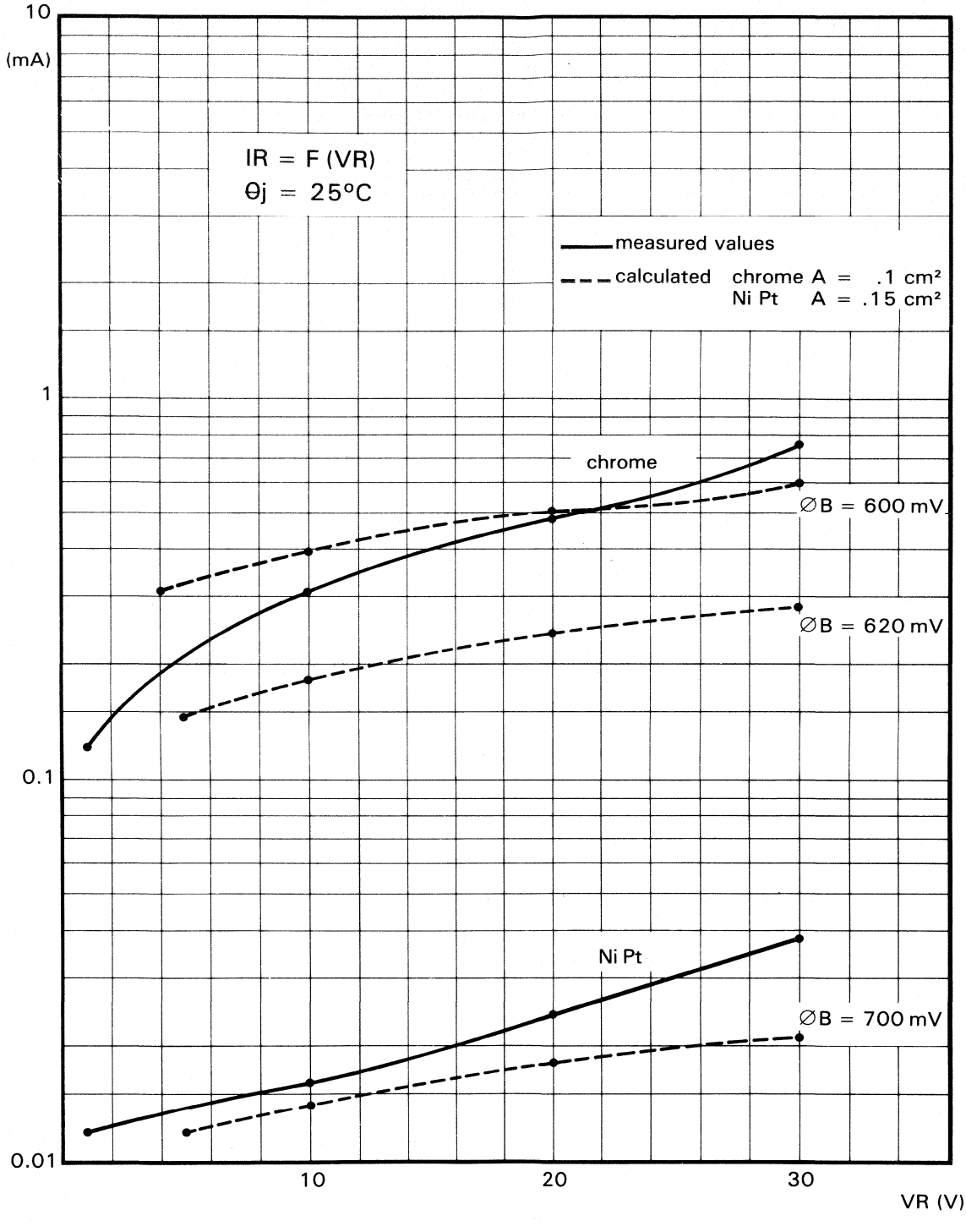
$$JR = 2.96\ Js$$

The table belows shows the results for other values of VR using these equations:

VR	5 V	10 V	20 V	30 V
JR	2.96 Js	3.64 Js	4.65 Js	5.48 Js

In practice, because of imperfections in the metal – Si interface and other side effects, the distribution of electric field is not the same over the entire surface. There are areas where barrier heights are decreased and the current density is higher. This results in actual IR current to be 2 to 10 times the theorical current.

Curve 5 permits the comparison of theorical and actual measured values of IR as a function of VR for both the chrome and the Ni Pt schottky.


10
(mA)
IR = F (VR)
θj = 25°C
measured values
calculated chrome A = .1 cm²
Ni Pt A = .15 cm²
1
chrome
∅B = 600 mV
∅B = 620 mV
0.1
Ni Pt
∅B = 700 mV
0.01
10
20
30
VR (V)

CURVE 4

A.IV. TEMPERATURE INFLUENCES

a) **Variation in VF as a function of temperature**

$$VF = \varnothing B + \frac{KT}{q} \text{Ln} \frac{JF}{RT^2}$$

$$VF = \varnothing B - \frac{KT}{q} \text{Ln } RT^2 + \frac{KT}{q} \text{Ln JF (mA)}$$

$$VF = \varnothing B - A + U \text{ Ln JF (mA)}$$

Where A and U are given in the table below:

θ°C	25	50	75	100	125	150
A(mV)	600	656	709	765	819	876
U(mV)	26	28.2	30.3	32.5	34.6	36.8

For JF = 100 mA/cm² the Δ VF = 45 mV/°C
1 A/cm² 40 mV/°C
10 A/cm² 35 mV/°C
100 A/cm² 30 mV/°C

b) **Variation of JS with temperature**

$$Js = RT^2 \exp \frac{-q \varnothing B}{KT}$$

$$Js = B \exp \frac{-\varnothing B}{U}$$

θ°C	25	50	75	100	125	150
B 10^7A	1.08	1.27	1.47	1.69	1.92	2.17
U(mV)	26.0	28.2	30.3	32.5	34.6	36.8

In the particular cases of Cr and Ni Pt, Js is found to be:

TABLE A

θ°C / Js(mA)	25	50	75	100	125	150
Cr ∅B = 600 mV	1.0	7.3	37	162	565	1800
NiPt ∅B = 700 mV	.022	.021	1.41	7.5	31.0	119

c) **Variation of Js with temperature**

$$JR = Js \exp \frac{q \Delta \varnothing B}{KT}$$

The table below gives the value for the multiplier coefficient

$M = \exp \frac{q \Delta \varnothing B}{KT}$ as a function of VR and temperature.

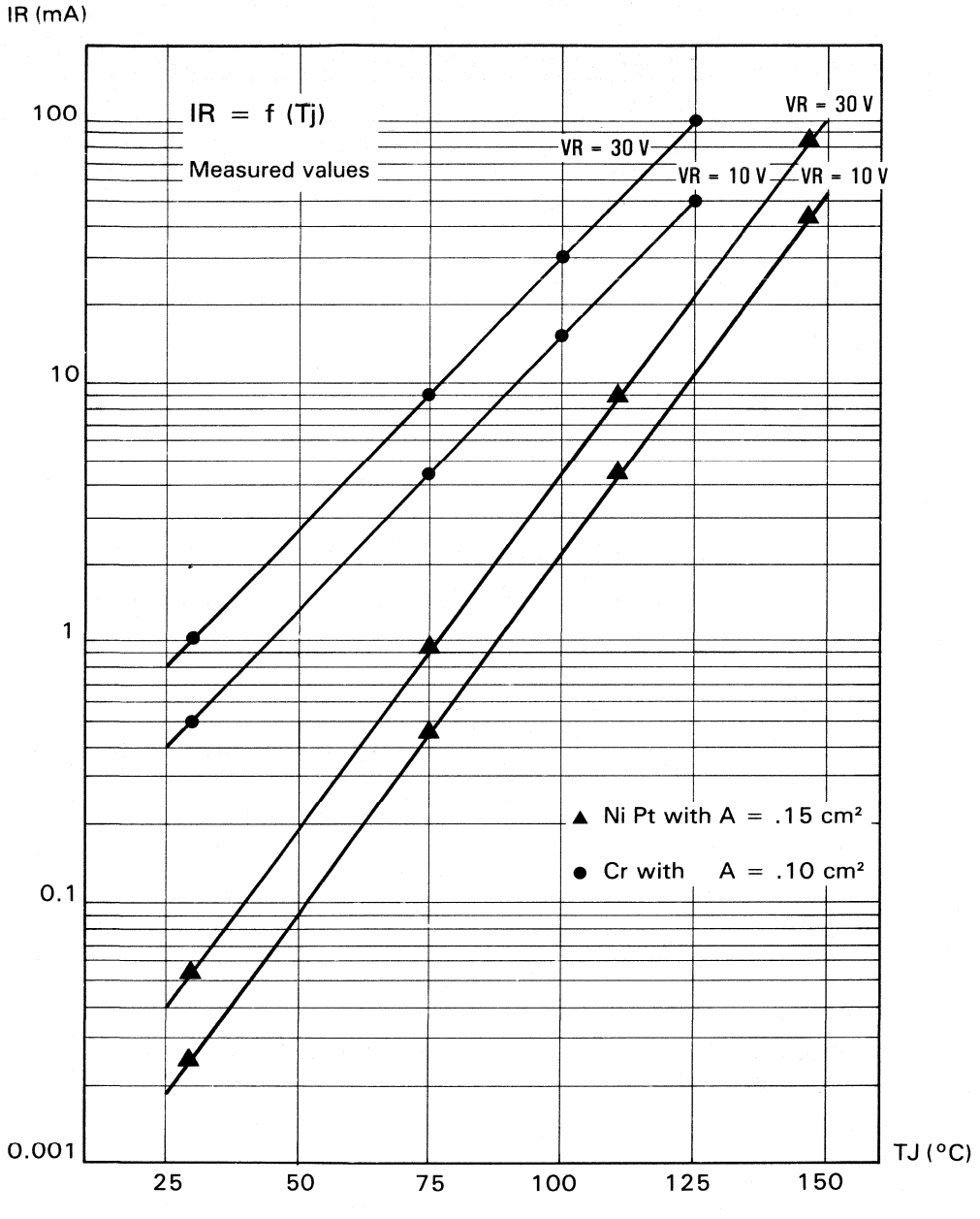
TABLE B

θ°C / VR	25	50	75	100	125	150
5 V	2.96	2.72	2.54	2.38	2.26	2.15
10 V	3.64	3.29	3.03	2.81	2.64	2.49
20 V	4.65	4.12	3.74	3.42	3.17	2.96
30 V	5.48	4.80	4.30	3.90	3.59	3.32

To calculate the effective IR find Js from TABLE A and the multiplier coefficient M given in table B

$$JR = M \times Js$$

Actual reverse current for MOTOROLA devices are shown on curve 6 as a function of temperature for Cr and Ni Pt.

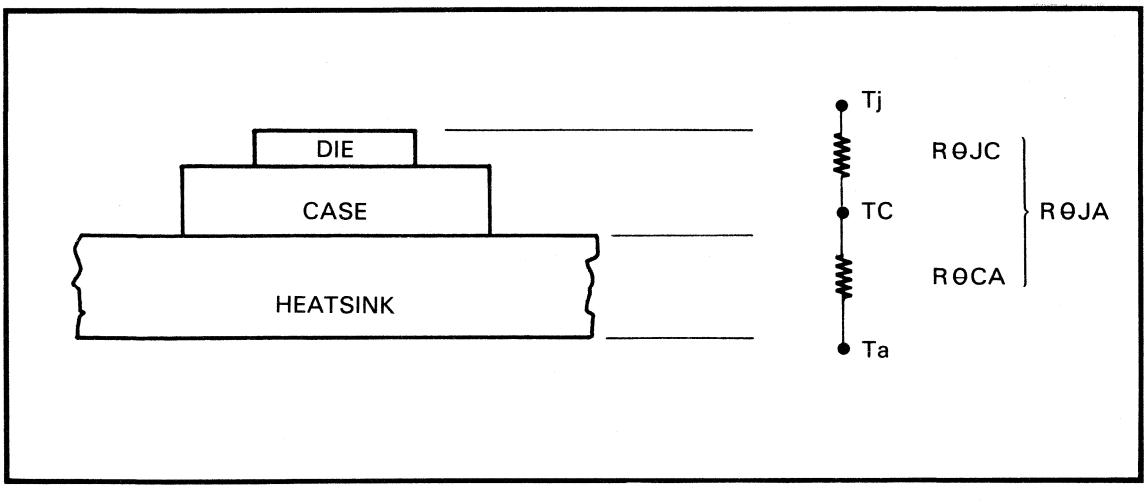

IR (mA)
100
10
1
0.1
0.001
IR = f (Tj)
Measured values
VR = 30 V
VR = 10 V
VR = 30 V
VR = 10 V
▲ Ni Pt with A = .15 cm²
● Cr with A = .10 cm²
25
50
75
100
125
150
TJ (°C)

CURVE 5

A.V. SCHOTTKY DIODES THERMAL STABILITY

A power rectifier is a thermal system where it's important to know the stability limits. This system is considered by:

- the heat source: the silicium die,
- the heat dissipation components: case and heatsink,
- the environment where the temperature is supposed constant: Ta



Stability Conditions

Power evacuated outside must be equals to the dissipated power in the die, then thermal stability equation is:

$$\frac{Tj - Ta}{R_{\theta JA}} = PF + PR\,(Tj)$$

With PF = dissipated power in forward conduction (quite independent of Tj)

PR = dissipated power in reverse (it is a function of Tj)

The condition of thermal stability is:

$$\frac{d\,PR\,(Tj)}{d\,Tj} < \frac{1}{R_{\theta}}$$

Stability Limit

In a diode, reverse current variation with the temperature must be represented in first approximation by the equation:

$$IR = I_1 \exp C\,Tj$$

Then we have

$$PR = VR \times I_1 \exp C\,Tj$$

And $$\frac{d\,PR}{d\,Tj} = C\,PR$$

And at the stability limit:

$$C\,PRm = \frac{1}{R_{\theta JA}}$$

At the stability limit, the value of the reverse current will be:

$$IRm = \frac{1}{C\, R_{\theta JA}\, VR}$$

Maximal junction temperature will be:

$$Tjm = \frac{1}{C} \, Ln \, \frac{IRm}{I_1}$$

And the maximal ambient temperature:

$$Tam = Tjm - PF\, R_{\theta} - \frac{1}{C}$$

For each value of Ta $<$ Tam, the diode will be thermally stable, the junction temperature value will be below Tjm and the leakage current IR lower than the limit value IRm.

For MOTOROLA diodes family, the value of C is quite constant ($\simeq$ 0.05), it is therefore interesting to notice the maximal value of admissible IR is directly determined by use conditions.

NOTE: when the solution θm we had is higher than θj max value, we must consider that $\theta m = \theta j$ max.

And then $\theta am = \theta j \text{ max} - R\theta\, VR\, IRm$

With $IRm = IR \text{ at } \theta = \theta j \text{ max}$

Example: for a mounting where the heatsink used is $R_{\theta JA} = 10°C/W$ and where the reverse voltage applied is VR = 30 V, the running maximum IR admissible will be:

$$IRm = \frac{1}{0.05 \times 10 \times 30} = 66 \text{ mA}$$

A measure of this current made on the functionning circuit in the worst conditions of charge and ambient temperature will allow to evaluate the security edge with regard to this limit.

In this same application, if we use a diode with Io = 0.3 mA (experimental measurement), the thermal stability limit temperatures will be:

$$Tj = \frac{1}{0.05} \text{ Ln } \frac{66}{0.3} = 108°C$$

$$Ta \text{ max} = 88°C - PF \times 10$$

If forward dissipated power is PF = 2 Watts, the maximum ambient temperature will be:

$$Ta \text{ max} = 68°C$$

Use of Data Sheets

MOTOROLA data sheets give directly the graphic solution of the stability limit calculations that we just made.

Generally the running diode is not submitted to a continue reverse voltage but to a square or sinusoïdal signal. The reverse voltage which must be consider is the equivalent VR voltage:

$$VR \text{ equi} = VR \text{ peak} \times F$$

The parameter F to use is given in the data sheets.

Therefore the average forward dissipated power value PF must be evaluated taking into account the average current value IF (AV) and the form of the signal.

The set of curves presented in the data sheets allow to determine the ambient temperature Tam in two steps:

1. From VR and $R\theta$, evaluation of the parameter.

2. From TR and PF, determine Tam value.

A.VI. MOTOROLA'S DEVICE FAMILY AND QUALITY/ RELIABILITY PROGRAM

MOTOROLA offers a wide range of schottky products ranging from 1 A plastic packages to the powerfull 75 A DO-5 with possibilities in chrome or Ni Pt, depending on the package / current requirement, with voltage ranges to 40, 50 Volts VR.

A high volume production is achieved by integrating a Quality Control monitoring at each step of operation. Long term reliability is assured by a continuous Line Audit program with life test including mechanical, thermal and electrical stresses.

SCHOTTKY POWER RECTIFIERS

CHROME BARRIER

- 125°C TJ
- BEST VF
- HIGH IR

1 A and 3 A Plastic Axial	5 A / AXIAL Tin Can	15 A / DO4	25 A / DO4	40 A / DO5
• 1 A: 1N5817/19	• MBR320M/40M	• MBR1520/40	• MBR 2520/40	• MBR4020/40
• 3 A: 1N5820/22	• 1N5823/25	• 1N5826/28	• 1N5829/31	• 1N5832/34
	• BYS05-20/40	• BYS16-20/40	• BYS25-20/40	• BYS40-20/40

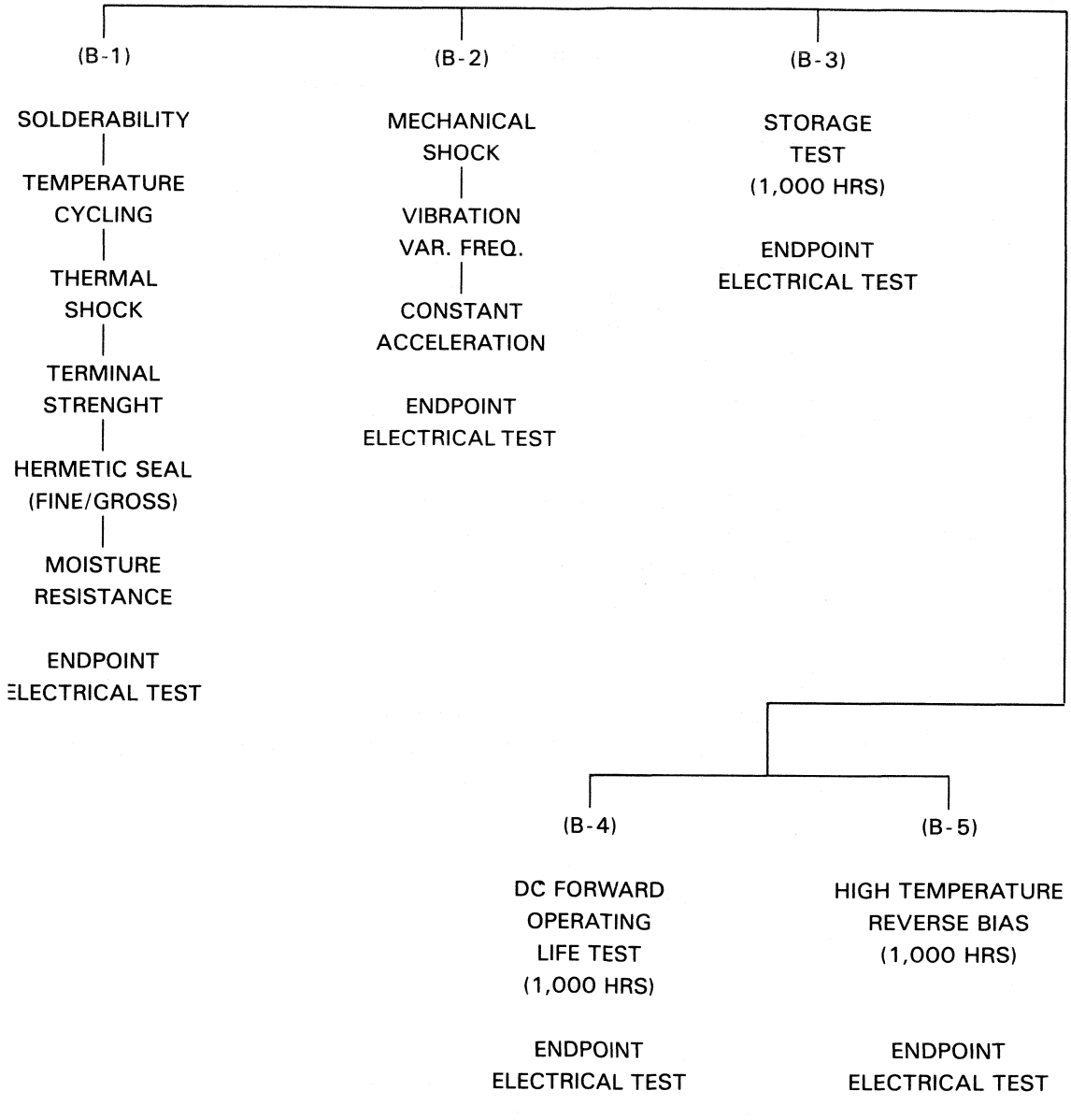
SCHOTTKY POWER RECTIFIERS

NICKEL / PLATINIUM BARRIER

- **150°C TJ**
- **LOW IR**
- **BETTER VF**

35 A / DO4	60 A / DO5	75 A / DO5
• MBR3520/50	• MBR6020/50	• MBR7520/50
• SD41	• SD51	• BYS75-20/50
• 1N6095/96	• 1N6097/98	
• BYS35-20/50	• BYS60-20/50	

RELIABILITY QUALIFICATION



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  April 18, 1977

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  IEEE Trans. Electron. devices vol ED-17, n° 9
  September 1970

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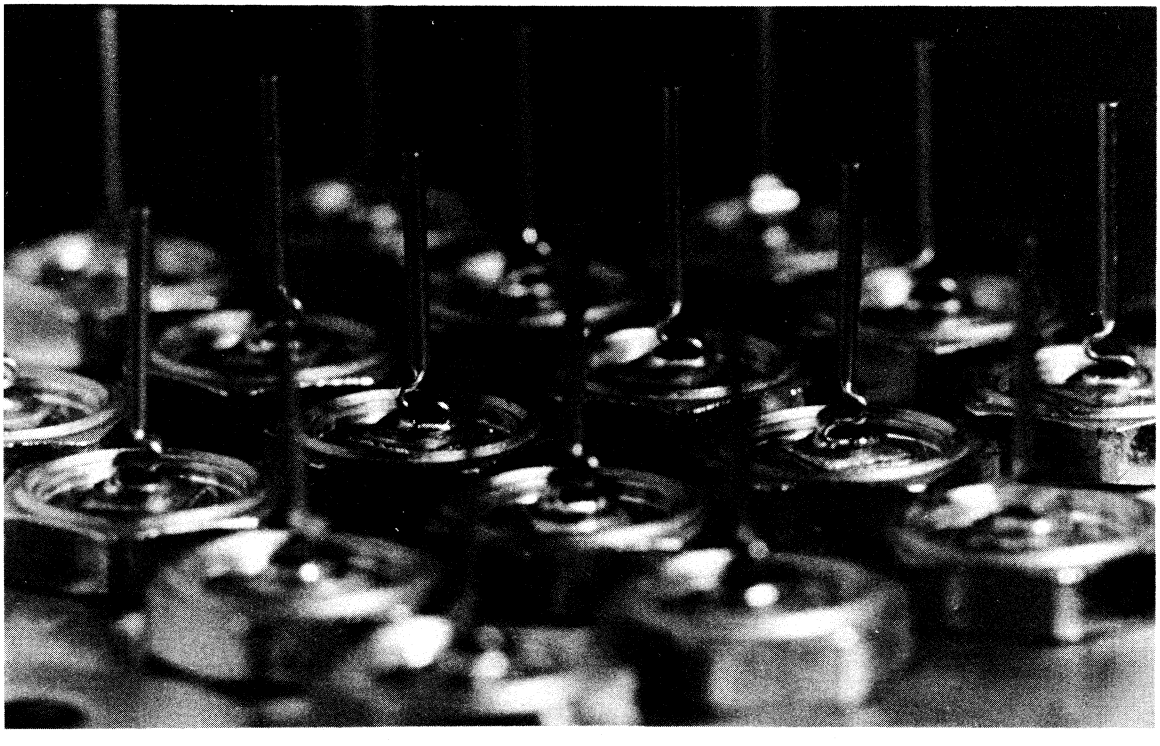


B.I. USE OF SCHOTTKY DIODES IN THE SWITCHMODE POWER SUPPLY

Us of schottky diodes in the continue to continue converter of a switching power supply allows:

- To decrease forward and switching power losses. Heatsinks used will be smaller, design of power supply will be more compact and the operating temperature lower.

- To decrease the stresses applied on the switching transistor and then to have a better reliability from the whole.

The subject of this study is to determine the operating conditions of the diodes used in the main configurations generally required in:

- Flyback converter

- Forward converter

The full knowledge of these conditions will allow the choice of an optimal product among our schottky diode family.

B.II. FLYBACK CONVERTER

In this type of converter (see diagram in figure 1), the power is accumulated in the primary of the transformer when the transistor is under conduction. The power is transfered to the load thru the diode D which becomes conductive when the transistor is blocked.

Figure 2 gives the diagram of voltages and currents as a function of time.

II.I. Forward Current in the Diode

The average current in the rectifying diode IF (AV) is equal to the current Io provided to the load. However the instantaneous value of the current IF (t) can reach a maximum value relatively high (IF max) that is important to estimate.

We must have $IF(AV) = Io$

And then on one period $T\,Io = \int_0^T IF(t)\,dt$

The diagram of the current IF (figure 2) allow to write:

$$T\,Io = \frac{T - \zeta}{2}\,(IF\,max + IF\,min)$$

Then $$IF\,max = \frac{2T}{\zeta - T}\,Io - IF\,min$$

Using $$\frac{\zeta}{T} = \delta$$

We have $$IF\,max = \frac{2\,Io}{\delta max - 1} - IF\,min$$

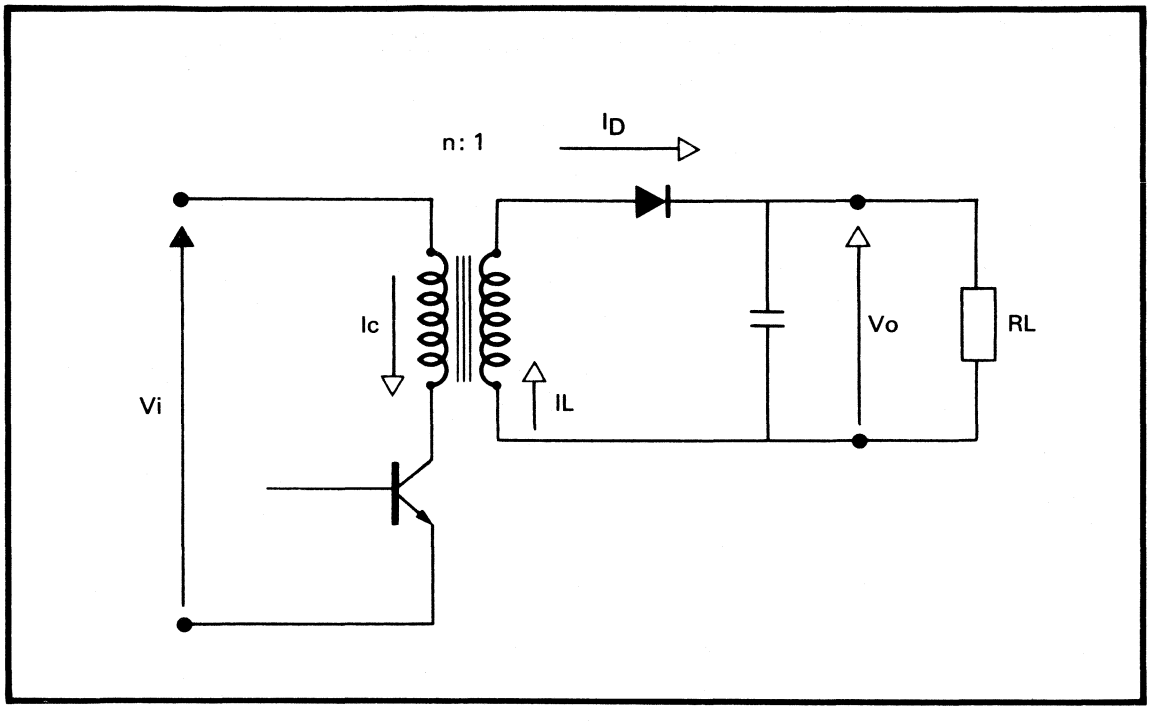


FIGURE 1: FLYBACK CONVERTER DIAGRAM

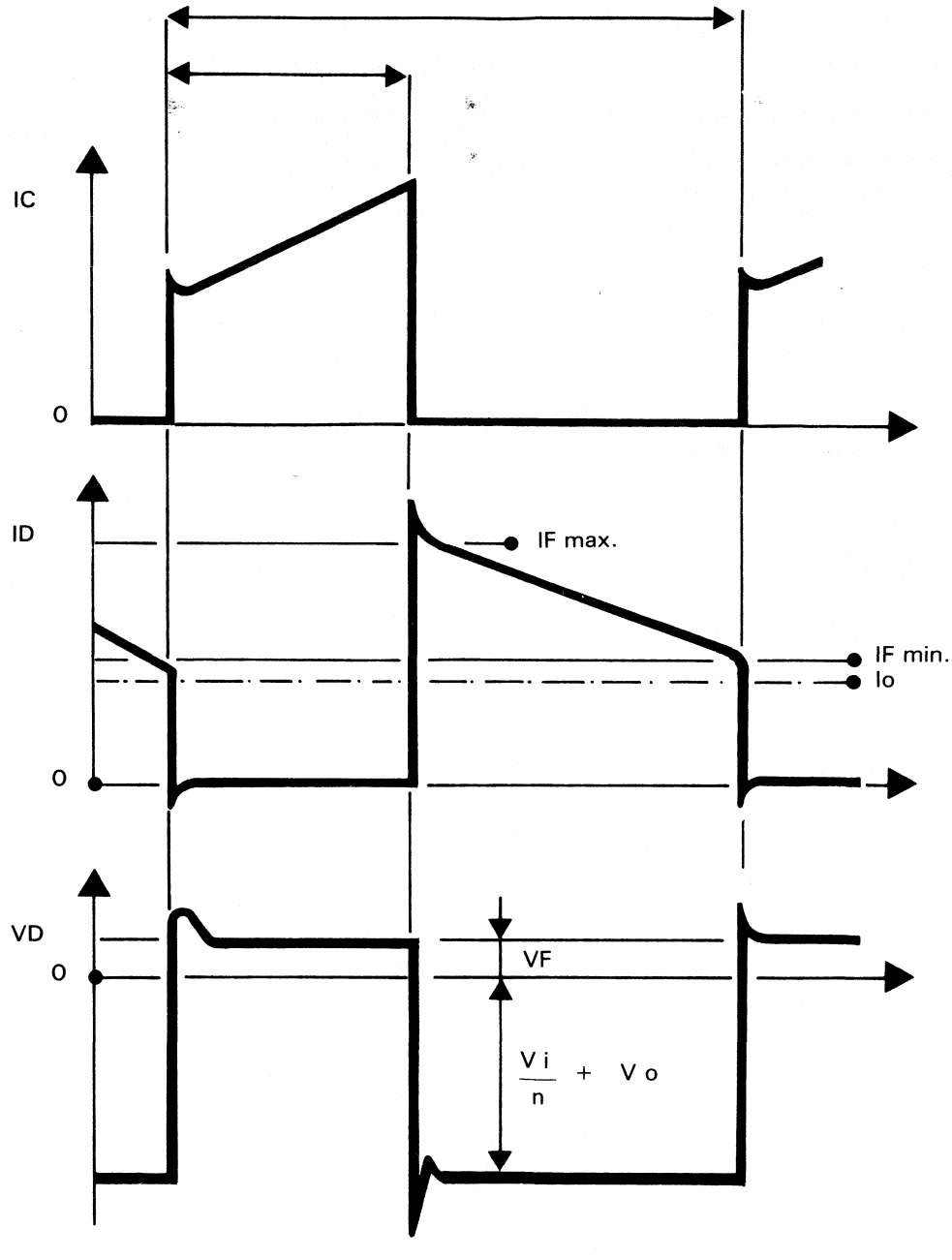


FIGURE 2: VOLTAGES AND CURRENTS DIAGRAM IN A FLYBACK CONVERTER

In the most unfavourable conditions IF min = 0 and for a maximum value of $\delta = 0.6$, we can therefore reach:

$$IF\ max = 5\ Io$$

In a Flyback converter, the rectifying diode will have to show a low direct voltage drop (VF) and must admit current peaks five times the average current delivered by the power supply.

II.2. Reverse Voltage

As showed in diagram figure 2, maximum voltage applied between the connections of the rectifying diode is:

$$VR = \frac{Vi}{n} + Vo$$

With $$Vo = \frac{1}{n} \frac{\delta}{1 - \delta} (Vi - Vp)$$

Then $$VR\ max = \frac{Vo}{\delta min} - Vp \frac{1 - \delta min}{\delta min}$$

Vp is the voltage loss thru the converter (resistive losses and diode VF).

One generally chooses a diode with VRRM equals to $\frac{Vo}{\delta min}$ plus 20% in order to take care of loss and peak voltages at the switching point.

B.III. FORWARD CONVERTER

In this type of converter (figure 3) power is directly transfered to the load through the diode D1 and the self Lo when the transistor is on.

When the transistor is blocked, power stocked in Lo at the previous phase, is transfered to the load by the free wheel diode D2.

Figure 4 gives the diagram of currents ID 1 and ID 2.

III.1. Direct Currents in D 1 and D 2 Diodes

a) ESTIMATED AMPLITUDE OF CURRENT PEAK IF MAX

The average current which passes thru Lo is equal to the Io current delivered by the power supply.

For a period T, we can write:

$$T\,Io = \int_0^T I_2(t)\,dt$$

$$T\,Io = \frac{T}{2}(IF\,max + IF\,min)$$

$$Io = \frac{1}{2}(IF\,max + IF\,min)$$

$$IF\,max = 2\,Io - IL\,min$$

For the limit conditions when IF min = 0, we therefore reach the maximum value:

$$IF\,max = 2\,Io$$

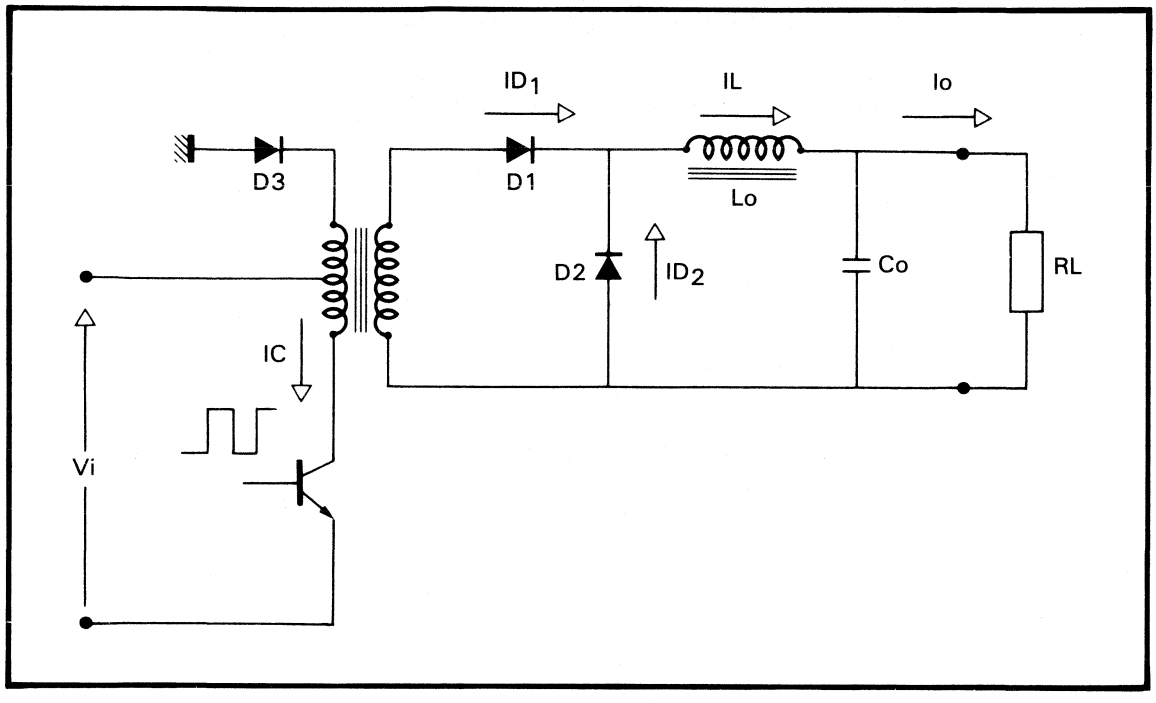


FIGURE 3: FORWARD CONVERTER DIAGRAM

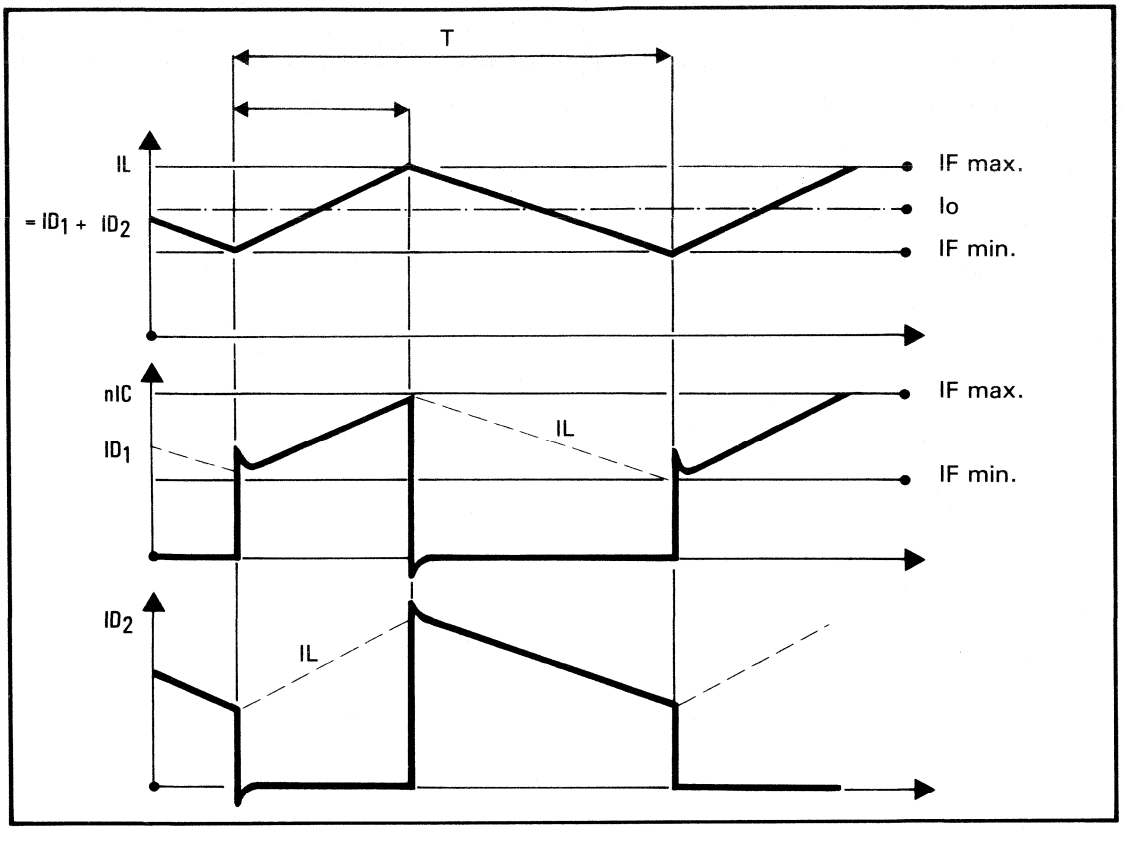


FIGURE 4: CURRENTS DIAGRAM IN A FORWARD CONVERTER

b) AVERAGE CURRENT IF (AV)

For the rectifying diode D1, on the T period:

$$T\ IF_1\ (AV) = \int_0^T IF\ (t)\ dt$$

$$T\ IF_1\ (AV) = \frac{\zeta}{2}\ (IF\ min + IF\ max)$$

$$T\ IF_1\ (AV) = \zeta\ Io$$

$$T\ IF_1\ (AV) = \frac{\zeta}{T}\ Io$$

$$IF_1\ (AV) = \delta D1\ Io$$

For the free wheel diode D2 the same calculation gives:

$$IF_2\ (AV) = \delta D2\ Io$$

III.2. Reverse Voltage

As in Flyback converter (see § II.2.) D1 and D2 diodes will have to hold:

$$VRRM \geqslant \frac{Vo}{\delta min} + 20\%$$

B. IV. CHOICE OF A DIODE/THERMAL STABILITY CONDITION

For determining the size for the diodes required, we must take into account:

- Maximum value of reverse voltage VRRM.
- Average value of direct current IF (AV) and its repetitive peak IF max value.

With this first choice done, it is important to verify the thermal stability conditions which will determine the maximum ambient temperature required for reliable operation of the device (see § A.V.).

As described on all MOTOROLA data sheets, thermal stability conditions take into account:

- Reverse power dissipation
- Forward power dissipation

IV.1. Reverse Dissipation

From the maximum value of VR (t), it is convenient to calculate an equivalent continuous reverse voltage VR (equi) which would give the same dissipation.

We must therefore have, on a T period:

$$VR\,(equi) \times IR\,(equi) \times T = VRM \times IRM \times (T - \quad)$$

Making the approximation IR = K VR (very unfavourable case) it is possible to write:

$$VR^2\,(equi) \times K \times T = VRM^2 \times K \times (T - \quad)$$

And then $VR\,(equi) = VRM - \sqrt{1 - \delta D}$

IV.2. Forward Dissipation

Direct current is a rectangular signal of maximum amplitude equal to IFM and of an average value IF (AV).

$$IFM = \frac{IF\ (AV)}{\delta\ D}$$

Dissipated power is $PF\ (AV) = IFM \times Vfm \times \delta\ D$

And $PF\ (AV) = IF\ (AV) \times VFM$

with VFM value of VF for $IF = \frac{IF\ (AV)}{\delta\ D}$

IV.3. Stability Conditions Verification

From the values found for VR (equi) and PF (AV), the set of curves given in MOTOROLA schottky diodes data sheets will allow to determine the maximum ambient operating temperature.

IV.4. Results Summary

	Flyback	Forward	
		Rectifying Diode D1	Free Wheel Diode D2
MAXIMAL REVERSE VOLTAGE VRRM	$\frac{Vo}{\delta\ min} + 20\ \%$		
EQUIVALENT REVERSE VOLTAGE VR (equi)	$VRRM \times \sqrt{\delta\ min}$	$VRRM \sqrt{1 - \delta min}$	$VRRM \times \sqrt{\delta\ min}$
MAXIMAL REPETITIVE FORWARD CURRENT IF max	5 Io	2 Io	2 Io
AVERAGE FORWARD CURRENT	Io	$Io \times \delta\ max$	$Io \times (1 - \delta\ min)$
AVERAGE FORWARD DISSIPATION PF (AV)	$PF\ (AV) = IF\ (AV) \times VFM$ with VFM = VF at $IF = \frac{IF\ (AV)}{1 - \delta\ max}$	$\frac{IF\ (AV)}{1 - \delta\ min}$	$\frac{IF\ (AV)}{1 - \delta\ max}$

B.V. USE EXAMPLES

V.1. Flyback converter = 5 V / 5 A

Assume a converter with:

δ min = 0.37
δ max = 0.50

Then the table in § IV.4. gives:

VRRM = 16.0 Volts
VR (equi) = 9.7 Volts
IFM = 25 A
IF (AV) = 5 A

One must use a product 15 A, 30 V: BYS 16-30

PF (AV) = 5 – (VF à 10 A)
= **2 Watts**

A heatsink with $R_{\theta JA}$ = 20° C/W is sufficient enough. The data sheet gives TR = 105° C, and the maximum ambien operating temperature will be:

$$TA = TR - PF\ (AV) \times R_{\theta JA} = 65°\,C$$

V.2. Flyback converter = 5 V / 12 A

Assume a converter with:

δ min = 0.35
δ max = 0.50

Then the table in § IV.4. allows to calculate the following parameters:

VRRM = 17 Volts
VR (equi) = 10 Volts

$$IFM = 60\ A$$
$$IF\ (AV) = 12\ A$$

With a relatively **high** value of VR (equi) **voltage** we must choose a 30 V product of Ni PT serie: BYS 35-30, and then:

$$PF\ (AV) = 12 \times (VF \text{ at } 24\ A)$$
$$= 6\ Watts$$

We will choose a heatsink with a total thermal resistivity $R_{\theta JA} = 10°\,C/W$. BYS 35-30 data sheet therefore gives the reference temperature $TR = 130°\,C$, and the maximum ambient temperature:

$$TA = TR - PF\ (AV) \times R_{\theta JA} = 64°\,C$$

V.3. Forward converter = 5 V / 40 A

If the converter is such that:

$$\delta \text{ min} = 0.35$$
$$\delta \text{ max} = 0.50$$

Table (§ IV.4.) allows to determine the main parameters of use for rectifying and free wheeling diodes.

	RECTIFIYING DIODE D1	**FREE WHEEL DIODE D2**
VRRM	17 V	17 V
VR (equi)	13 V	10 V
IF max	80 A	80 A
IF (AV)	20 A	26 A

For rectifying and free wheeling diodes, we will prefer a BYS 60-30 product.

Direct supply power will be:

$$PF\ (AV)\ D1 = 20 \times (VF \text{ at } 57\ A) = 11.0\ W$$
$$PF\ (AV)\ D2 = 26 \times (VF \text{ at } 52\ A) = 13.5\ W$$

With a heatsink of $R_{\theta JA} = 5°\ C/W$ for each diode the operating temperature will be lower than 62° C.

.VI. SCOPE OF USE

From the product characteristics given by the data sheet and use conditions (see § IV.4.) it is possible to determine for each diode a scope of use.

Figure 5 defines these scopes in the particular case of a 5 V power supply, as a function of the power delivered by the supply.

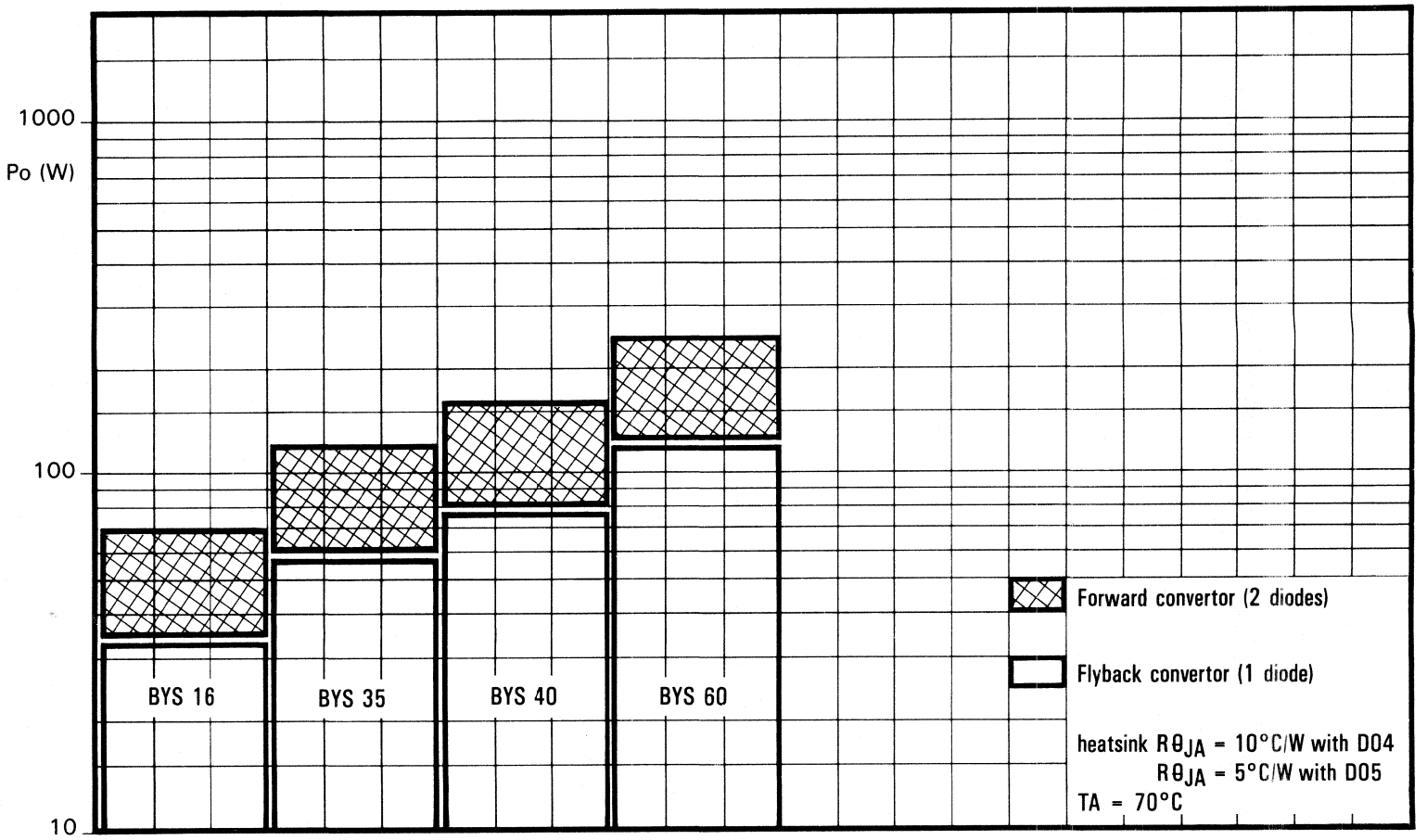
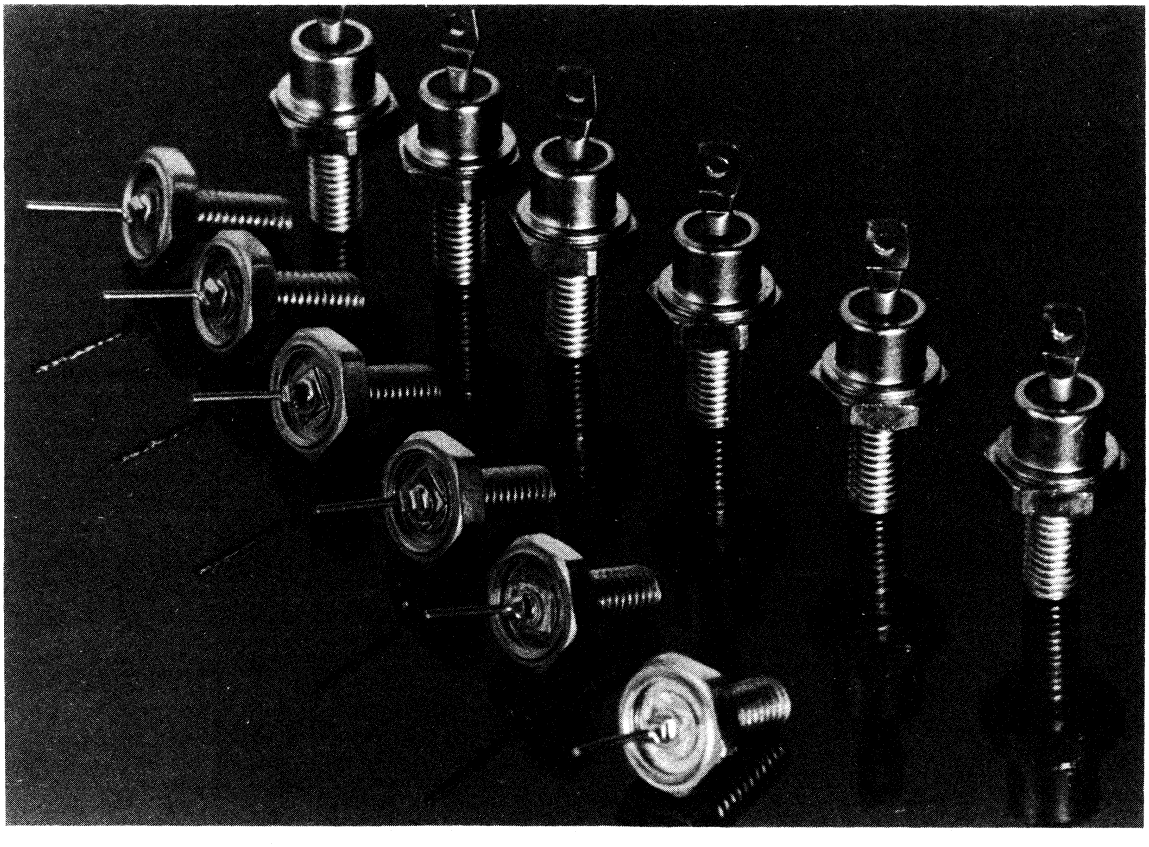


FIGURE 5: PARTICULAR CASE OF A POWER SUPPLY Vo = 5 V
CHOICE OF A DIODE TYPE FUNCTION OF THE POWER DELIVERED



MOTOROLA SWITCHMODE™ RECTIFIERS FOR SWITCHING POWER SUPPLIES

Total Supply Power	Typical Circuit	Input Rectifiers				Output Rectifiers							
		Standard Recovery for Line Voltage Operation				Schottky for 5 V Outputs				Fast Recovery For > 5 V Outputs			
		Input Current	Suggested Devices			Output Current	Suggested Devices			Output Current	Suggested Devices		
			Type	I_O	V_R		Type	I_O	V_R		Type	I_O	V_R
10 W	FLYBACK	< 1 A	1N4004 MDA104A MDA920A6	1 A 1 A 1.5 A	400 V 400 V 400 V	1-2 A	1N5821 MBR 330 M 1N5824 BYS 05-30 BYS 16-30	3 A 3 A 5 A 5 A 16 A	30 V 30 V 30 V 30 V 30 V	<½ A	1N4934	1 A	100 V
50 W		1 A	1N4004 MDA104A MDA920A6	1 A 1 A 1.5 A	400 V 400 V 400 V	5-10 A	1N5827 BYS 16-30 MBR 2530 BYS 25-30	15 A 16 A 25 A 25 A	30 V 30 V 30 V 30 V	½-1-½ A	1N4934 MR851 MR831 MR801	1 A 1 A 3 A 3 A	100 V 100 V 100 V 100 V
75 W		2 A	MR504 1N5404 MDA204	3 A 3 A 2 A	400 V 400 V 400 V	10-15 A	1N5830 MBR 3535 BYS 35-30 BYS 40-30	25 A 35 A 35 A 40 A	30 V 35 V 30 V 30 V	1-½-2-½ A	MR851 MR821 MR831 MR801	3 A 5 A 3 A 3 A	100 V 100 V 100 V 100 V
75 W	FORWARD	2 A	MR504 1N5404 MDA204	3 A 3 A 2 A	400 V 400 V 400 V	8-16 A	MBR 1530 BYS 16-30 1N5830 BYS 25-30 MBR 3035 CT	15 A 16 A 25 A 25 A 30 A	30 V 30 V 30 V 30 V 35 V	2--2-½ A	1N4934 MR851 MR801	1 A 3 A 3 A	100 V 100 V 100 V
100 W		3 A	MR504 1N5404 MDA970A5	3 A 3 A 4 A	400 V 400 V 400 V	10-20 A	1N5827 BYS 16-30 1N5830 BYS 35-30 MBR 3035 CT	15 A 16 A 25 A 35 A 30 A	30 V 30 V 30 V 30 V 35 V	2--2-½ A	1N4934 MR851 MR801	1 A 3 A 3 A	100 V 100 V 100 V
250 W		6 A	MR754 1N1204,A,B,C MR1124 MDS804	6 A 12 A 12 A 8 A	400 V 400 V 400 V 400 V	30-50 A	MBR 3535 MBR 3535 CT BYS 35-30 BYS 60-30	35 A 30 A 35 A 60 A	35 V 35 V 30 V 30 V	2-8 A	1N4934 MR851 MR821 1N3880 A MDA2501FR	1 A 3 A 5 A 6 A 25 A	100 V 100 V 100 V 100 V 100 V
1000 W	HALF BRIDGE	12 A	1N1204,A,B,C MR1124 MDA1204 MR2004S	12 A 12 A 12 A 20 A	400 V 400 V 400 V 400 V	200 A	MBR6035 BYS 60-30 BYS 75-30 (IN PARALLEL)	60 A 60 A 75 A	35 V 30 V 30 V	40 A	1N3900 1N3910 MDA3501FR	20 A 30 A 35 A	100 V 100 V 100 V
2500 W		25 A	MDA2504 MDA3504 1N1183,A	25 A 35 A 40 A	400 V 400 V 400 V	500 A	MBR 6035 BYS 60-30 MBR 7535 BYS 75-30 (IN PARALLEL)	60 A 60 A 75 A 75 A	35 V 30 V 35 V 30 V	100 A	MR871	50 A	100 V

PART N°	MOTOROLA DIRECT REPLACEMENT	PART N°	MOTOROLA DIRECT REPLACEMENT
BYS 05-20	BYS 05-20	BYV 21-30	BYS 35-30
BYS 05-30	BYS 05-30	BYV 21-35	BYS 35-45
BYS 05-40	BYS 05-40	BYV 21-40	BYS 35-45
BYS 15	1 N 5828	BYV 21-45	BYS 35-45
BYS 16-20	BYS 16-20	MBR 120 P	MBR 120 P
BYS 16-30	BYS 16-30	MBR 130 P	MBR 130 P
BYS 16-40	BYS 16-40	MBR 135 P	MBR 135 P
BYS 25-20	BYS 25-20	MBR 140 P	MBR 140 P
BYS 25-30	BYS 25-30	MBRT 320 P	MBR 320 P
BYS 25-40	BYS 25-40	MBR 330 P	MBR 330 P
BYS 30	BYS 35-45	MBR 335 P	MBR 335 P
BYS 35-20	BYS 35-20	MBR 340 P	MBR 340 P
BYS 35-30	BYS 35-30	MBR 320 M	MBR 320 M
BYS 35-45	BYS 35-45	MBR 330 M	MBR 330 M
BYS 35-50	BYS 35-50	MBR 335 M	MBR 335 M
BYS 40-20	BYS 4020	MBR 340 M	MBR 340 M
BYS 40-30	BYS 40-30	MBR 1520	MBR 1520
BYS 40-40	BYS 40-40	MBR 1530	MBR 1530
BYS 50	BYS 60-45	MBR 1535	MBR 1535
BYS 60-20	BYS 6020	MBR 1540	MBR 1540
BYS 60-30	BYS 60-30	MBR 2520	MBR 2520
BYS 60-45	BYS 60-45	MBR 2530	MBR 2530
BYS 60-50	BYS 6050	MBR 2535	MBR 2535
BYS 75-20	BYS 75-20	MBR 2540	MBR 2540
BYS 75-30	BYS 75-30	MBR 3020 CT	MBR 3020 CT
BYS 75-45	BYS 75-45	MBR 3035 CT	MBR 3035 CT
BYS 75-50	BYS 75-50	MBR 3045 CT	MBR 3045 CT
BYV 10-20	1 N 5817	MBR 3520	MBR 3520
BYV 10-30	1 N 5818	MBR 3535	MBR 3535
BYV 10-40	1 N 5819	MBR 3540	MBR 3540

PART N°	MOTOROLA DIRECT REPLACEMENT	PART N°	MOTOROLA DIRECT REPLACEMENT
MBR 3545	MBR 3545	SSP 320	1 N 5823
MBR 3550	MBR 3550	SSP 330	1 N 5824
MBR 4020	MBR 4020	SSP 340	1 N 5825
MBR 4030	MBR 4030	SSP 810	1 N 5826
MBR 4040	MBR 4040	SSP 820	1 N 5826
MBR 6020	MBR 6020	SSP 830	1 N 5827
MBR 6035	MBR 6035	SSP 840	1 N 5828
MBR 6040	MBR 6040	SSP 1510	1 N 5826
MBR 6045	MBR 6045	SSP 1520	1 N 5826
MBR 6050	MBR 6050	SSP 1530	1 N 5827
MBR 7529	MBR 7520	SSP 1540	1 N 5828
MBR 7535	MBR 7535	SSP 1550	BYS 35-50
MBR 7540	MBR 7540	SSP 2010	1 N 5829
MBR 7545	MBR 7545	SSP 2020	1 N 5829
MBR 7550	MBR 7550	SSP 2030	1 N 5830
S 15 S 3	1 N 5827	SSP 2040	1 N 5831
S 15 S 4	1 N 5828	SSP 2050	BYS 35-50
S 30 S 3 A	BYS 35-30	SSP 3005	BYS 35-20
S 30 S 4 A	BYS 35-45	SSP 3010	BYS 35-20
S 60 S 3	BYS 60-30	SSP 3020	BYS 35-20
S 60 S 4	BYS 60-45	SSP 3040	BYS 35-45
SD 241	SD 241	SSP 3050	BYS 35-50
SD 31	BYS 35-50	USD 520	BYS 75-20
SD 32	BYS 35-45	USD 535	BYS 75-45
SD 41	SD 41	USD 545	BYS 75-45
SD 51	SD 51	VSK 120	1 N 5817
SD 71	BYS 75-50	VSK 130	1 N 5818
SD 72	BYS 75-45	VSK 140	1 N 5819
SD 75	BYS 75-45	VSK 320	1 N 5820
SSP 310	1 N 5823	VSK 330	1 N 5821

PART N°	MOTOROLA DIRECT REPLACEMENT	PART N°	MOTOROLA DIRECT REPLACEMENT
VSK 340	1 N 5822	1 N 5830	1 N 5830
VSK 520	1 N 5823	1 N 5831	1 N 5831
VSK 530	1 N 5824	1 N 5832	1 N 5832
VSK 540	1 N 5825	1 N 5833	1 N 5833
VSK 1520	1 N 5826	1 N 5834	1 N 5834
VSK 1530	1 N 5827	1 N 6095	1 N 6095
VSK 1540	1 N 5828	1 N 6096	1 N 6096
VSK 3020 S	BYS 35-20	1 N 6097	1 N 6097
VSK 3030 S	BYS 35-30	1 N 6098	1 N 6098
VSK 3040 S	BYS 35-45	21 FQ 030	BYS 35-30
VSK 4020	1 N 5832	21 FQ 045	BYS 35-45
VSK 4030	1 N 5833	40H Q 025	BYS 60-30
VSK 4040	1 N 5834	40H Q 030	BYS 60-30
VSK 3020 T	MBR 3020 CT	40H Q 035	BYS 60-45
VSK 3030 T	MBR 3035 CT	40H Q 040	BYS 60-45
VSK 3040 T	MBR 3045 CT	50H Q 010	BYS 60-20
1 N 5817	1 N 5817	50H Q 015	BYS 60-20
1 N 5818	1 N 5818	50H Q 020	BYS 60-20
1 N 5819	1 N 5819	50H Q 025	BYS 60-30
1 N 5820	1 N 5820	50H Q 030	BYS 60-30
1 N 5821	1 N 5821	51H Q 045	BYS 60-435
1 N 5822	1 N 5822	75H Q 030	BYS 75-30
1 N 5823	1 N 5823	75H Q 040	BYS 75-45
1 N 5824	1 N 5824	75H Q 045	BYS 75-45
1 N 5825	1 N 5825	30 Q H C 030	MBR 3035 CT
1 N 5826	1 N 5826	30 Q H C 045	MBR 3045 CT
1 N 5827	1 N 5827	80 SQ 030	1 N 5824
1 N 5828	1 N 5828	80 SQ 040	1 N 5825
1 N 5829	1 N 5829		

SECTION 5

DATA SHEETS

MOTOROLA Semiconductors

BYS 35 SERIES

ADVANCE INFORMATION

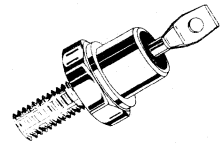
SWITCHMODE POWER RECTIFIERS

Epitaxial construction with oxyde passivation and metal overlap contact – ion implanted guard ring for transient voltage protection.

- lowest combinated power losses
- high surge capability
- majority carrier conduction

SCHOTTKY BARRIER RECTIFIERS

35 AMPERES – 30 TO 50 VOLTS



MAXIMUM RATINGS

Rating	Symbol	BYS35 –20	BYS35 –30	BYS35 –45	BYS35 –50	Units
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	45	50	Volts
Minimum Reverse Breakdown Voltage 10 mA, Tc = 25°C	V_{BR}	30	40	47	53	Volts
Average Rectified Forward Current Square Wave, V_r rated	$I_{F(av)}$	35 (Tc = 100°C)		35 (Tc = 90°C)		Amp
Non-Repetitive Peak Surge Current, 10 ms	I_{FSM}	600				Amp
Operating and Storage Temperature	T_j, T_{stg}	–65 to +150				°C
Peak Operating Junction Temperature	T_j (pk)	175				°C
Voltage Rate of Change	dV/dT	1000				Volts/ u sec

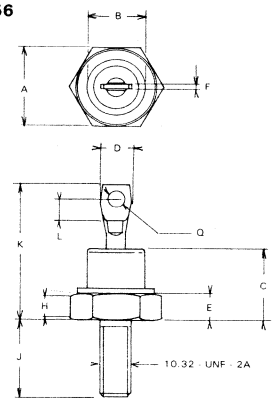
THERMAL CHARACTERISTICS

Characteristics	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	RθJC	1.2	1.5	°C/W

ELECTRICAL CHARACTERISTICS

Characteristics		Symbol	Typ	Max	Unit
Instantaneous Forward Voltage					
I_F = 35 Amp	T_C = 25°C		0.55	0.63	
	T_C = 100°C		0.48	0.60	
	T_C = 150°C		0.45	–	
I_F = 70 Amp	T_C = 25°C	V_F	0.70	0.80	Volts
	T_C = 100°C		0.62	0.77	
	T_C = 150°C		0.57	–	
Instantaneous Reverse Current, Rated V_R					
T_C = 25°C	BYS35 – 20/30		70	700	
	BYS35 – 45/50		100	1000	μA
T_C = 100°C	BYS35 – 20/30	I_R	8	15	
	BYS35 – 45/50		12	25	mA

CASE 56
DO-4



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.77	11.10	0.424	0.437
B				0.424
C	–	10.29		0.450
D			–	0.250
E	1.91	4.45	0.075	0.175
F	0.6	–	0.023	–
H	1.5	–	0.06	–
J	10.72	11.51	0.422	0.453
K	–	20.32	–	0.800
L	2.0	–	0.078	–
Q	1.5	–	0.060	

MECHANICAL CHARACTERISTICS

CASE: Welded, hermetically sealed
POLARITY: Cathode to Case
MOUNTING POSITION: Any
STUD TORQUE: 15 in. lb. Max

NOTE 1: DETERMINATING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runway must be considered when operating this rectifier at reverse voltages above $0.2V_{RWM}$. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA} P_{F(AV)} - R_{\theta JA} P_{R(AV)} \quad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature.

$T_{J(max)}$ = Maximum allowable junction temperature. (125°C or the temperature at which thermal runway occurs, whichever is lowest).

$P_{F(AV)}$ = Average forward power dissipation.

$P_{R(AV)}$ = Average reverse power dissipation.

$R_{\theta JA}$ = Junction-to-ambient thermal resistance.

Figure 1 permits easier use of equation (1) by taking reverse power dissipation and thermal runway into consideration. The figure solves for a reference temperature as determinated by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA} P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA} P_{F(AV)} \quad (3)$$

Inspections of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runway occurs or where $T_J = 150°C$ when forward power is zero.

The data of Figure 1 is based upon dc conditions. For use in common rectifiers circuits, Table 1 indicates suggested factors for an equivalent dc voltage to use for conservative design i.e.:

$$V_{R(equiv)} = V_{in\,(PK)} \times F \quad (4)$$

The factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

EXAMPLE:

Find $T_{A(max)}$ for BYS35-20 operated in a 12V dc power supply using a bridge circuit with capacitive filter such that I_{DC} 30amps ($I_{F(AV)}$ = 15amps), $I_{F(AV)}/I_{F(pk)} = \delta = 0.1$ input voltage = 11V(rms), $R_{\theta JA}$ = 5°C/Watt.

STEP 1: Find $V_{R(equiv)}$. Read F = 0.65 from Table 1. $V_{R(equiv)} = (11)(1.41)(0.65) = 10.1$ Volts.

STEP 2: Find T_R from Figure 1. Horizontally, intercept V_R = 10.1Volts with the BYS35-20 curve. Vertically intercept this point with the $R_{\theta JA}$ = 5°C/W curve. Read T_R directly. T_R = 138°C.

STEP 3: Find $P_{F(AV)}$ from Figure 3, Read $P_{F(AV)}$ = 12.6W. $I_{F(AV)} / I_{F(PK)} = \delta = 0.1$ and $I_{F(AV)}$ = 15 amps.

STEP 4: Find $T_{A(max)}$ from equation (3) – $T_{A(max)}$ = 138 – (12.6)(5) = 75°C.

TABLE 1 — VALUES FOR FACTOR F

Circuit Load	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped	
	Resistive	Capacitive	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

FIGURE 1 — MAXIMUM REFERENCE TEMPERATURE

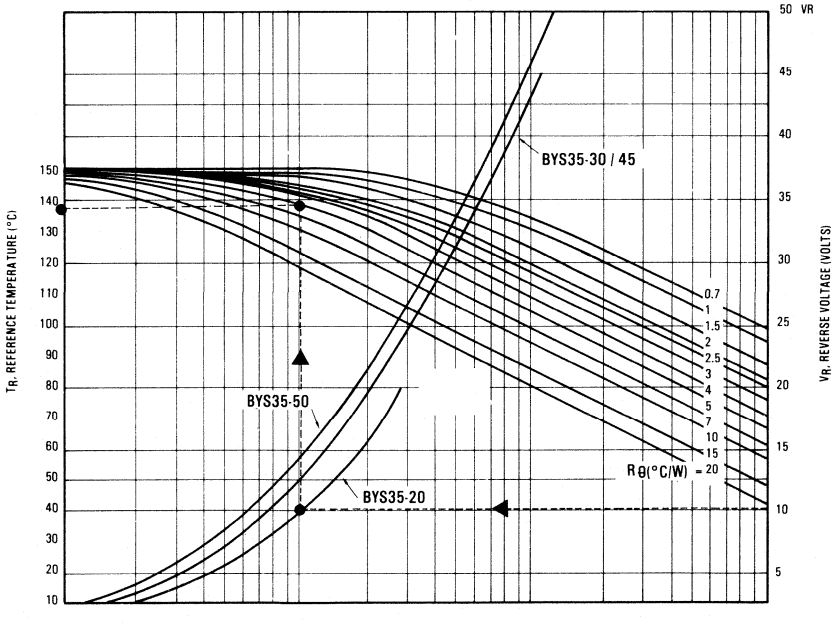


FIGURE 2 — TYPICAL FORWARD VOLTAGE

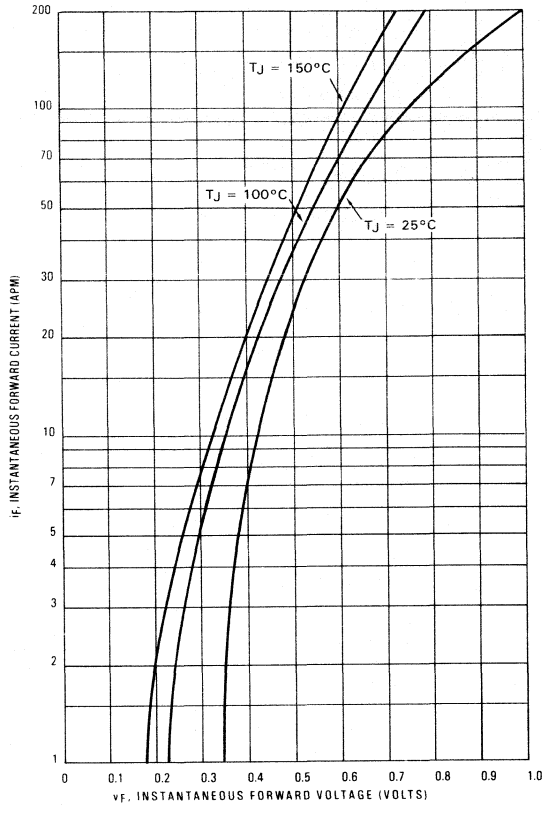


FIGURE 3 — MAXIMUM SURGE CAPABILITY

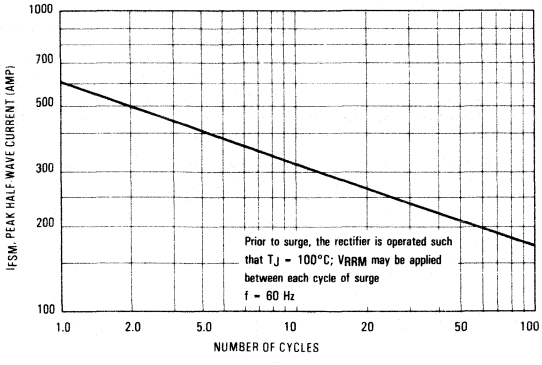


FIGURE 4 — FORWARD POWER DISSIPATION

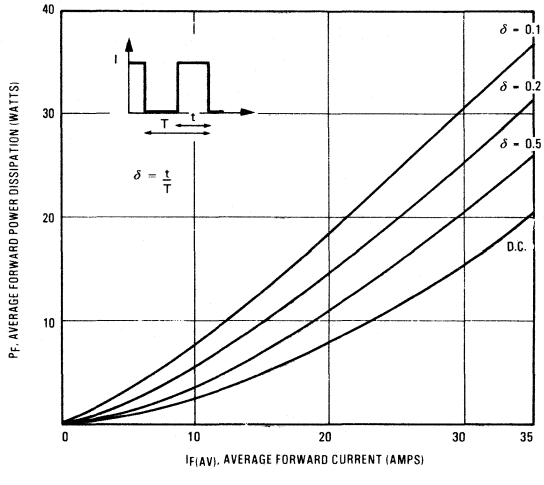


FIGURE 5 — THERMAL RESPONSE

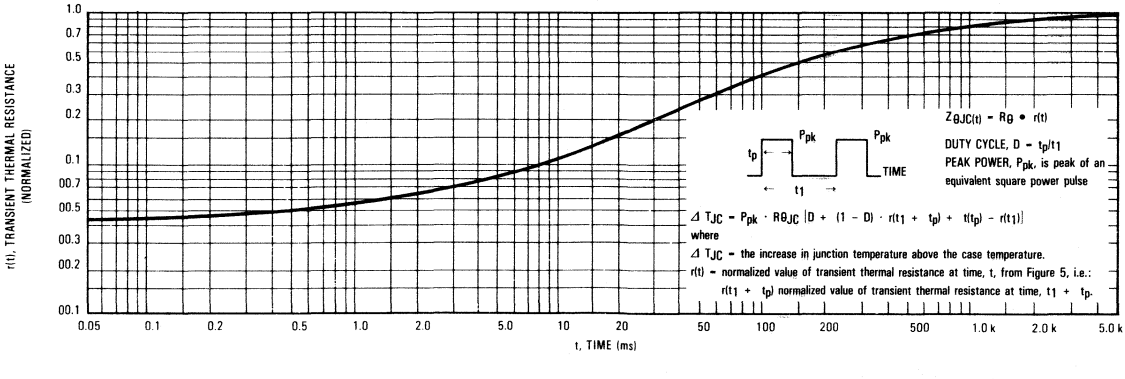


FIGURE 6 — CAPACITANCE

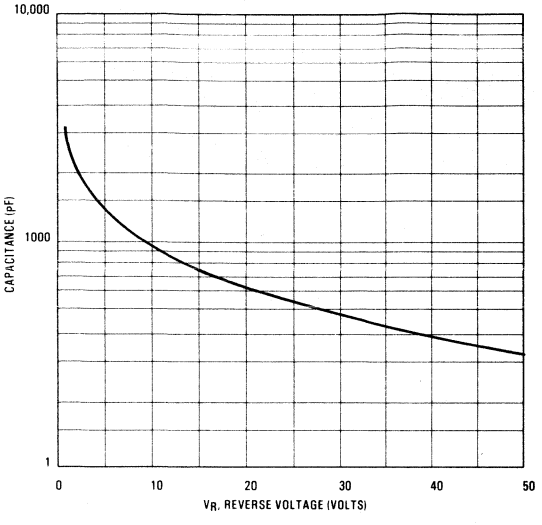
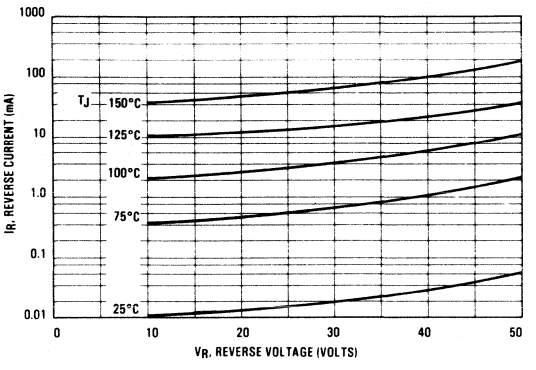


FIGURE 7 — TYPICAL REVERSE OPERATION



NOTE 2 HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 6).

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 per cent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, where as perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss; it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage.

MOTOROLA Semiconductors

BYS 60 SERIES

ADVANCE INFORMATION

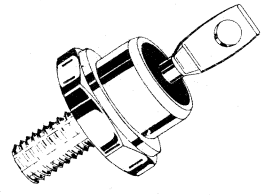
SWITCHMODE POWER RECTIFIERS

Epitaxial construction with oxyde passivation and metal overlap contact – ion implanted guard ring for transient voltage protection.

- lowest combinated power losses
- high surge capability
- majority carrier conduction

SCHOTTKY BARRIER RECTIFIERS

60 AMPERES – 30 TO 50 VOLTS



MAXIMUM RATINGS

Rating	Symbol	BYS60 -20	BYS60 -30	BYS60 -45	BYS60 -50	Units
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	45	50	Volts
Minimum Reverse Breakdown Voltage 10 mA, Tc = 25°C	V_{BR}	30	40	47	53	Volts
Average Rectified Forward Current Square Wave, V_r rated	$I_{F(av)}$	60 (Tc = 100°C)		60 (Tc = 90°C)		Amp
Non-Repetitive Peak Surge Current, 10 ms	I_{FSM}	800 (for 1 cycle)				Amp
Operating and Storage Temperature	T_j, T_{stg}	−65 to +150				°C
Peak Operating Junction Temperature	T_j (pk)	175				°C
Voltage Rate of Change	dV/dT	1000				Volts/ u sec

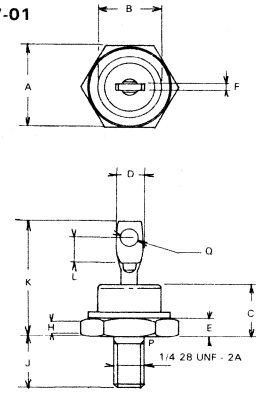
THERMAL CHARACTERISTICS

Characteristics	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	RΘjc	0.7	0.9	°C/W

ELECTRICAL CHARACTERISTICS

Characteristics		Symbol	Typ	Max	Unit
Instantaneous Forward Voltage					
I_F = 60 Amp	T_C = 25°C		0.65	0.70	
	T_C = 100°C		0.60	0.68	
	T_C = 150°C		0.55	–	
I_F = 120 Amp	T_C = 25°C	V_F	0.79	0.86	Volts
	T_C = 100°C		0.74	0.81	
	T_C = 150°C		0.68	–	
Instantaneous Reverse Current, Rated V_R					
T_C = 25°C	BYS60-20/30		70	700	
	BYS60-45/50		100	1000	μA
T_C = 100°C	BYS60-20/30	I_R	8	15	
	BYS60-45/50		12	25	mA

CASE 257-01
DO-5



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	16.94	17.45	0.667	0.687
B	–	16.94	–	0.667
C	–	11.43	–	0.450
D	–	9.53	–	0.375
E	2.92	5.08	0.115	0.200
F	–	2.03	–	0.080
H	1.52	–	0.060	–
J	10.72	11.51	0.422	0.453
K	–	25.40	–	1.000
L	3.86	–	0.152	–
P	5.59	6.32	0.220	0.249
Q	3.56	4.45	0.140	1.175

NOTE:
Dimension "P" is diameter.

MECHANICAL CHARACTERISTICS

CASE: welded, hermetically sealed
POLARITY: cathode to case
MOUNTING POSITION: any
STUD TORQUE: 25 in. lb. max

NOTE 1: DETERMINATING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runway must be considered when operating this rectifier at reverse voltages above $0.2V_{RWM}$. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA} P_{F(AV)} - R_{\theta JA} P_{R(AV)} \quad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature.

$T_{J(max)}$ = Maximum allowable junction temperature. (125°C or the temperature at which thermal runway occurs, whichever is lowest).

$P_{F(AV)}$ = Average forward power dissipation.

$P_{R(AV)}$ = Average reverse power dissipation.

$R_{\theta JA}$ = Junction-to-ambient thermal resistance.

Figure 1 permits easier use of equation (1) by taking reverse power dissipation and thermal runway into consideration. The figure solves for a reference temperature as determinated by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA} P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA} P_{F(AV)} \quad (3)$$

Inspections of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runway occurs or where T_J = 150°C when forward power is zero.

The data of Figure 1 is based upon dc conditions. For use in common rectifiers circuits, Table 1 indicates suggested factors for an equivalent dc voltage to use for conservative design i.e.:

$$V_{R(equiv)} = V_{in\,(PK)} \times F \quad (4)$$

The factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

EXAMPLE:

Find $T_{A(max)}$ for BYS60-20 operated in a 12V dc power supply using a bridge circuit with capacitive filter such that I_{DC}60amps ($I_{F(AV)}$ = 30amps), $I_{F(AV)}/I_{F(pk)} = \delta = 0.1$ input voltage = 11V(rms), $R_{\theta JA}$ = 3°C/Watt.

STEP 1: Find $V_{R(equiv)}$. Read F = 0.65 from Table 1. $V_{R(equiv)}$ = (11) (1.41) (0.65) = 10.1 Volts.

STEP 2: Find T_R from Figure 1. Horizontally, intercept V_R = 10.1Volts with the BYS60-20 curve. Vertically intercept this point with the $R_{\theta JA}$ = 3°C/W curve. Read T_R directly. T_R = 144°C.

STEP 3: Find $P_{F(AV)}$ from Figure 3, Read $P_{F(AV)}$ = 30 W. $I_{F(AV)} / I_{F(PK)} = \delta = 0.1$ and $I_{F(AV)}$ = 30 amps.

STEP 4: Find $T_{A(max)}$ from equation (3) – $T_{A(max)}$ = 144 – (30)(3) = 54°C.

TABLE 1 — VALUES FOR FACTOR F

Circuit Load	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped	
	Resistive	Capacitive	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

FIGURE 1 — MAXIMUM REFERENCE TEMPERATURE

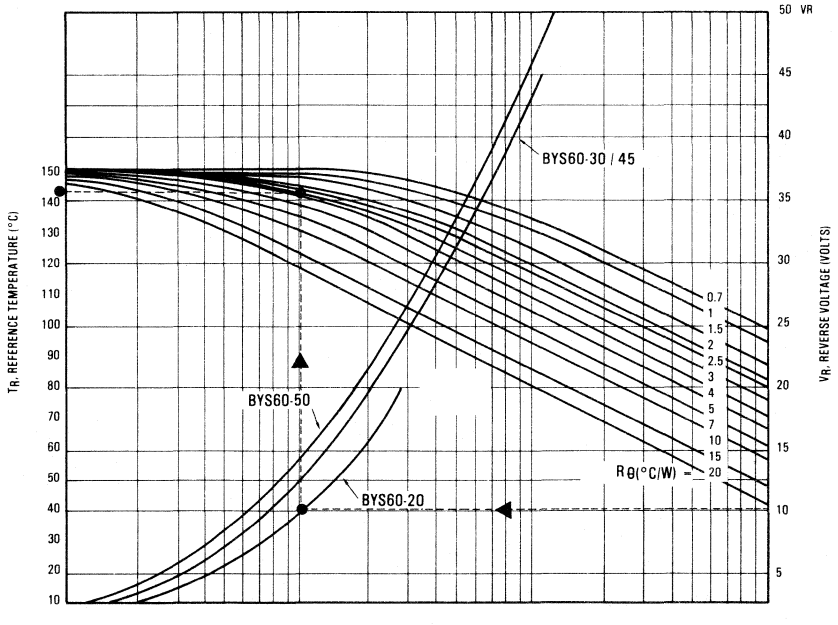


FIGURE 2 — TYPICAL FORWARD VOLTAGE

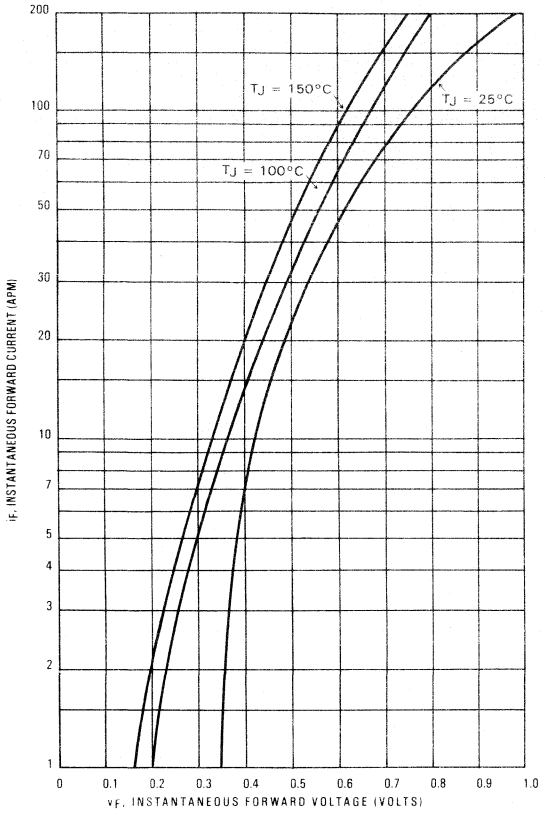


FIGURE 3 — MAXIMUM SURGE CAPABILITY

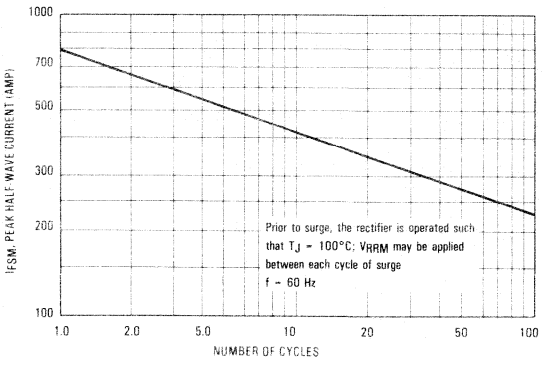


FIGURE 4 — FORWARD POWER DISSIPATION

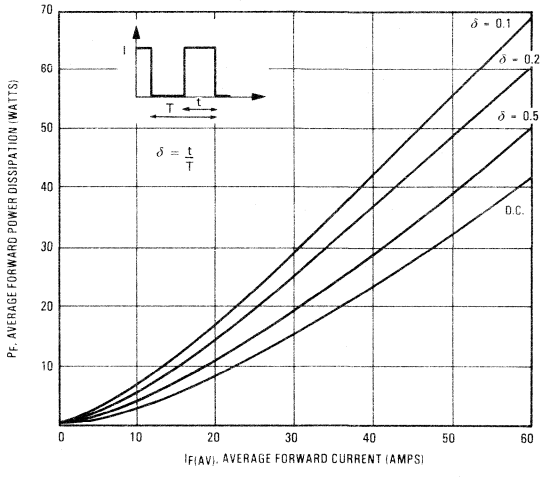


FIGURE 5 — THERMAL RESPONSE

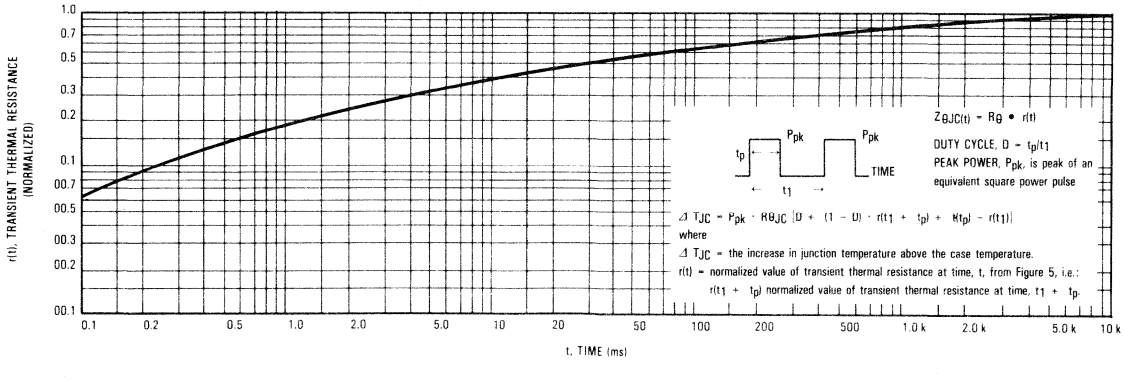


FIGURE 6 — CAPACITANCE

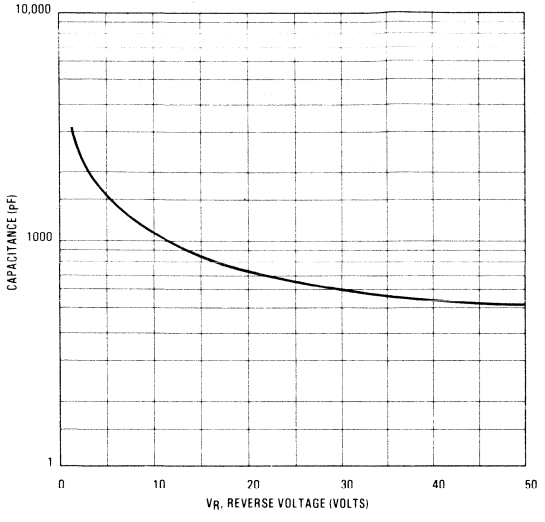
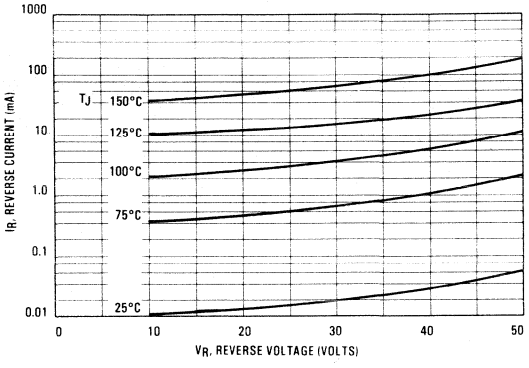


FIGURE 7 — TYPICAL REVERSE OPERATION



NOTE 2 HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 6).

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 per cent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, where as perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss; it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage.

MOTOROLA Semiconductors

BYS 75 SERIES

ADVANCE INFORMATION

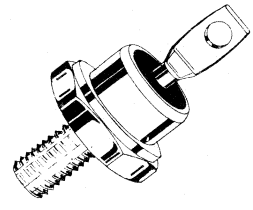
SWITCHMODE POWER RECTIFIERS

Epitaxial construction with oxyde passivation and metal overlap contact – ion implanted guard ring for transient voltage protection.

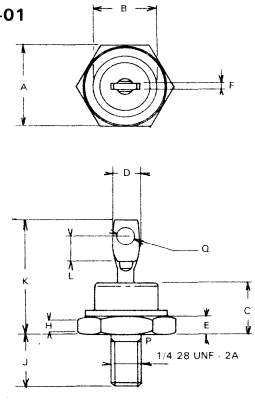
- lowest combinated power losses
- high surge capability
- majority carrier conduction

SCHOTTKY BARRIER RECTIFIERS

75 AMPERES – 30 TO 50 VOLTS



CASE 257-01
DO-5



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	16.94	17.45	0.667	0.687
B	–	16.94	–	0.667
C	–	11.43	–	0.450
D	–	9.53	–	0.375
E	2.92	5.08	0.115	0.200
F	–	2.03	–	0.080
H	1.52	–	0.060	–
J	10.72	11.51	0.422	0.453
K	–	25.40	–	1.000
L	3.86	–	0.152	–
P	5.59	6.32	0.220	0.249
Q	3.56	4.45	0.140	1.175

NOTE:
Dimension "P" is diameter.

MAXIMUM RATINGS

Rating	Symbol	BYS75 –20	BYS75 –30	BYS75 –45	BYS75 –50	Units
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	45	50	Volts
Minimum Reverse Breakdown Voltage 10 mA, Tc = 25°C	V_{BR}	30	40	47	53	Volts
Average Rectified Forward Current Square Wave, V_r rated	$I_{F(av)}$	75 (Tc = 100°C)		75 (Tc = 90°C)		Amp
Non-Repetitive Peak Surge Current, 10 ms	I_{FSM}	1000				Amp
Operating and Storage Temperature	T_j, T_{stg}	–65 to +150				°C
Peak Operating Junction Temperature	T_j (pk)	175				°C
Voltage Rate of Change	dV/dT	1000				Volts/ u sec

THERMAL CHARACTERISTICS

Characteristics	Symbol	Typ	Max	Unit
Thermal Resistance, Junction to Case	RθJC	0.6	0.75	°C/W

ELECTRICAL CHARACTERISTICS

Characteristics		Symbol	Typ	Max	Unit
Instantaneous Forward Voltage					
I_F = 75 Amp	T_C = 25°C		0.6	0.72	
	T_C = 100°C		0.55	0.64	
	T_C = 150°C		0.53	–	
I_F = 150 Amp	T_C = 25°C	V_F	0.8	0.88	Volts
	T_C = 100°C		0.68	0.78	
	T_C = 150°C		0.64	–	
Instantaneous Reverse Current, Rated V_R					
T_C = 25°C	BYS75–20/30		90	1000	
	BYS75–45/50		130	1200	μA
T_C = 100°C	BYS75–20/30	I_R	15	25	
	BYS75–45/50		40	50	mA

MECHANICAL CHARACTERISTICS

CASE: welded, hermetically sealed
POLARITY: cathode to case
MOUNTING POSITION: any
STUD TORQUE: 25 in. lb. max

NOTE 1: DETERMINATING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runway must be considered when operating this rectifier at reverse voltages above $0.2V_{RWM}$. Proper derating may be accomplished by use of equation (1):

$$T_{A(max)} = T_{J(max)} - R_{\theta JA} P_{F(AV)} - R_{\theta JA} P_{R(AV)} \quad (1)$$

where

$T_{A(max)}$ = Maximum allowable ambient temperature.

$T_{J(max)}$ = Maximum allowable junction temperature. (125°C or the temperature at which thermal runway occurs, whichever is lowest).

$P_{F(AV)}$ = Average forward power dissipation.

$P_{R(AV)}$ = Average reverse power dissipation.

$R_{\theta JA}$ = Junction-to-ambient thermal resistance.

Figure 1 permits easier use of equation (1) by taking reverse power dissipation and thermal runway into consideration. The figure solves for a reference temperature as determinated by equation (2):

$$T_R = T_{J(max)} - R_{\theta JA} P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA} P_{F(AV)} \quad (3)$$

Inspections of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runway occurs or where T_J = 150°C when forward power is zero.

The data of Figure 1 is based upon dc conditions. For use in common rectifiers circuits, Table 1 indicates suggested factors for an equivalent dc voltage to use for conservative design i.e.:

$$V_{R(equiv)} = V_{in\,(PK)} \times F \quad (4)$$

The factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

EXAMPLE:

Find $T_{A(max)}$ for BYS75-20 operated in a 12V dc power supply using a bridge circuit with capacitive filter such that I_{DC} 70amps ($I_{F(AV)}$ = 35amps), $I_{F(AV)}/I_{F(pk)} = \delta$ = 0.1 input voltage = 11V(rms), $R_{\theta JA}$ = 1.5°C/Watt.

STEP 1: Find $V_{R(equiv)}$. Read F = 0.65 from Table 1. $V_{R(equiv)}$ = (11) (1.41) (0.65) = 10.1 Volts.

STEP 2: Find T_R from Figure 1. Horizontally, intercept V_R = 10.1Volts with the BYS75-20 curve. Vertically intercept this point with the $R_{\theta JA}$ = 1.5°C/W curve. Read T_R directly. T_R = 142°C.

STEP 3: Find $P_{F(AV)}$ from Figure 3, Read $P_{F(AV)}$ = 33.5W. $I_{F(AV)} / I_{F(PK)} = \delta$ = 0.1 and $I_{F(AV)}$ = 35 amps.

STEP 4: Find $T_{A(max)}$ from equation (3) – $T_{A(max)}$ = 142 – (33.5)(1.5) = 92°C.

TABLE 1 – VALUES FOR FACTOR F

Circuit Load	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped (1), (2)	
	Resistive	Capacitive(1)	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

FIGURE 1 – MAXIMUM REFERENCE TEMPERATURE

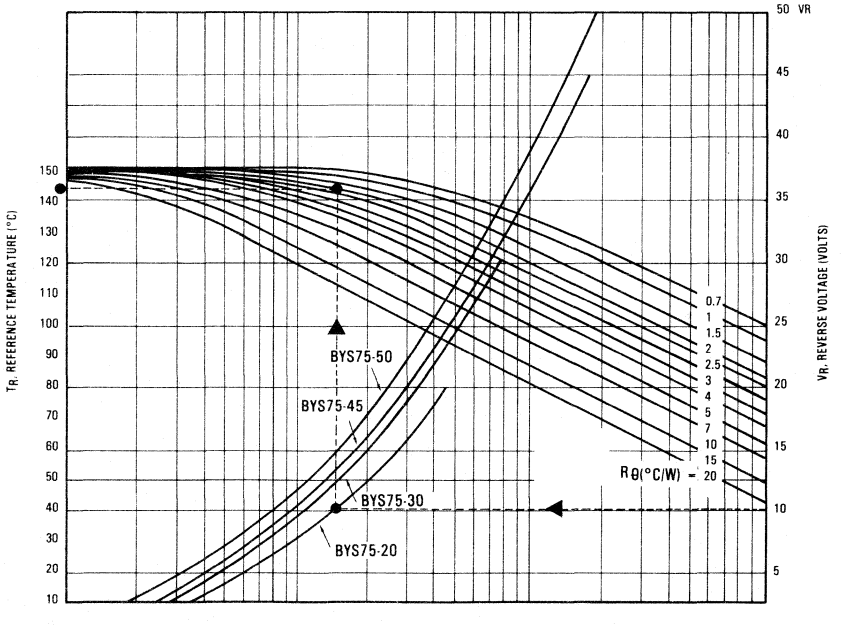


FIGURE 2 — TYPICAL FORWARD VOLTAGE

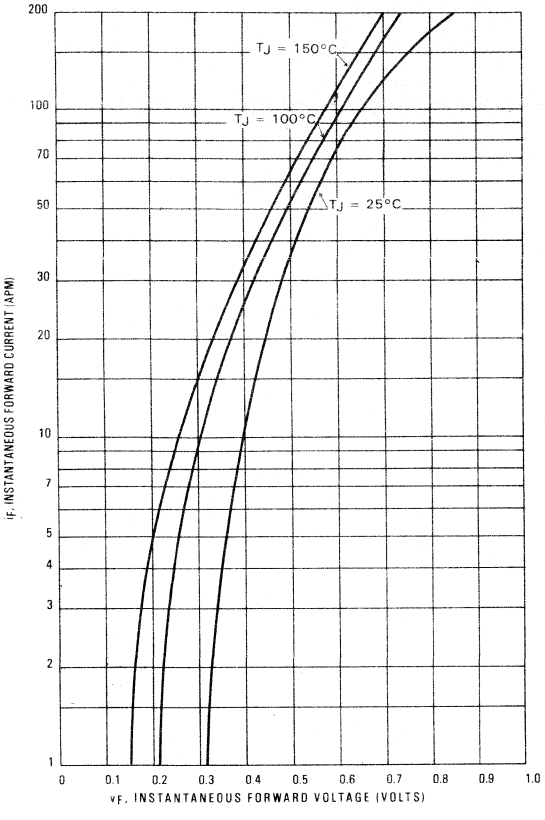


FIGURE 3 — MAXIMUM SURGE CAPABILITY

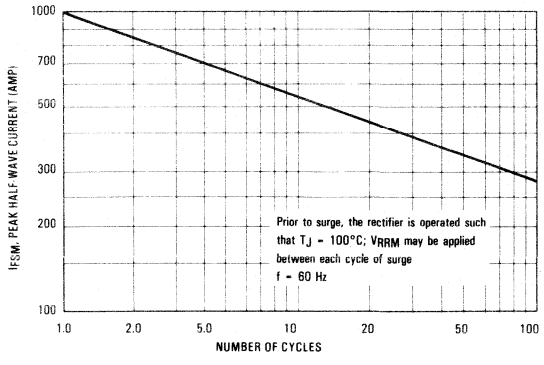


FIGURE 4 — FORWARD POWER DISSIPATION

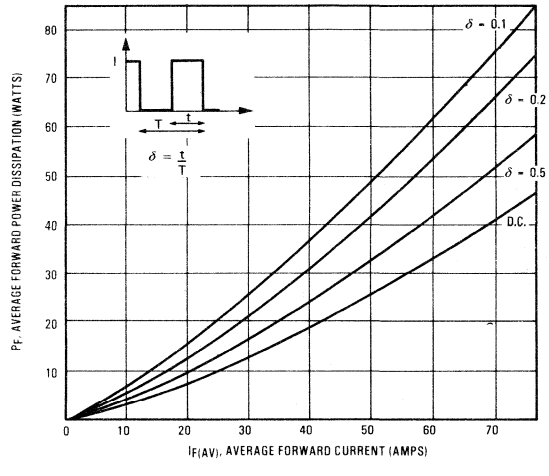


FIGURE 5 — THERMAL RESPONSE

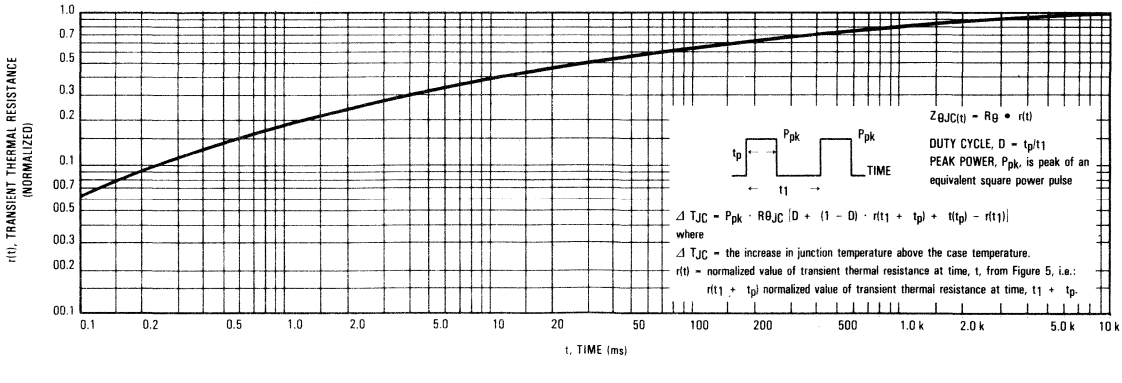


FIGURE 6 — CAPACITANCE

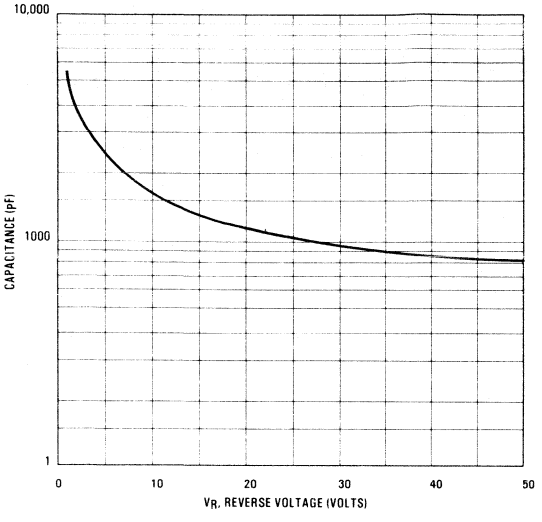
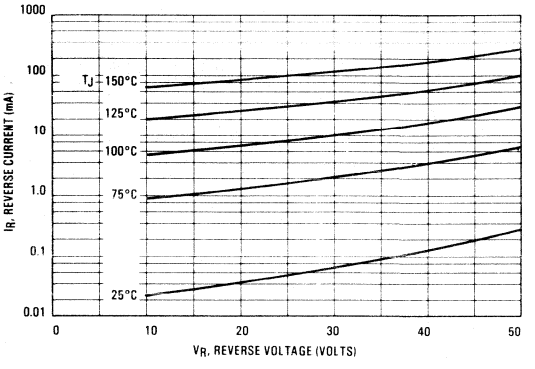


FIGURE 7 — TYPICAL REVERSE OPERATION



NOTE 2 HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 6).

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 per cent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, where as perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss; it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage.

MOTOROLA Semiconductors

MC3420
MC3520

SWITCHMODE REGULATOR CONTROL CIRCUIT

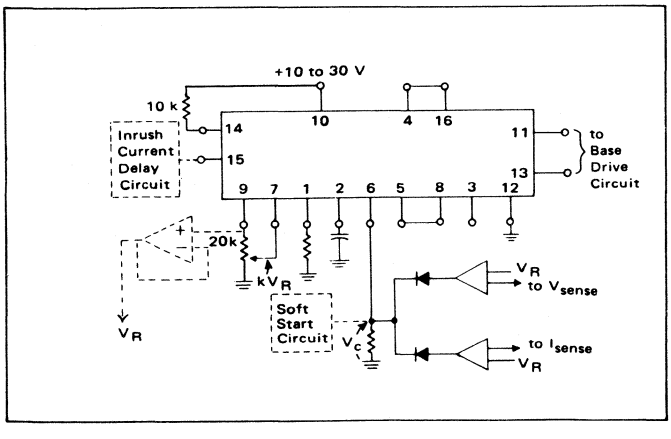
The MC3520/3420 is an inverter control unit which provides all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

These devices are designed to supply the pulse width modulated drive to the base of two external power transistors. Other applications where these devices can be used are in transformerless voltage doublers, transformer coupled dc-to-dc converters and other power control functions.

The MC3520 is specified over the military operating range of -55°C to +125°C. The MC3420 is specified from 0°C to +70°C.

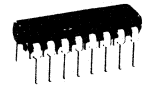
- Includes Symmetrical Oscillator
- On Chip Pulse Width Modulator, Voltage Reference, Dead Time Comparator, and Phase Splitter
- Output Frequency Adjustable (2 kHz to 100 kHz)
- Inhibit and Symmetry Correction Inputs Available
- Controlled Start-Up
- Frequency and Dead Time are Independently Adjustable (0% to 100%)
- Can be Slaved to Other MC3420s
- Open Collector Outputs
- Output Capability 50 mA (Max.)
- On Chip Protection Against Double Pulsing of Same Output During Load Transient Condition

FIGURE 1–TYPICAL APPLICATION

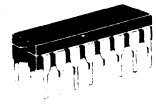


SWITCHMODE REGULATOR CONTROL CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUITS

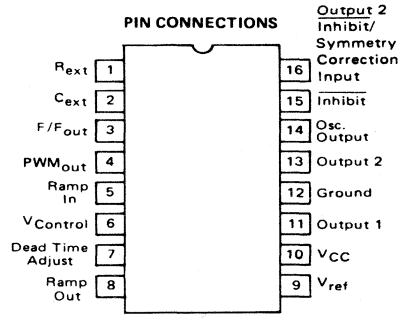


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3420P	0 to +70°C	Plastic DIP
MC3420L	0 to +70°C	Ceramic DIP
MC3520L	-55 to +125°C	Ceramic DIP

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DS 9424
(Replaces ADI-40

MAXIMUM RATINGS

Rating	Symbol	MC3520	MC3420	Unit
Power Supply Voltage	V_{CC}	30		V
Output Voltage (pins 11 and 13)	V_{out}	40		V
Oscillator Output Voltage (pin 14)	V_{14}	30		V
Voltage at pin 4	V_4	2.0		V
Voltage at pins 3 and 8	V_3, V_8	5.0		V
Voltage at pin 5	V_5	7.0		V
Power Dissipation	P_D	See Thermal Information		
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 – 150	 125 150	°C
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 to 30 V, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	MC3520 Min	MC3520 Typ	MC3520 Max	MC3420 Min	MC3420 Typ	MC3420 Max	Unit
REFERENCE SECTION									
Reference Voltage (I_{ref} = 400 μA)	5	V_{ref}	7.6	7.8	8.0	7.4	7.8	8.2	V
Temperature Coefficient of Reference Voltage (V_{CC} = 15 V, I_{ref} = 400 μA)	5	TCV_{ref}	–	0.008	0.03	–	0.008	0.03	%/°C
Input Regulation of Reference Voltage	5	$Reg_{(in)}$							mV/V
(I_{ref} = 400 μA)			–	3.0	7.5	–	4.0	7.5	
(I_{ref} = 1.0 mA)			–	5.0	–	–	5.0	–	
DC SUPPLY SECTION									
Supply Voltage	5	V_{in}	10	–	30	10	–	30	V
Supply Current (R_{ext} = 10 kΩ, excluding load and current and reference current)	5	I_D	–	–	16	–	–	22	mA
OSCILLATOR SECTION									
Line Frequency Stability	5								
(f = 20 kHz)		Δf	–	–	3.0	–	–	5.0	%
(f = 20 kHz, V_{CC} = 15 V, T_{low} to T_{high})		Δf	–	0.03	–	–	0.04	–	%/°C
Maximum Output Frequency (V_{CC} = 15 V)	6	f_{max}	100	200	–	100	200	–	kHz
Minimum Output Frequency (V_{CC} = 15 V)	6	f_{min}	–	2.0	5.0	–	2.0	5.0	kHz
Oscillator Output Saturation Voltage ($I_{14\ sink}$ = 5.0 mA)	11	$V_{osc(sat)}$	–	0.2	0.5	–	0.2	0.5	V
OUTPUT SECTION									
Output Saturation Voltage	7	$V_{CE(sat)}$							V
(I_L = 40 mA, T_{high} to T_{low})			–	0.33	0.5	–	0.33	0.5	
(I_L = 25 mA, T_{high} to T_{low})			–	0.22	–	–	0.22	–	
Output Leakage Current (V_{CE} = 40 V, pins 11 and 13)	8	I_{CE}	–	–	50	–	–	50	μA
COMPARATOR SECTION									
Pulse Width Adjustment Range	9	ΔPW	0	–	100	0	–	100	%
Dead Time Adjustment Range	9	ΔDT	0	–	100	0	–	100	%
Temperature Coefficient of Dead Time	–	TCDT	–	0.1	–	–	0.1	–	%/°C
Comparator Bias Currents	12, 13, 14	I_{IB}	–	5.0	15	–	5.0	15	μA

ELECTRICAL CHARACTERISTICS (continued)

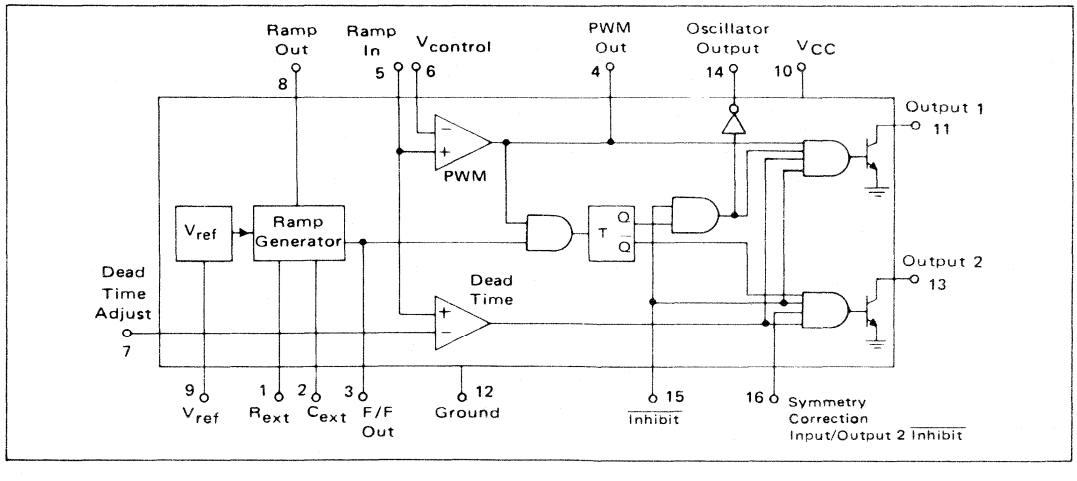
Characteristic	Figure	Symbol	MC3520 Min	MC3520 Typ	MC3520 Max	MC3420 Min	MC3420 Typ	MC3420 Max	Unit
AUXILIARY INPUTS/OUTPUTS									
Ramp Voltage Peak High Peak Low	5	 $V_{ramp(Hi)}$ $V_{ramp(Low)}$	 5.5 2.0	 6.0 2.4	 6.5 2.8	 5.5 2.0	 6.0 2.4	 6.5 2.8	V
Ramp Voltage Change ($V_{ramp\ Hi} - V_{ramp\ Low}$)	5	ΔV_{ramp}	3.0	3.5	4.0	3.0	3.5	4.0	V
Ramp Out Sink Current	5	I_{sink}	–	400	–	–	400	–	μA
Ramp Out Source Current	5	I_{source}	–	3.0	–	–	3.0	–	mA
$\overline{\text{Inhibit}}$ Input Current – High (V_{IH} = 2.0 V)	10	I_{IH}	–	–	40	–	–	40	μA
$\overline{\text{Inhibit}}$ Input Current – Low (V_{IL} = 0.8 V)	10	I_{IL}	–	-25	-180	–	-25	-180	μA
Symmetry Correction Input/Output 2 Inhibit Current – High (V_{SY} = 2.0 V, pin 16)	10	$I_{SY/H}$	–	–	40	–	–	40	μA
Symmetry Correction Input/Output 2 Inhibit Current – Low (V_{SY} = 0.8 V, pin 16)	10	$I_{SY/L}$	–	-10	-180	–	-10	-180	μA
F/F_{out} Source Current	–	I_{source}	–	2.0	–	–	2.0	–	mA
OUTPUT AC CHARACTERISTICS ($T_A = T_{high}$, V_{CC} = +15 V, f = 20 kHz)									
Rise Time	15	t_r	–	40	–	–	40	–	ns
Fall Time	15	t_f	–	150	–	–	150	–	ns
Overlap Time	15	t_{ov}	–	275	–	–	275	–	ns
Assymmetry (Duty Cycle = 50%)	15	$\frac{t_{on1} - t_{on2}}{t_{on1}}$	–	±1.0	–	–	±1.0	–	%

NOTE:

T_{high} = +125°C for MC3520
+70°C for MC3420

T_{low} = -55°C for MC3520
0°C for MC3420

FIGURE 2–EQUIVALENT CIRCUIT



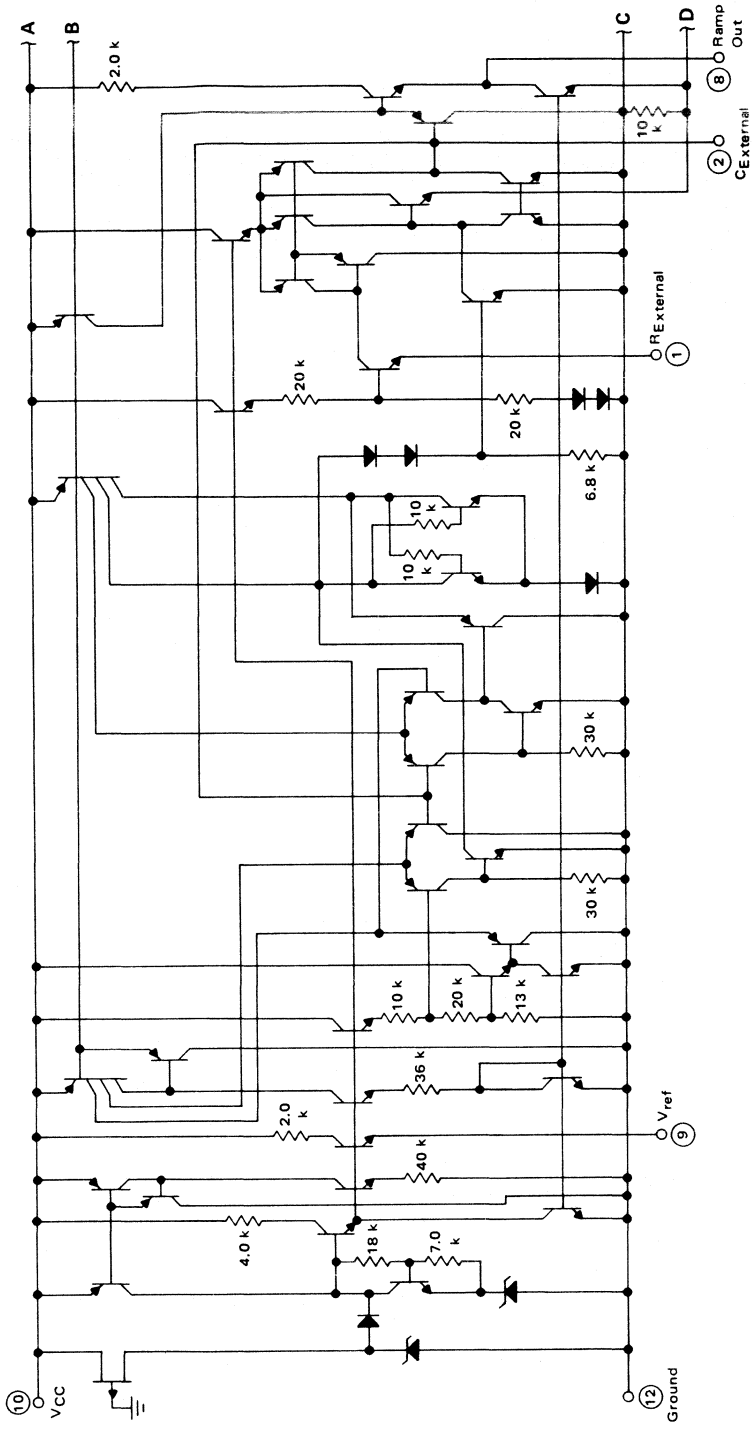
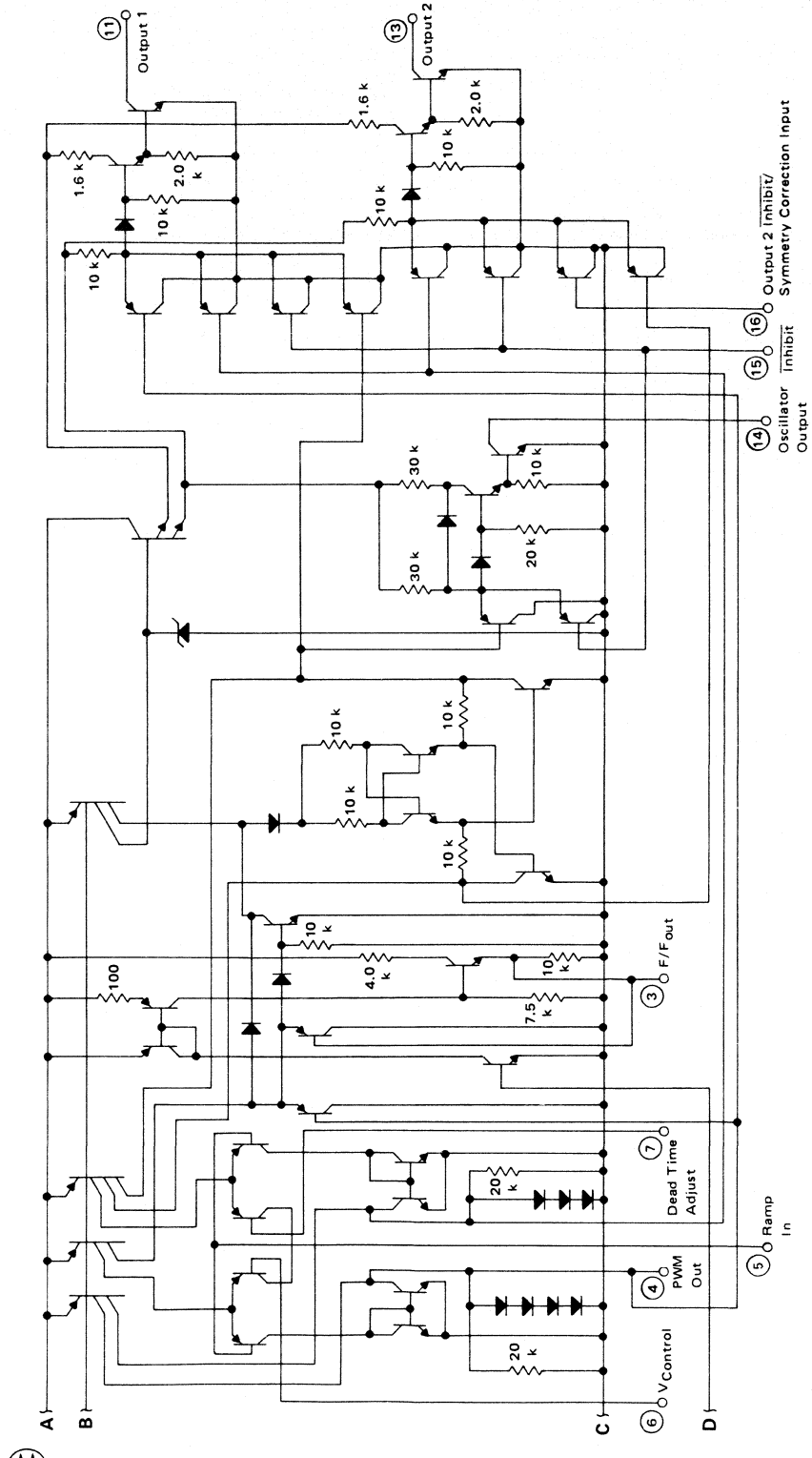


FIGURE 3 – CIRCUIT SCHEMATIC
(continued next page)



(continued) FIGURE 3 – CIRCUIT SCHEMATIC

The internal block diagram of the MC3420 is shown in Figure 2, and consists of the following sections:

Voltage Reference

A stable reference voltage is generated by the MC3420 primarily for internal use. However, it is also available externally at Pin 9 (V_{ref}) for use in setting the dead time (Pin 7) and for use as a reference for the external control loop error amplifiers.

Ramp Generator

The ramp generator section produces a symmetrical triangular waveform ramping between 2.4 V and 6.0 V, with frequency determined by an external resistor (R_{ext}) and capacitor (C_{ext}) tied from Pins 1 and 2, respectively, to ground.

PWM Comparator

The output of the ramp generator at pin 8 is normally connected to Pin 5, RAMP IN. The PWM (pulse width modulation) comparator compares the voltage at Pin 6 ($V_{control}$) to the ramp generator output. The level of $V_{control}$ determines the outputs' pulse width or duty cycle. The duty cycle of each output can vary, exclusive of dead time, from 50% (when $V_{control}$ is at approximately 2.4 V) to 0% ($V_{control}$ approximately 6.0 V).

Dead Time Comparator

An additional comparator has been included in MC3420 to allow independent adjustment of system dead time or maximum duty cycle. By dividing down V_{ref} at Pin 9 with a resistive divider or potentiometer, and applying this voltage to Pin 7, a stable dead time is obtained for prevention of inverter switching transistor cross conduction at high duty cycles due to storage time delays.

Phase Splitter

A phase splitter is included to obtain two 180° out of phase outputs for use in multiple transistor inverter systems. It consists of a toggle flip-flop whose clock signal is derived by "ANDing" the output of the PWM comparator and a signal from the ramp generator section. This "AND" gate ensures that the outputs truly alternate under control loop transient conditions. Better understanding of this feature and MC3420 operation may be gained by studying the circuit waveforms, shown in Figure 4.

FIGURE 4 – INTERNAL WAVEFORMS

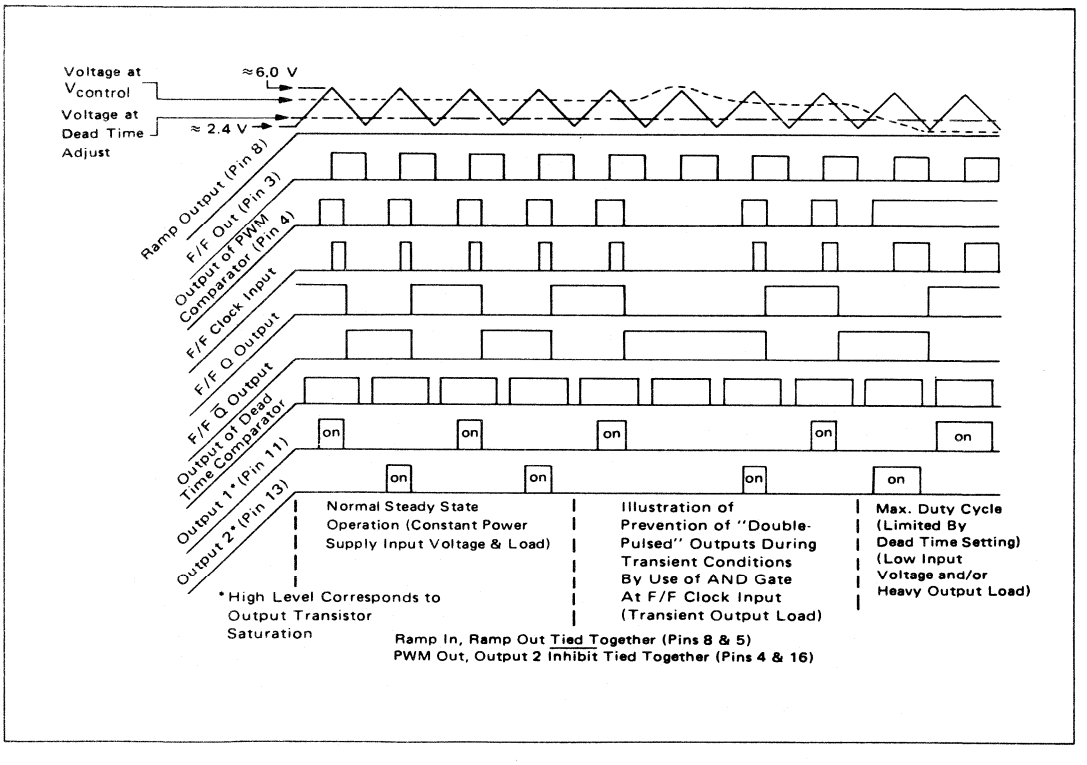


FIGURE 5 – STANDARD AC, DC TEST CIRCUIT

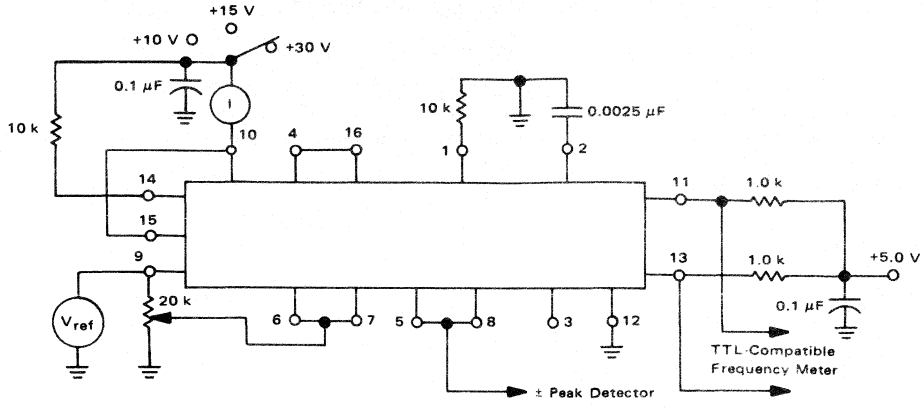


FIGURE 6 – FREQUENCY LIMIT TEST CIRCUIT

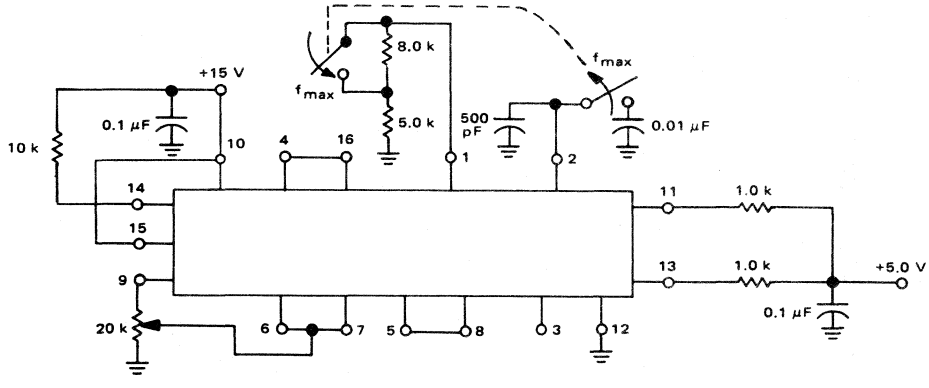
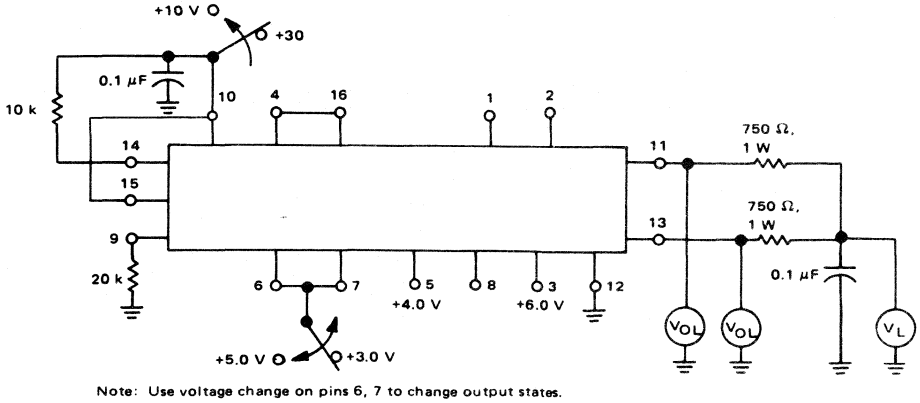
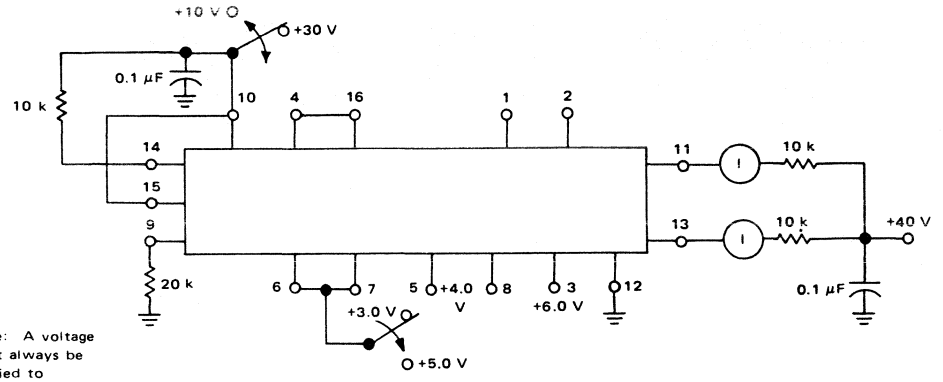


FIGURE 7 – OUTPUT SATURATION TEST CIRCUIT



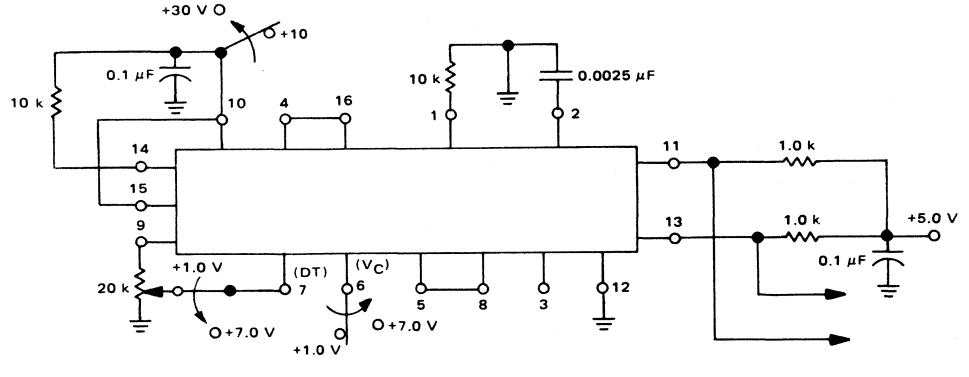
Note: Use voltage change on pins 6, 7 to change output states.
A voltage must always be present on pins 6 and 7.

FIGURE 8 – OUTPUT LEAKAGE TEST CIRCUIT



Note: A voltage must always be applied to pins 6 and 7.

FIGURE 9 – OUTPUT DUTY CYCLE TEST CIRCUIT



TYPICAL DUTY CYCLE versus DEAD TIME VOLTAGE		TYPICAL DUTY CYCLE versus PWM VOLTAGE ($V_{control}$)	
PIN 7. DEAD TIME VOLTAGE (V) ($V_{control}$ = 2.0 V)	% DUTY CYCLE (FOR EACH OUTPUT)	PIN 6. $V_{control}$ (V) (DEAD TIME VOLTAGE = 1.0 V)	% DUTY CYCLE (FOR EACH OUTPUT)
2.0	50	2.0	50
2.5	46	2.5	46
3.0	40	3.0	40
3.5	33	3.5	33
4.0	26	4.0	26
4.5	18	4.5	18
5.0	11	5.0	11
5.5	4.0	5.5	4.0
6.0	0	6.0	0

	V_6	V_7	
	Volts		
100% Adjust			
Dead Time	1.0	1.0	(Pin 11 + Pin 13 = Logic "1")
Pulse Width	1.0	1.0	
0% Adjust			
Dead Time	7.0	1.0	(Pin 11)(Pin 13) = Logic "1"
Pulse Width	1.0	7.0	

NOTE: Logic "1" is TTL-Compatible V_{OH}.

FIGURE 10 – INHIBIT/SYMMETRY TEST CIRCUIT

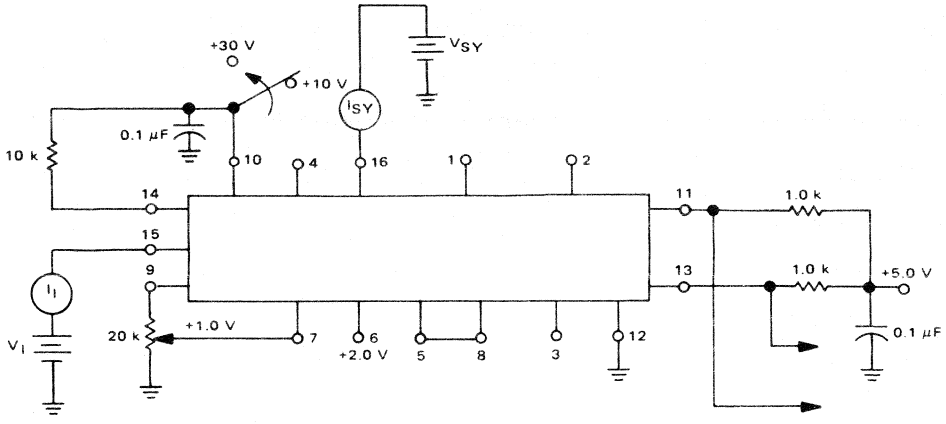


FIGURE 11 – OSCILLATOR OUTPUT (pin 14) TEST CIRCUIT

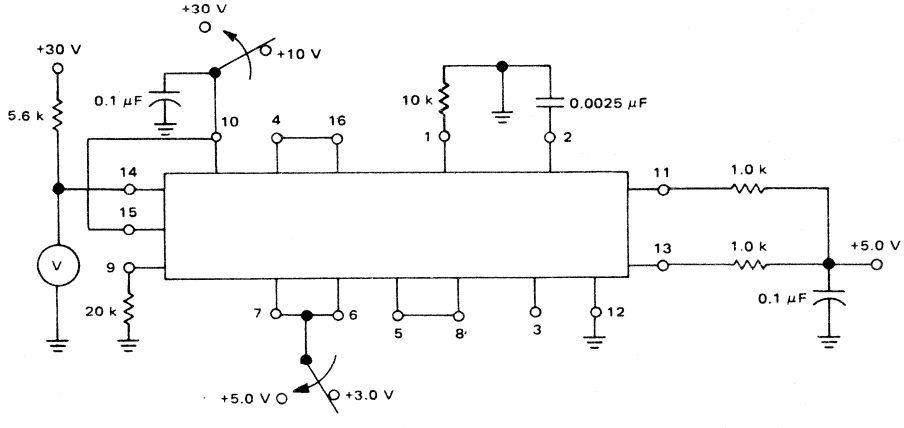


FIGURE 12 – $V_{Control}$ BIAS CURRENT TEST CIRCUIT

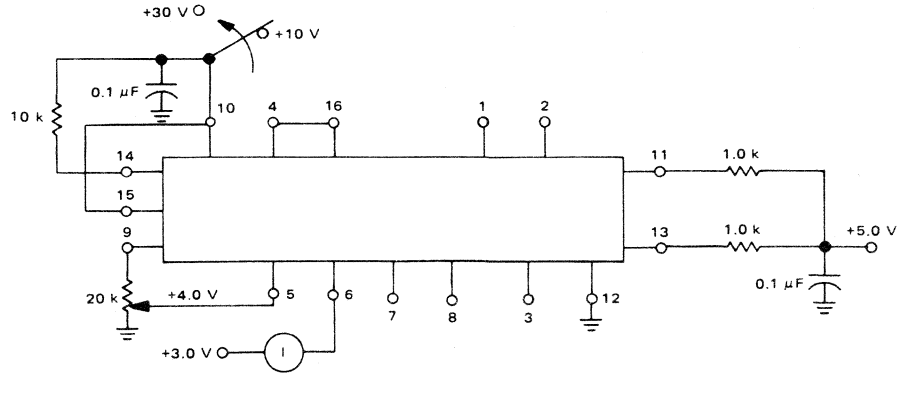


FIGURE 13 – DEAD TIME BIAS CURRENT TEST CIRCUIT

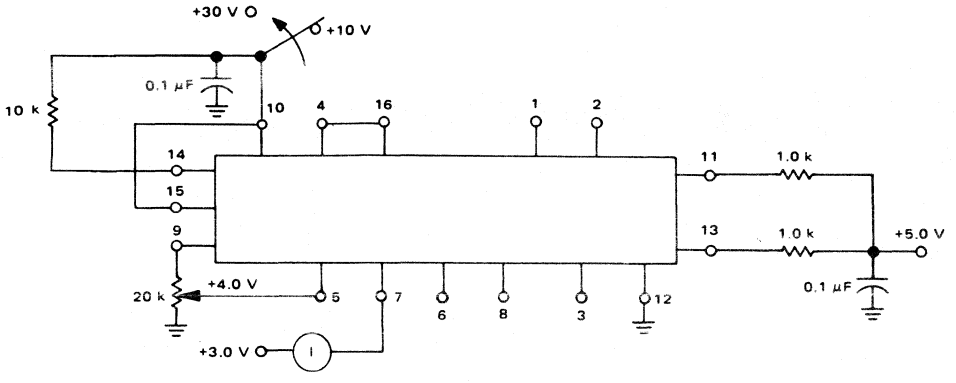


FIGURE 14 – RAMP IN BIAS CURRENT TEST CIRCUIT

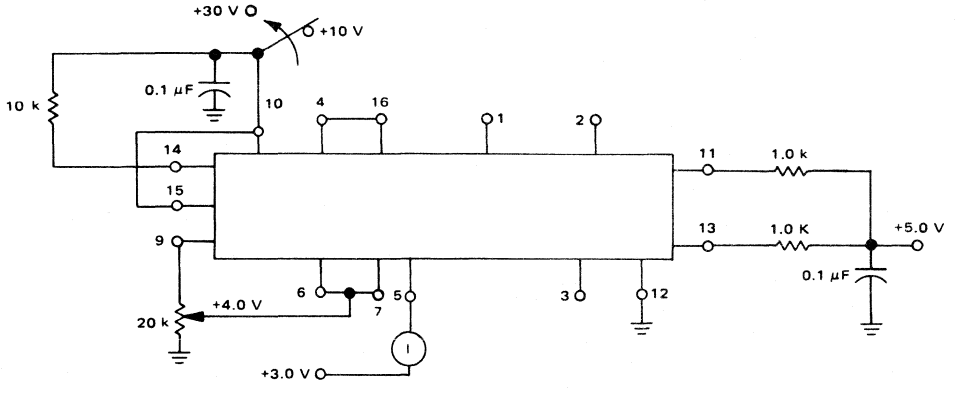
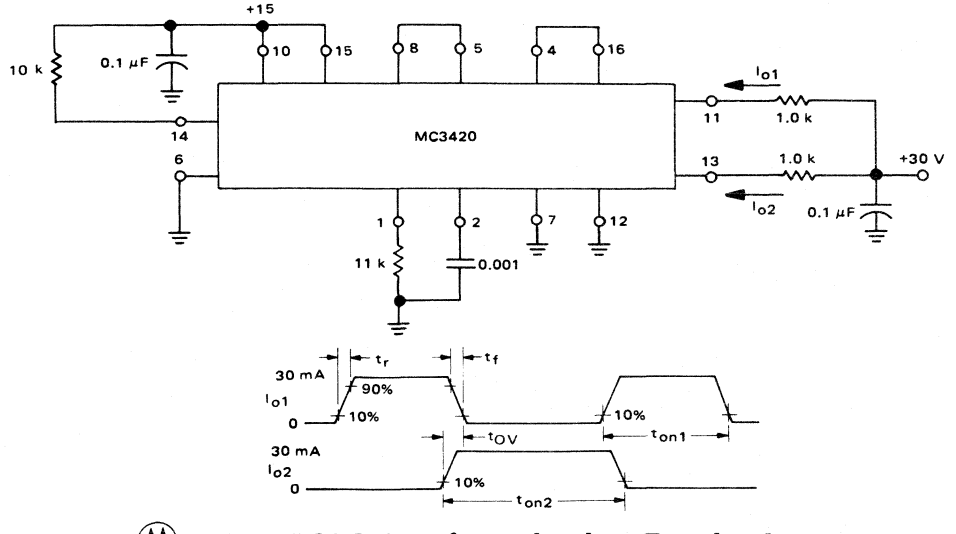


FIGURE 15 – AC TEST CIRCUIT AND WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 16 – OUTPUT SATURATION VOLTAGE versus LOAD CURRENT

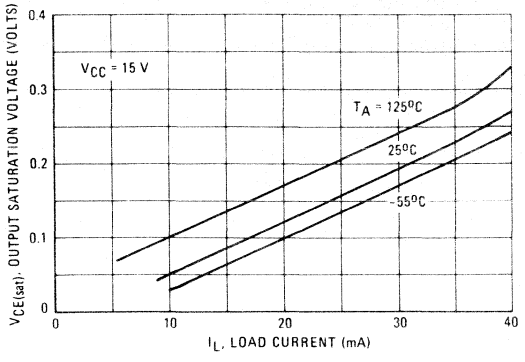


FIGURE 17 – REFERENCE VOLTAGE versus REFERENCE CURRENT

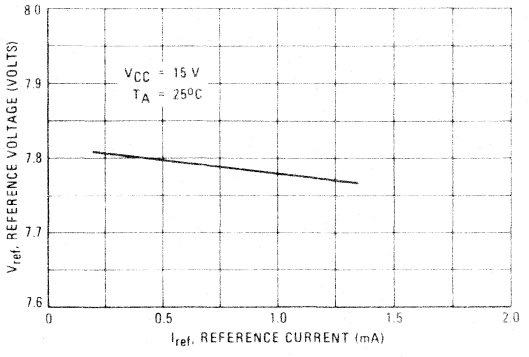


FIGURE 18 – DRAIN CURRENT versus EXTERNAL RESISTANCE

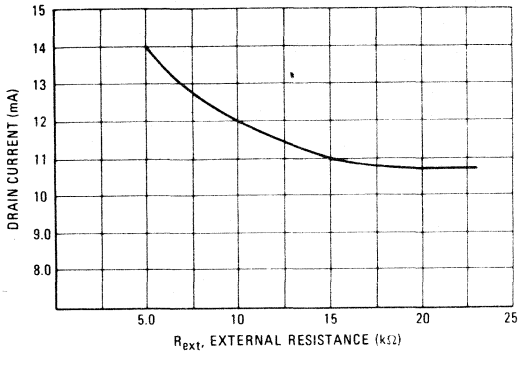


FIGURE 19 – PEAK FLIP-FLOP$_{out}$ VOLTAGE versus EXTERNAL RESISTANCE

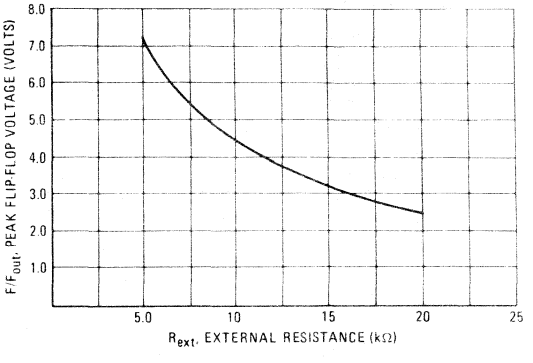


FIGURE 20 – DRAIN CURRENT versus TEMPERATURE

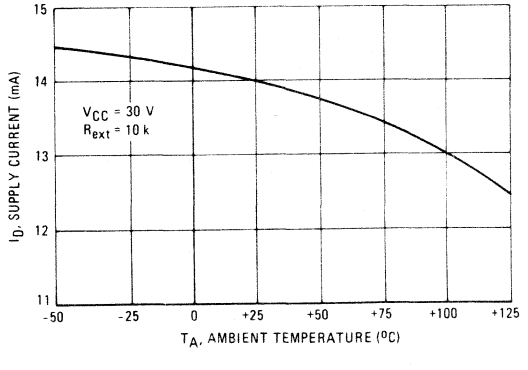
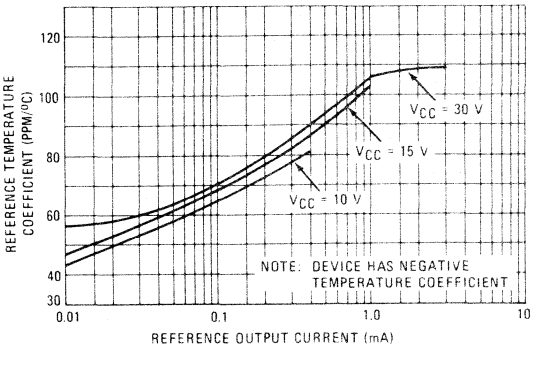


FIGURE 21 – REFERENCE VOLTAGE TEMPERATURE COEFFICIENT versus OUTPUT CURRENT

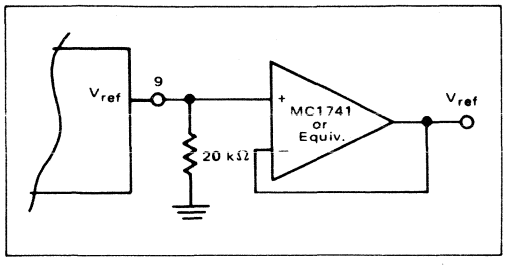


OPERATION AND APPLICATIONS INFORMATION

The Voltage Reference

The temperature coefficient of V_{ref} has been optimized for a 400 μA (≅20 kΩ) load. If increased current capability is required, an op amp buffer may be used, as shown in Figure 22.

FIGURE 22



Output Frequency

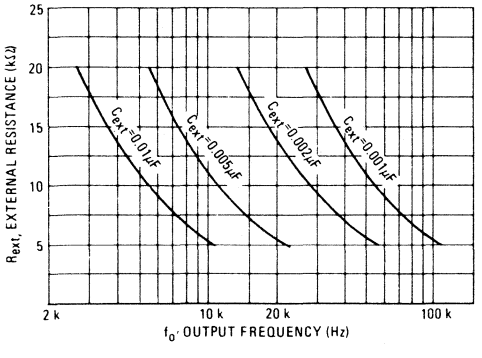
The values of R_{ext} and C_{ext} for a given output frequency, f_o, can be found from:

$$f_o \cong \frac{0.55}{R_{ext}\,C_{ext}} \; ; \; 5.0\,k\Omega \leq R_{ext} \leq 20\,k\Omega \quad \text{(Eq. 1)}$$

or from the graph shown in Figure 23.

Note that f_o refers to the frequency of Output 1 (Pin 11) or Output 2 (Pin 13). The frequency of the ramp generator output waveform at Pin 8 will be twice f_o.

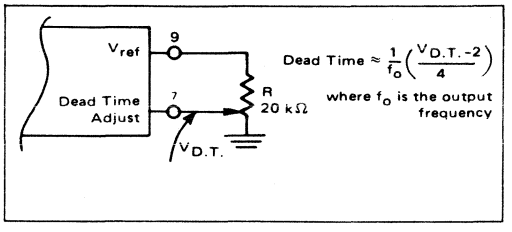
FIGURE 23



Dead Time

Figure 24 illustrates how to set or adjust the MC3420 outputs' dead time or maximum duty cycle. For minimum dead time drift with temperature or supply voltage, $V_{D.T.}$ should be derived from V_{ref} as shown.

FIGURE 24



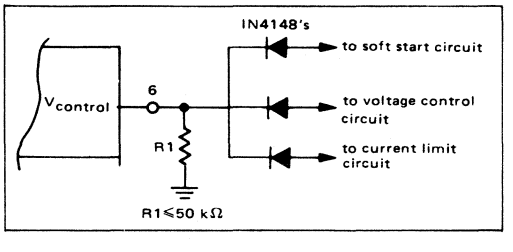
Connections to the $V_{control}$ Pin

In many systems, it is necessary to make multiple connections to the $V_{control}$ Pin in order to implement features in addition to voltage regulation such as current limiting, soft start, etc. These can be made by the use of a simple "diode-OR" connection, as shown in Figure 25. This allows whichever control element is seeking the lowest PWM duty cycle to dominate. Note that a resistor, R1, whose value is ≤ 50 kΩ is placed from the $V_{control}$ Pin to ground. This is necessary to provide a dc path for the PWM comparator input bias current under all conditions.

The system duty cycle is given by:

$$\text{D.C. (\%)} \cong \frac{V_{Control} - 2}{4} \times 100 \quad \text{(Eq. 2)}$$

FIGURE 25

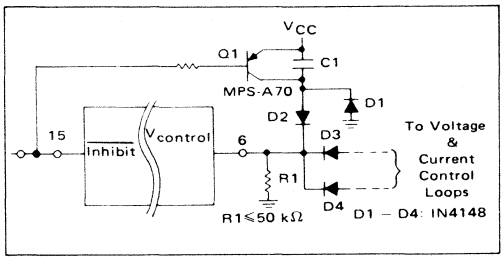


Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

Soft Start

In most PWM switching supplies, a soft start feature is desired to prevent output voltage overshoots and magnetizing current imbalances in the power transformer primary. This feature forces the duty cycle of the switching elements to gradually increase from zero to their normal operating point during initial system power-up or after an inhibit. This feature can be easily implemented with the MC3420. One method is shown in Figure 26.

FIGURE 26



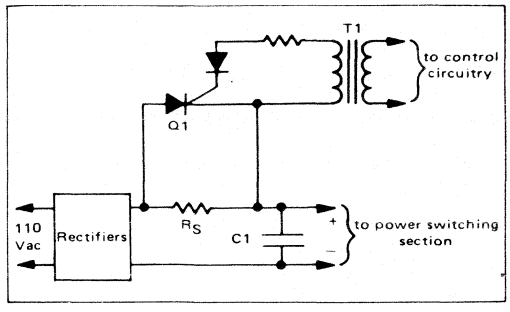
After an inhibit command or during power-up, the voltage on R1 and Pin 6 exponentially decays from V_{CC} toward ground with a time constant of R1C1, allowing a gradual increase in duty cycle. Diodes D2 – D4 provide a diode-or function at the $V_{control}$ Pin, while Q1 serves to reset the timing capacitor, C1, when an inhibit command is received thereby reinitializing the soft-start feature. D1 allows C1 to reset when power (V_{CC}) is turned off.

Inrush Current Limiting

Since many PWM switching supplies are operated directly off the rectified 110 Vac line with capacitive input filters, some means of preventing rectifier failure due to inrush surge currents is usually necessary. One method which can be used is shown in Figure 27.

In this circuit, a series resistor, R_S, is used to provide inrush surge current limiting. After the filter capacitor, C1, is charged, Q1 receives a trigger signal from the control circuitry through T1 and shorts R_S out of the circuit, eliminating its otherwise larger power dissipation. The trigger signal for Q1 may be derived from either the oscillator output (Pin 14) or one of the MC3420's outputs. If the oscillator output is used, it will be necessary

FIGURE 27

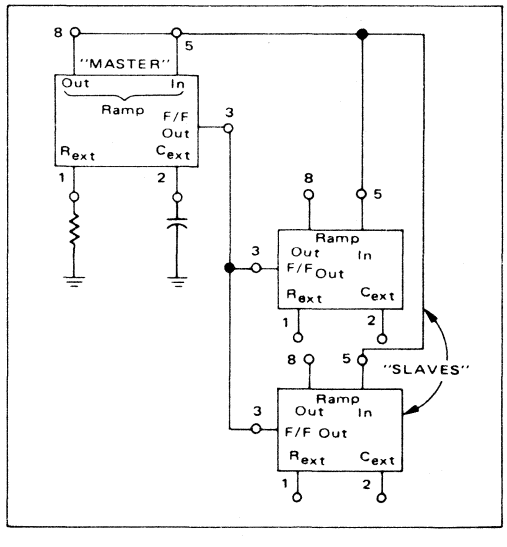


to provide a time delay on the inhibit pin to keep it low until the input filter capacitor, C1, has had time to charge, whereas the initial portion of the soft start timing cycle can be used for this delay if this signal is derived from one of the output pins. However, using the Oscillator Output Pin does offer the advantage that its waveform has a constant 50% duty cycle, independent of the outputs' duty cycle which can simplify the design of a drive circuit for T1.

Slaving

In some applications, as when one PWM inverter/converter is used to feed another, it may be desired that their frequencies be synchronized. This can be done with multiple MC3420s as shown in Figure 28. By omitting their R_{ext} and C_{ext}, up to two MC3420s may be slaved to a master MC3420.

FIGURE 28 – SLAVING THE MC3420



15 V, 2 A DC-to-DC Converter

Figure 29 illustrates the use of the MC3520 in a PWM switching power supply utilizing a single series switching element (see Appendix for description of PWM switching supply configurations). The series switching transistor, Q1, chops the dc input voltage, V_{in}, at a frequency of ≅ 25 kHz, and the resulting waveform is filtered by L1 and C1 to provide the dc output voltage. The frequency is set by R4 and C3, and since the outputs of the MC3520 are wire-ORed together, fo is twice that given by Equation 1 and Figure 23. V_o is regulated by comparing its value to the MC3520's reference voltage and amplifying the error voltage with U1. The output of U1 is fed into the MC3520 to provide PWM to Q1, thereby controlling its duty cycle and thus the value of V_o.

C2 provides a soft-start feature during power up to prevent output voltage overshoots and excessive start up currents through Q1.

Short circuit protection is provided by R_{SC}, Q3 and Q4. When an overcurrent condition occurs, Q3 is turned on by the voltage across R_{SC}; Q3 drives Q4 on, which raises the voltage at pin 6 ($V_{control}$) of the MC3520, reducing Q1's duty cycle and maintaining a constant output current of ≅ 2.5 A.

5 V, 50 A Line-Operated Supply

A 5 V, 50 A line-operated 20 kHz switching power supply using the MC3520 is shown in Figures 30a and b. An explanation of the operation of each section of the supply follows.

Input Section

The 120 Vac line is full wave voltage doubled by CR1, CR2, C1 and C2 to provide 310 Vdc to the power section of the supply. Inrush surge current limiting is provided by R1, which is shorted out of the circuit by Q1 after C1 and C2 are initially charged.

Power Section

The supply utilizes two switching transistors, Q2 and Q3, in a half-bridge configuration (see Appendix) to drive the high frequency power transformer, T2.

The bases of Q2 and Q3 are driven by T3 and T4, respectively, to provide isolation from the control and base drive sections of the supply. CR3, CR5, CR6, and CR8 constitute anti-saturation (Baker) clamps which provide increased and more uniform switching speeds for Q2 and Q3. CR4 and CR7 allow reverse base currents during turn off.

Output Section

The output of T2 is rectified by Schottky diodes, CR9 and CR10. VR1 is a transient suppressor to protect CR9 and CR10 from transients that might cause reverse breakdown. L1 and C4 constitute the output filter. C4 should have very low ESR (equivalent series resistance) at 20 kHz to provide the most effective filtering. L2 and C5 make up a high-frequency filter to reduce commutation spikes which pass L1 due to its interwinding capacitance. R_{SC} provides output overcurrent sensing to the control section.

Control Section

The MC3520 provides the PWM control for the supply. R2 is adjusted to obtain a 20 kHz operating frequency. R3 adjusts the dead time (≅ 5 μs each half-cycle). U1A and U1B are the output current and output voltage error amplifiers, respectively. R5 sets the output voltage while R4 determines the output current limit. C7 and C8 are the current and voltage loop compensation capacitors.

C6 provides the soft-start feature while Q4 ensures a soft-start after each system inhibit (pin 15 low).

Base Drive Section

Turn on drive to the power section switching transistors occurs when each of the outputs of the MC3520 saturate. Q5 or Q6 are therefore turned on, and 15 V applied to the primaries of T3 or T4, supplying forward base drive to Q2 or Q3.

Turn off drive occurs when Q5 or Q6 turn off, and the magnetizing energy stored in T3 or T4's core is transformed into a negative "flyback" voltage at their secondaries, providing reverse base drive to Q2 or Q3. CR11 and CR12 act as clamps, to prevent this flyback voltage from exceeding -5 V at T3 or T4's secondary (30 V on Q5 or Q6's collector).

Q1 Driver Section

Q7 and T1 provide the gate drive to Q1. Q7 starts operating after an initial delay of 100 ms created by the soft-start circuit, thereby allowing C1 and C2 to charge up before firing Q1.

FIGURE 29 – 15 V, 2A DC-TO-DC CONVERTER

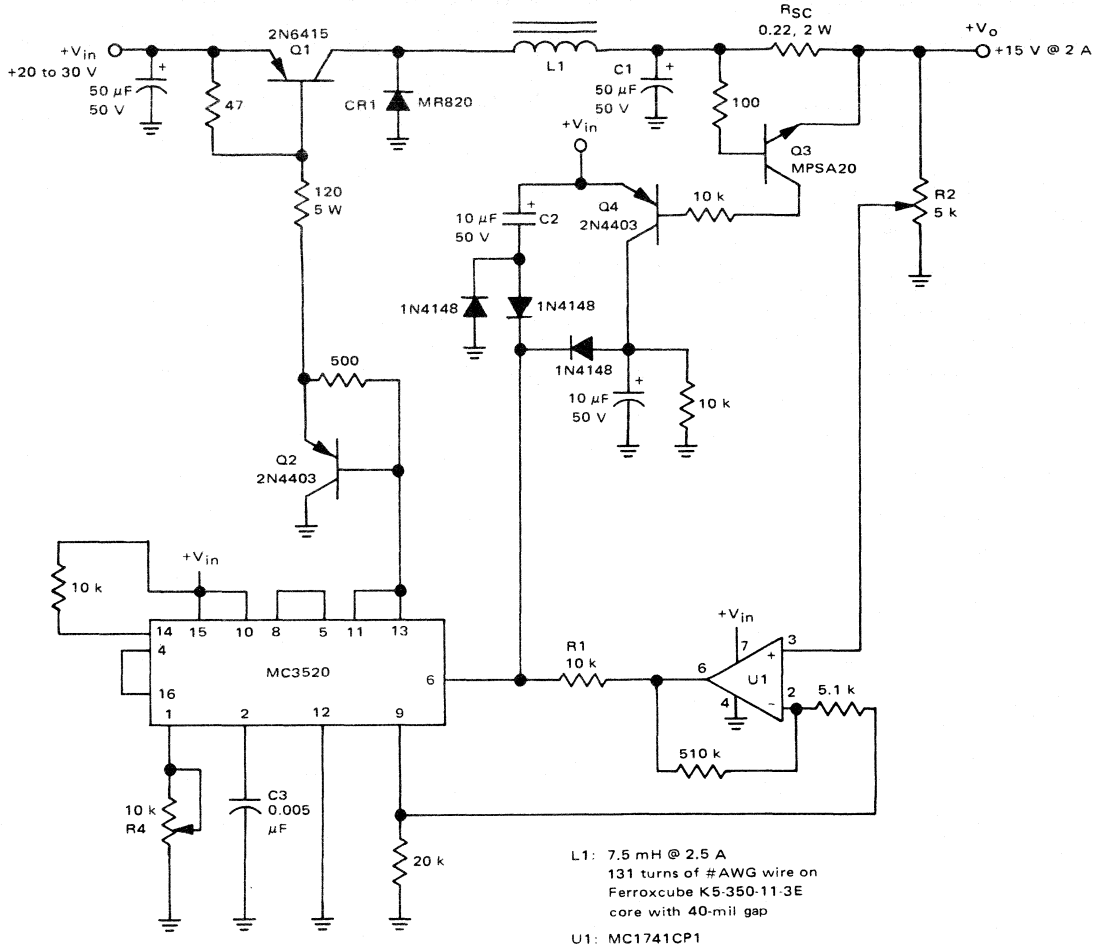
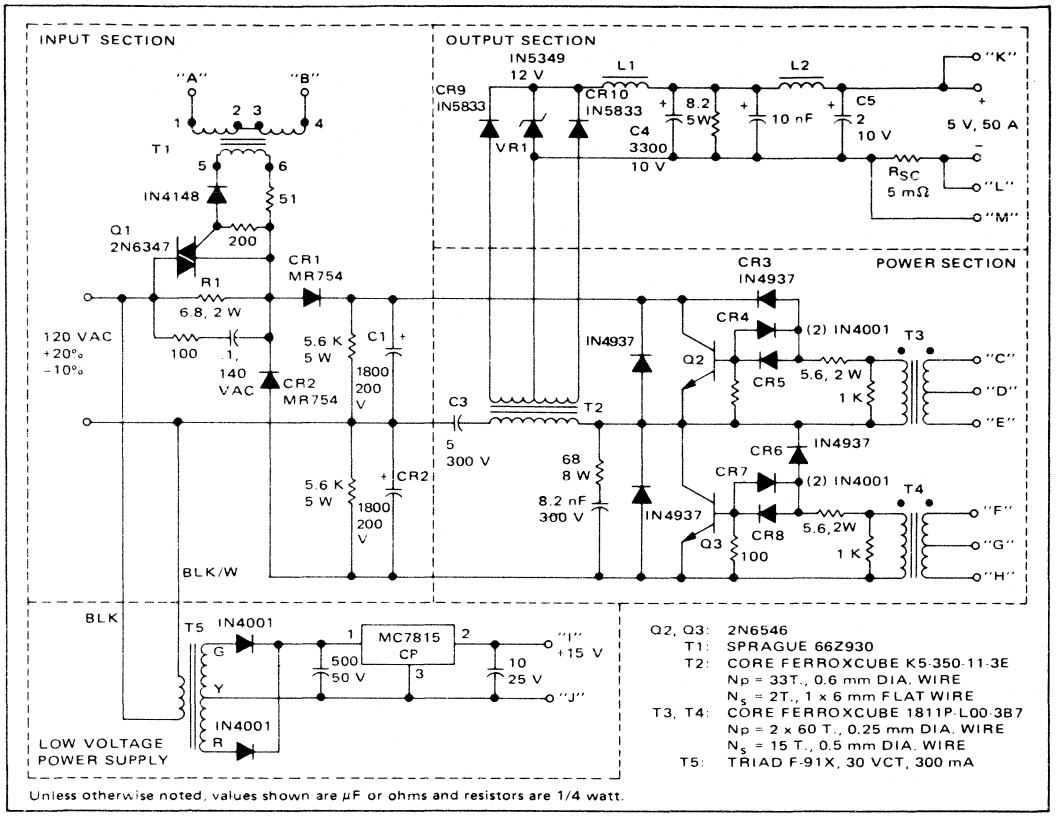


FIGURE 30a – 5 V, 50A LINE-OPERATED SUPPLY **(continued on following page)**

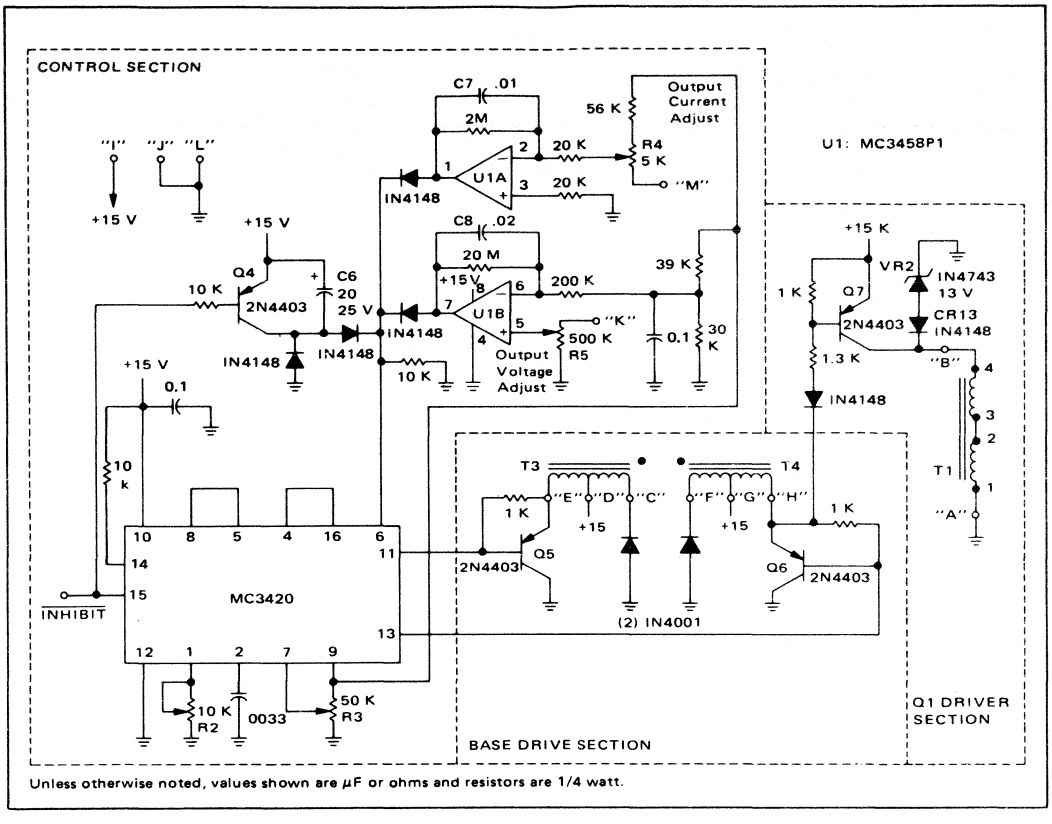


Q2, Q3: 2N6546
T1: SPRAGUE 66Z930
T2: CORE FERROXCUBE K5-350-11-3E
N_p = 33T., 0.6 mm DIA. WIRE
N_s = 2T., 1 x 6 mm FLAT WIRE
T3, T4: CORE FERROXCUBE 1811P-L00-3B7
N_p = 2 x 60 T., 0.25 mm DIA. WIRE
N_s = 15 T., 0.5 mm DIA. WIRE
T5: TRIAD F-91X, 30 VCT, 300 mA

Unless otherwise noted, values shown are μF or ohms and resistors are 1/4 watt.

Performance	
Line Regulation:	0.4%
Load Regulation:	0.25%
Output Ripple and Noise:	60 mV p-p
	25 mV rms
Line current surge at turn-on:	35 A max
Efficiency:	80%

FIGURE 30b



Unless otherwise noted, values shown are μF or ohms and resistors are 1/4 watt.

APPENDIX: BASIC PWM SWITCHING SUPPLY POWER CIRCUIT CONFIGURATIONS

The material given in this section is intended to acquaint the designer with the basic switching transistor configurations used in PWM power supplies. Circuit configurations, collector voltage and current waveforms of the switching transistors, and required transistor specifications for the most commonly utilized configurations are shown in Figures 1A through 4A. It should be noted that the waveforms and specifications are idealized, in that the effects of leakage inductance voltage spikes, stray circuit capacitance, snubber networks, clamp diode overshoots, diode reverse recovery and saturation voltages have been neglected. For more information on these effects, the configurations, or switching supplies in general, consult the references listed in the References section.

Series Configuration

The single transistor series configuration is shown in Figure 1A. This configuration is usually limited to applications in which $0.2\ V_{CC} < V_o < 0.8\ V_{CC}$ and where input-output isolation is not required.

Push-Pull Configuration

Figure 2A shows the two-transistor push-pull configuration. Unlike the series configuration, it can be used to either step-up or step-down the input voltage, V_{CC}, and also provides input-output isolation. It does, however, have the disadvantage that additional circuitry must be used to provide symmetry correction for the prevention of transformer saturation.

Half-Bridge Configuration

The half-bridge configuration, shown in Figure 3A, does not suffer from the symmetry problems of the push-pull configuration since the transformer primary is capacitively coupled. This prevents transformer core saturation since no net dc current is allowed to flow in its primary.

Note that for the same input power, bus voltage, and duty cycle, the half-bridge requires switching transistors which have twice the current and half the voltage requirements as those of the push-pull configuration.

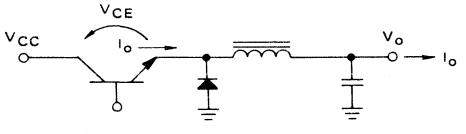
Full-Bridge Configuration

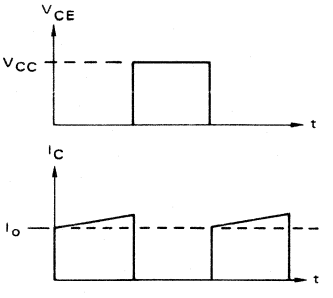
By replacing the bridge capacitors, C, of the half-bridge configuration of Figure 4A results. With this configuration, double the power of the half-bridge configuration can be obtained at the expense of two additional switching transistors and their associated circuitry.

ABBREVIATIONS USED IN FIGURES 1A THROUGH 4A

I_C:	Switching transistor collector current
V_{CE}:	Switching transistor collector-to-emitter-voltage
P_{in}:	Average input power
D.C.:	Inverter duty cycle
V_{CC}:	DC bus voltage
$V_{CEO(sus)}$:	V_{CE} that transistor must withstand during turn-on
V_{CEX}:	V_{CE} that transistor must block during non-conduction period.

FIGURE 1A – SERIES CONFIGURATION





TRANSISTOR REQUIREMENTS*

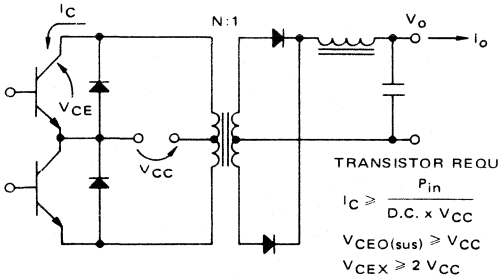
$I_C \geq I_o$

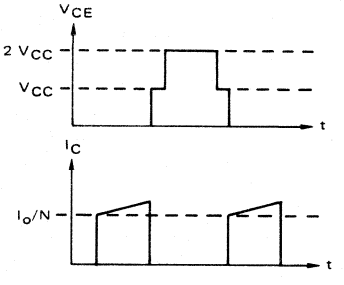
$V_{CEO(sus)} \geq V_{CC}$

$V_{CEX} \geq V_{CC}$

*See explanation of abbreviations in text.

FIGURE 2A – PUSH-PULL CONFIGURATION





TRANSISTOR REQUIREMENTS*

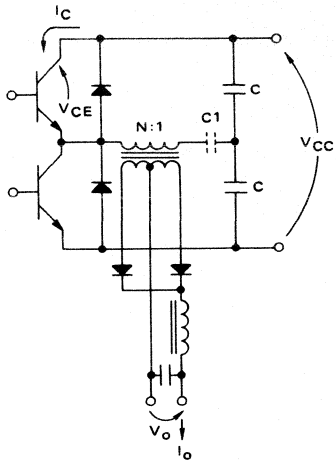
$I_C \geq \frac{P_{in}}{D.C. \times V_{CC}}$

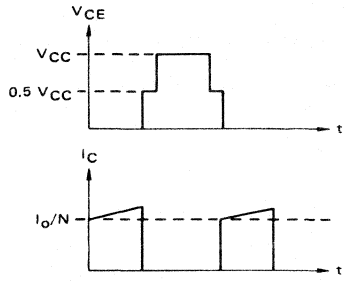
$V_{CEO(sus)} \geq V_{CC}$

$V_{CEX} \geq 2\ V_{CC}$

*See explanation of abbreviations in text.

FIGURE 3A – HALF-BRIDGE CONFIGURATION





TRANSISTOR REQUIREMENTS*

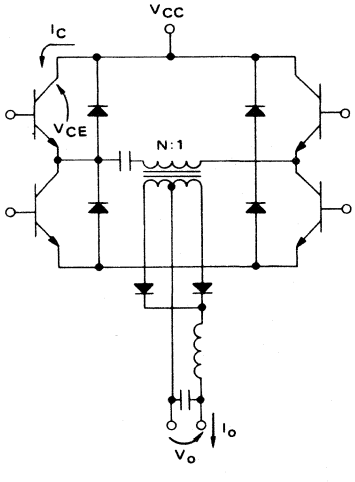
$$I_C \geq \frac{2 \times P_{in}}{D.C. \times V_{CC}}$$

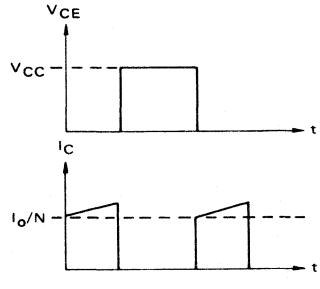
$V_{CEO(sus)} \geq V_{CC}/2$

$V_{CEX} \geq V_{CC}$

*See explanation of abbreviations in text.

FIGURE 4A – FULL-BRIDGE CONFIGURATION





TRANSISTOR REQUIREMENTS*

$$I_C \geq \frac{P_{in}}{D.C. \times V_{CC}}$$

$V_{CEO(sus)} \geq V_{CC}$

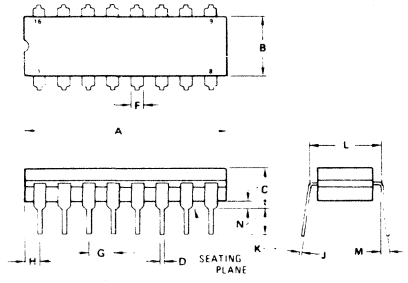
$V_{CEX} \geq V_{CC}$

*See explanation of abbreviations in text.

REFERENCES

More detailed information on switching power supplies may be obtained by consulting the following articles:

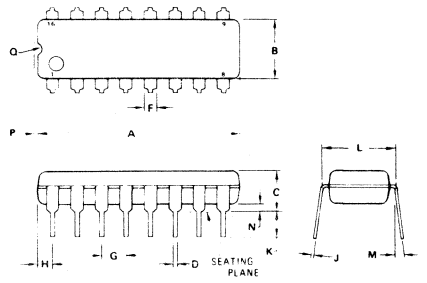
1. L. Jansson: "A Survey of Converter Circuits for SMPS," Mullard Technical Communications #119, July 1973.
2. R. Haver: "A New Approach to Switching Regulators," Motorola AN-719, May 1974.
3. R. Haver: "Switched Mode Power Supplies, a 5 V, 40 A Design," Motorola AN-737, December 1974.
4. W. Hersom: "Optimizing the High Current Transistor Converter," *Solid State Power Conversion,* March/April 1975.
5. W. Hirshberg: "Simplify Converter Designs with Flyback," *Solid State Power Conversion,* March/April 1975.
6. P. Wood: "Design of a 5 V, 100 Watt Power Supply, TRW AN #122, February 1975.
7. J. Turnbull: "Radio Frequency Interference Suppression in SMPS," Ferroxcube AN-F601.
8. W. Hetterscheid: "Base Circuit Design for High-Voltage Switching Transistors in Power Converters," Mullard Technical Communications (North American Phillips) #473, November 1974.
9. B. George: "6 V 100 A Switched-Mode Power Supply Operating Directly from the Mains," Mullard Technical Communications (North American Phillips) #123, July 1974.
10. B. Bailey: "Circuit Design and Semiconductor Selection for Square-Wave and Sine-Wave Inverters," *Proc. of Powercon 2,* October 1975.
11. B. Bailey: "Safe Reverse Bias Operation—A New Approach," *Proc. of Powercon 3,* June 1976.
12. Gutmann and Suva: "A Line-Operated, Regulated 5 V/50 A Switching Power Supply," Motorola AN-767, September 1976.



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	0.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

L SUFFIX
CERAMIC PACKAGE
CASE 620
$R_{\theta JA}$=100°C/W



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

P SUFFIX
PLASTIC PACKAGE
CASE 648
$R_{\theta JA}$=100°C/W

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geq I_C V_{CC}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

I_C = Total Sink Current

V_{CC} = Supply Voltage

MOTOROLA Semiconductors

MC3423
MC3523

Specifications and Applications Information

OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

These overvoltage protection circuits (OVP) protect sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. They sense the overvoltage condition and quickly "crowbar" or short circuit the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

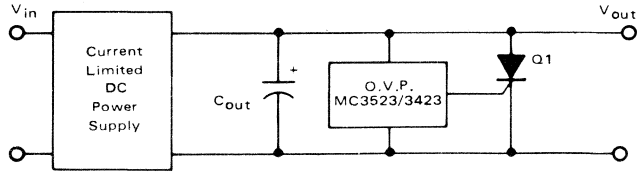
The protection voltage threshold is adjustable and the MC3423/3523 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

The MC3423/3523 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Differential Power Supply Voltage	V_{CC}-V_{EE}	40	Vdc
Sense Voltage (1)	$V_{Sense\ 1}$	6.5	Vdc
Sense Voltage (2)	$V_{Sense\ 2}$	6.5	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperature Range MC3423 MC3523	T_A	 0 to +70 –55 to +125	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 125 150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

TYPICAL APPLICATION

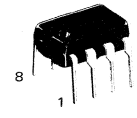


NOTE: A 2N6504 or equivalent is suggested for Q1.

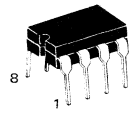
OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

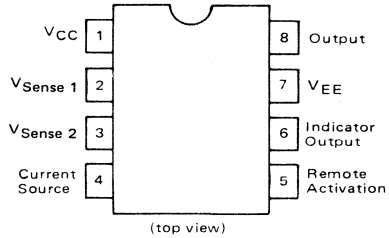
P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC3423 only)



U SUFFIX
CERAMIC PACKAGE
CASE 693



PIN CONNECTIONS



(top view)

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC3423P1	0 to +70°C	Plastic DIP
MC3423U	0 to +70°C	Ceramic DIP
MC3523U	–55 to +125°C	Ceramic DIP

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ELECTRICAL CHARACTERISTICS ($5\ V \leq V_{CC} - V_{EE} \leq 36\ V$, $T_{low} < T_A < T_{high}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}-V_{EE}	4.5	–	40	Vdc
Output Voltage (I_O = 100 mA)	V_O	V_{CC}-2.2	V_{CC}-1.8	–	Vdc
Indicator Output Voltage ($I_{O(Ind)}$ = 1.6 mA)	$V_{OL(Ind)}$	–	0.1	0.4	Vdc
Sense Voltage (T_A = 25°C)	$V_{Sense\ 1}$, $V_{Sense\ 2}$	2.45	2.6	2.75	Vdc
Temperature Coefficient of $V_{Sense\ 1}$ (Figure 2)	TCV_{S1}	–	0.06	–	%/°C
Remote Activation Input Current (V_{IH} = 2.0 V, V_{CC}-V_{EE} = 5.0 V) (V_{IL} = 0.8 V, V_{CC}-V_{EE} = 5.0 V)	I_{IH} I_{IL}	– –	5.0 -120	40 -180	μA
Source Current	I_{source}	0.1	0.2	0.3	mA
Output Current Risetime (T_A = 25°C)	t_r	–	400	–	mA/μs
Propagation Delay (T_A = 25°C)	t_{pd}	–	0.5	–	μs
Supply Current MC3423 MC3523	I_D	– –	6.0 5.0	10 7.0	mA

T_{low} = -55°C for MC3523
= 0°C for MC3423

T_{high} = +125°C for MC3523
= +70°C for MC3423

FIGURE 1 – BLOCK DIAGRAM

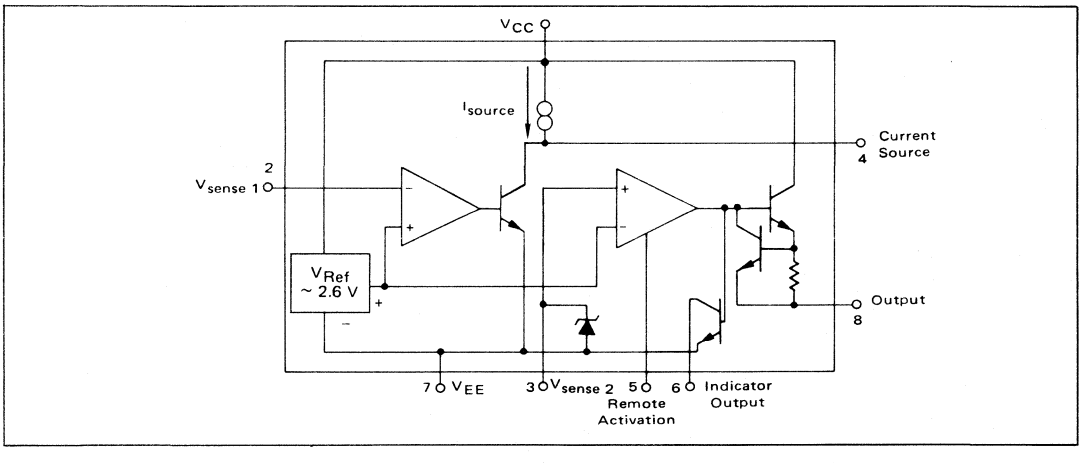
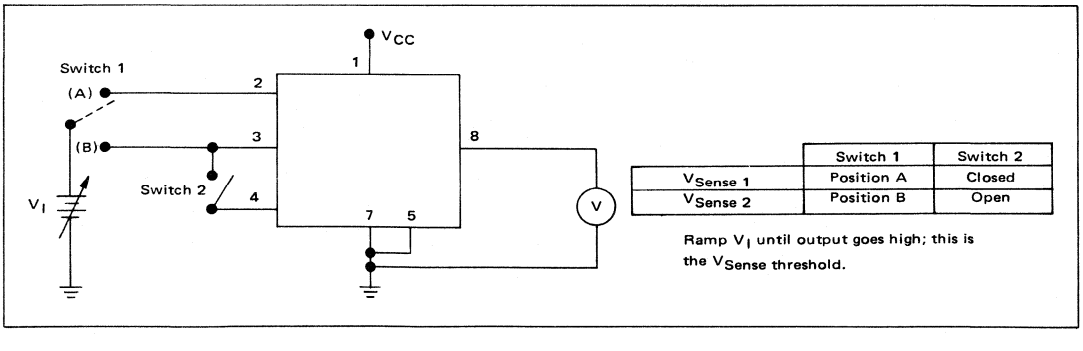


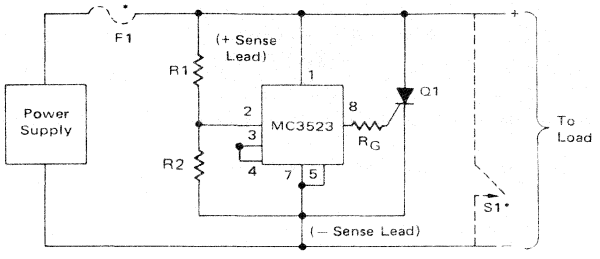
FIGURE 2 – SENSE VOLTAGE TEST CIRCUIT



	Switch 1	Switch 2
$V_{Sense\ 1}$	Position A	Closed
$V_{Sense\ 2}$	Position B	Open

Ramp V_I until output goes high; this is the V_{Sense} threshold.

FIGURE 3 – BASIC CIRCUIT CONFIGURATION



$V_{trip} = V_{ref}\left(1+\frac{R1}{R2}\right) \approx 2.6\ V\left(1+\frac{R1}{R2}\right)$

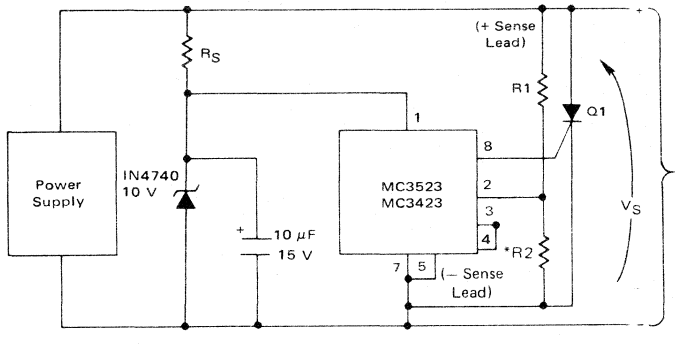
$R2 \leq 10\ k\Omega$ for minimum drift

For minimum value of R_G, see Figure 9

Q1 is 2N6504 or equivalent

*See text for explanation

FIGURE 4 – CIRCUIT CONFIGURATION FOR SUPPLY VOLTAGE ABOVE 36 V



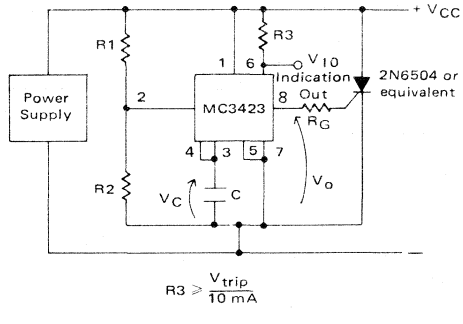
$R_S = \left(\frac{V_S - 10}{25}\right) k\Omega$

$V_{trip} = V_{ref}\left(1+\frac{R1}{R2}\right) \approx 2.6\ V\left(1+\frac{R1}{R2}\right)$

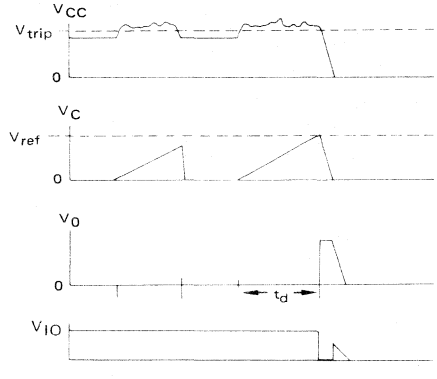
*$R2 \leq 10\ k\Omega$

Q1: $V_S \leq 50$ V; 2N6504 or equivalent
$V_S \leq 100$ V; 2N6505 or equivalent
$V_S \leq 200$ V; 2N6506 or equivalent
$V_S \leq 400$ V; 2N6507 or equivalent
$V_S \leq 600$ V; 2N6508 or equivalent
$V_S \leq 800$ V; 2N6509 or equivalent

FIGURE 5 – BASIC CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP



$R3 \geqslant \frac{V_{trip}}{10\ mA}$



$t_d = \left(\frac{V_{ref}}{I_{source}} \times C \approx [12 \times 10^3]\ C\right)$ (See Figure 10)

APPLICATIONS INFORMATION

BASIC CIRCUIT CONFIGURATION

The basic circuit configuration of the MC3423/3523 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V, and in Figure 4 for trip voltages above 36 V. The threshold or trip voltage at which the MC3423/3523 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, R_G, is given in Figure 9. Using this value of R_G, the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423/3523. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Figure 3 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

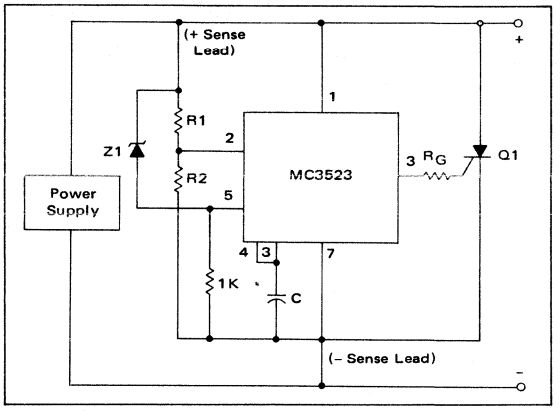
The circuit configurations shown in Figures 3 and 4 will have a typical propogation delay of 1.0 μs. If faster operation is desired, pin 3 may be connected to pin 2 with pin 4 left floating. This will result in decreasing the propogation delay to approximately 0.5 μs at the expense of a slightly increased TC for the trip voltage value.

CONFIGURATION FOR PROGRAMMABLE MINIMUM DURATION OF OVERVOLTAGE CONDITION BEFORE TRIPPING

In many instances, the MC3423/3523 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423/3523 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from pin 3 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When V_{CC} rises above the trip point set by R1 and R2, an internal current source (pin 4) begins charging the capacitor, C, connected to pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≅ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds V_{Z1} + 1.4 V.

FIGURE 6 – CONFIGURATION FOR PROGRAMMABLE DURATION OF OVERVOLTAGE CONDITION BEFORE TRIP/WITH IMMEDIATE TRIP AT HIGH OVERVOLTAGES



ADDITIONAL FEATURES

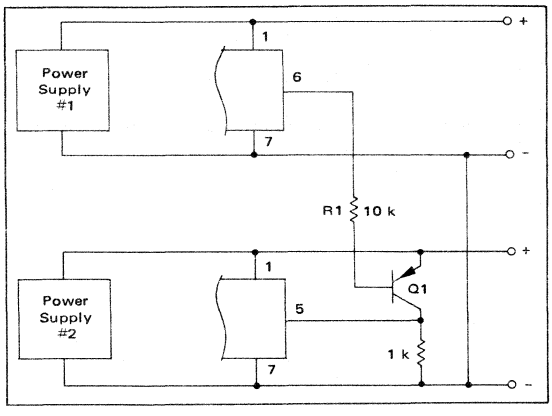
1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423/3523. This output is an open collector transistor which saturates when the OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V as in Figure 5. This output can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

2. Remote Activation Input

Another feature of the MC3423/3523 is its remote activation input, pin 5. If the volage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423/3523 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423/3523 can be used to activate another MC3423/3523 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

FIGURE 7 – CIRCUIT CONFIGURATION FOR ACTIVATING ONE MC3523 FROM ANOTHER



Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}[1]. This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the application make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities – depending on the severity of the occasion.

[1] C_{out} consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps.

FIGURE 8 – R1 versus TRIP VOLTAGE

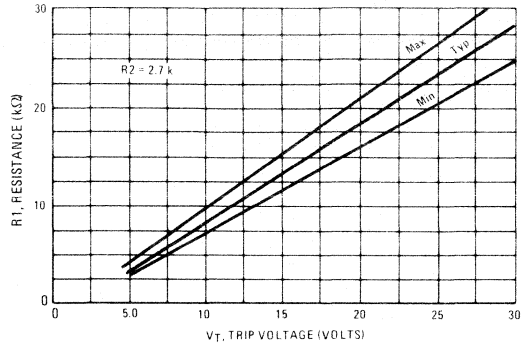


FIGURE 9 – MINIMUM R_G versus SUPPLY VOLTAGE

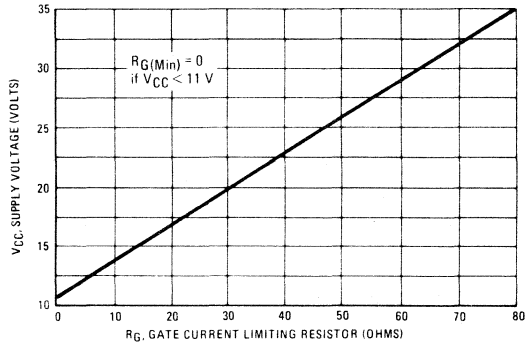


FIGURE 10 – CAPACITANCE versus MINIMUM OVERVOLTAGE DURATION

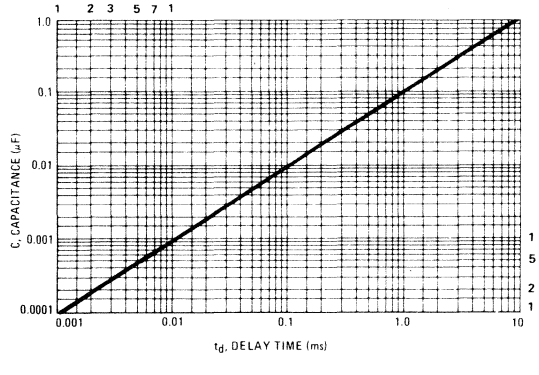


FIGURE 11 – TYPICAL CROWBAR OVP CIRCUIT CONFIGURATIONS

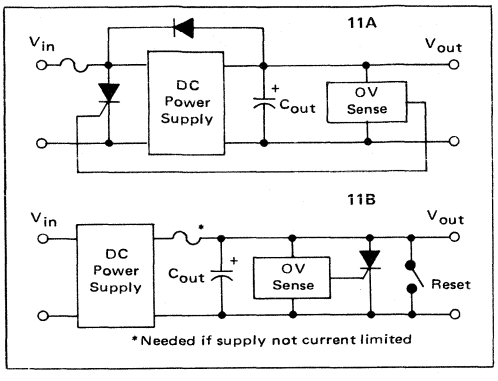


FIGURE 12 – CROWBAR SCR SURGE CURRENT WAVEFORM

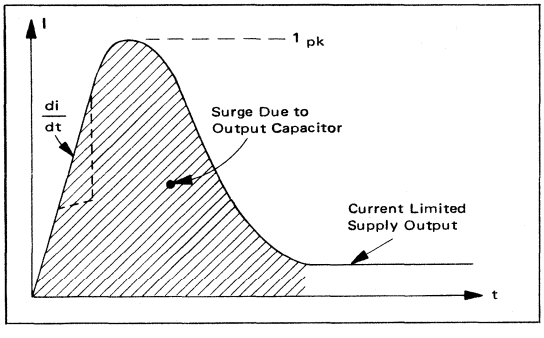
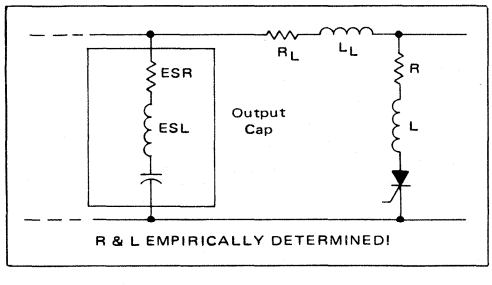


FIGURE 13 – CIRCUIT ELEMENTS AFFECTING SCR SURGE & di/dt



The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast (< 1 μs) rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 Arms rating might be 200 A/μs, assuming a gate current of five times I_{GT} and < 1 μs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance – see Figure 13) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Refering back to Figure 11A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

DEVICE	I_{RMS}	I_{TSM}	PACKAGE
2N6400 Series	16A	160A	TO220 Plastic
2N6504 Series	25A	160A	TO220 Plastic
2N1842 Series	16A	125A	Metal Stud
2N2573 Series	25A	260A	Metal TO-3 Type
2N681 Series	25A	200A	Metal Stud
MCR3935-1 Series	35A	350A	Metal Stud
MCR81-5 Series	80A	1000A	Metal Stud

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geq V_{CC}I_S - V_OI_O$$

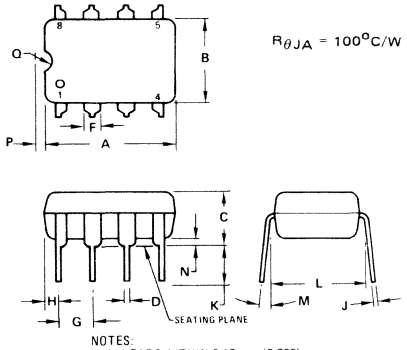
Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

I_S = Total Supply Current

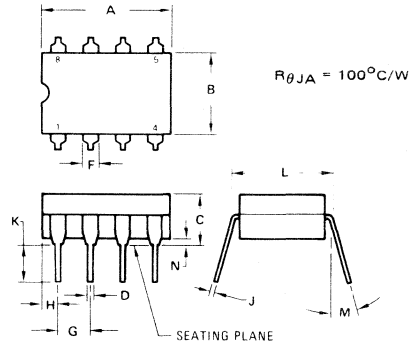


$R_{\theta JA}$ = 100°C/W

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	0.76	0.020	0.030
P	0.13	0.38	0.005	0.015
Q	0.76	1.02	0.030	0.040

CASE 626-03
(MC3423 only)
P1 SUFFIX
PLASTIC PACKAGE



$R_{\theta JA}$ = 100°C/W

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 693-02

U SUFFIX
CERAMIC PACKAGE

MOTOROLA Semiconductors

MCR70 series
(35 Amperes RMS)

MCR71 series
(55 Amperes RMS)

SILICON CONTROLLED RECTIFIERS

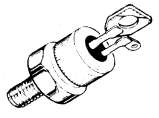
25 thru 100 VOLTS

REVERSE BLOCKING TRIODE THYRISTOR

. . . designed for overvoltage protection in crowbar circuits.

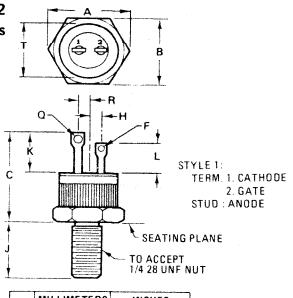
- Glass-Passivated Junctions for Greater Parameter Uniformity and Reliability
- Center-Gate Geometry for Uniform Current Spreading Enabling High Peak Current Capability
- High Capacitor Discharge Current Capability
  850 Amps (MCR70)
  1700 Amps (MCR71)
- Hermetically-Sealed Metal Packages

CASE 175
MCR70 series



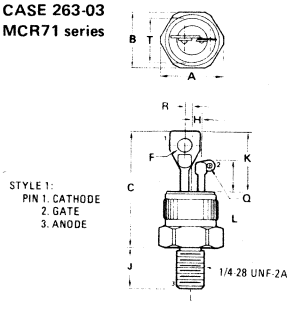
CASE 263
MCR71 series

CASE 175-02
MCR70 series



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	20.70	24.13	0.815	0.950
F	0.89	2.16	0.035	0.085
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	9.78	10.54	0.385	0.415
L	6.99	7.75	0.275	0.305
Q	1.65	4.06	0.065	0.160
R	1.65 REF		0.065 REF	
T	12.70	12.83	0.500	0.505

CASE 263-03
MCR71 series



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.34	15.60	0.604	0.614
B	14.00	14.20	0.551	0.559
C	26.67	30.23	1.050	1.190
F	3.43	4.06	0.135	0.160
H	2.29 REF		0.090 REF	
J	10.67	11.56	0.420	0.455
K	15.75	17.02	0.620	0.670
L	7.62	8.89	0.300	0.350
Q	1.40	2.16	0.055	0.085
R	1.65 REF		0.065 REF	
T	12.73	12.83	0.501	0.505

MAXIMUM RATINGS

Rating	Symbol	MCR70 Value	MCR71 Value	Unit
Repetitive Peak Forward or Reverse Blocking Voltage (Note 1)	V_{DRM} or V_{RRM}			Volts
MCR70,71-1		25		
MCR70,71-2		50		
MCR70,71-3		100		
Peak Discharge Current (Note 2)	I_{TM}	850	1700	Amps
On-State Current ($T_C \leq 75^oC$)	$I_{T(RMS)}$	35	55	Amps
	$I_{T(AV)}$	22	35	
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave, 60 Hz, $T_J = 125^oC$)	I_{TSM}	350	550	Amps
Circuit Fusing ($t \leq 8.3$ ms)	I^2t	510	1255	A^2s
Critical Rate of Rise of Current (Note 3)	di/dt	100	200	A/μs
Forward Peak Gate Power ($t \leq 20\ \mu s$)	P_{GM}	20		Watts
Forward Average Gate Power	$P_{G(AV)}$	0.5		Watts
Forward Peak Gate Current ($t \leq 20\ \mu s$)	I_{GM}	2.0		Amps
Operating Junction Temperature Range	T_J	−40 to +125		^oC
Storage Temperature Range	T_{stg}	−40 to +150		^oC
Mounting Torque	—	30		in.lb.

THERMAL CHARACTERISTIC

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^oC/W$

NOTES:
1. The rated voltage can be applied over the rated operating junction temperatures without incurring damage. Ratings apply for shorted-open or shorted-gate conditions or negative voltage on the gate. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltages.
2. Rating is for t_W = 1.0 ms. See Figure 1 for I_{TM} limits of an exponentially decaying current pulse of various durations.
3. Test Conditions: I_G = 150 mA, V_D = Rated V_{DRM}, I_{TM} = Rated Value, $T_J \leq 125^oC$.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Forward Blocking Current (Note 1) (V_D = Rated V_{DRM}, T_J = 125°C)		I_{DRM}	–	–	2.0	mA
Peak Reverse Blocking Current (V_R = Rated V_{RRM}, T_J = 125°C)		I_{RRM}	–	–	2.0	mA
On-State Voltage (Note 2)		V_{TM}				Volts
(I_{TM} = 70 A)	MCR70 series		–	1.5	1.85	
(I_{TM} = 175 A)	MCR71 series		–	1.7	2.1	
(I_{TM} = 850 A, t_w = 1.0 ms) Note 3	MCR70 series		–	6.0	–	
(I_{TM} = 1700 A, t_w = 1.0 ms) Note 3	MCR71 series		–	7.0	–	
Gate Trigger Current (V_D = 12 V, R_L = 100 Ω)		I_{GT}	2.0	10	30	mA
Gate Trigger Voltage		V_{GT}				Volts
(V_D = 12 V, R_L = 100 Ω)			–	1.0	1.5	
(V_D = Rated V_{DRM}, R_L = 1.0 kΩ, T_J = 125°C)			0.2	–	–	
Holding Current (I_{TM} = 0.5 A, Gate-Open)		I_H	3.0	15	50	mA
Latching Current (V_D = 12 V, I_G = 150 mA, $t_r \leq$ 50 μs)		I_L	–	30	60	mA
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Gate Open, Exponential Waveform, T_C = 125°C)		dv/dt	10	–	–	V/μs
Turn-On Time (Note 3) (V_D = Rated V_{DRM}, I_G = 150 mA)		t_{on}				μs
(I_{TM} = 70 Amps, peak)	MCR70 series		–	1.0	–	
(I_{TM} = 110 Amps, peak)	MCR71 series		–	1.2	–	

NOTES:

1. The rated voltages can be applied over the rated operating junction temperatures without incurring damage. Ratings apply for shorted-open or shorted-gate conditions or negative voltage on the gate. Devices should not be tested for blocking capability in a manner such that the voltage supplied exceeds the rated blocking voltages.
2. Duty Cycle ≤ 1%, Pulse Width ≤ 300 μs.
3. Characteristic applies for t_w = 1.0 ms. t_w is defined as 5 time constants of an exponentially decaying current pulse.
4. The gate controlled turn-on time in a crowbar circuit will be influenced by the circuit inductance.

FIGURE 1 – PEAK CAPACITOR DISCHARGE CURRENT

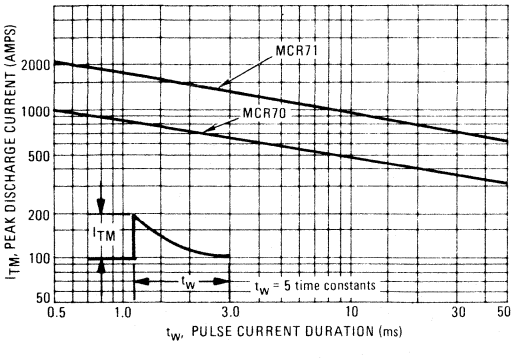


FIGURE 2 – PEAK CAPACITOR DISCHARGE CURRENT DERATING

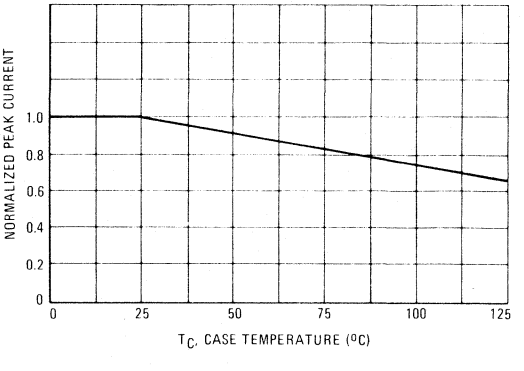


FIGURE 3 – AVERAGE CURRENT DERATING
MCR70

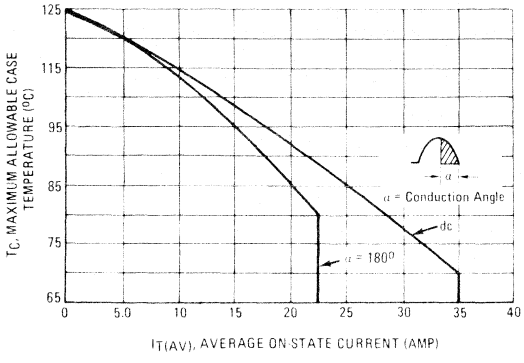


FIGURE 4 – POWER DISSIPATION
MCR70

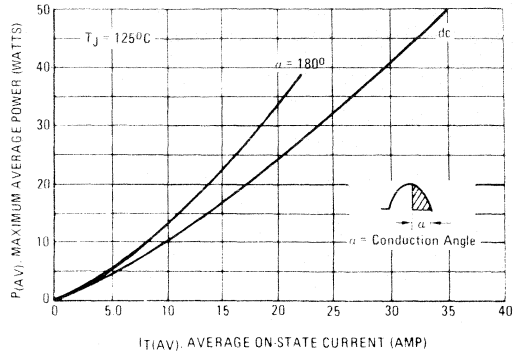


FIGURE 5 – CURRENT DERATING
MCR71

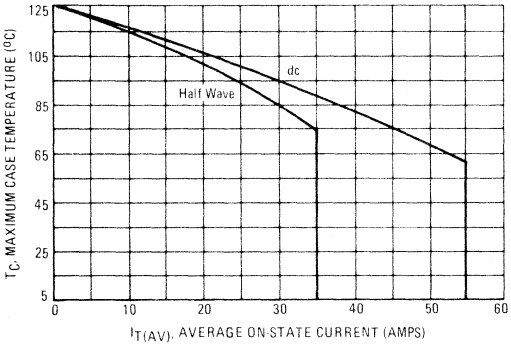


FIGURE 6 – POWER DISSIPATION
MCR71

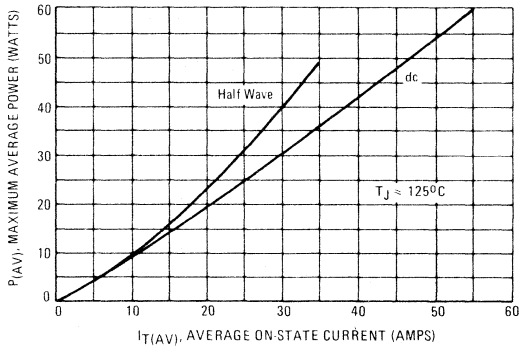


FIGURE 7 – TYPICAL THERMAL RESPONSE

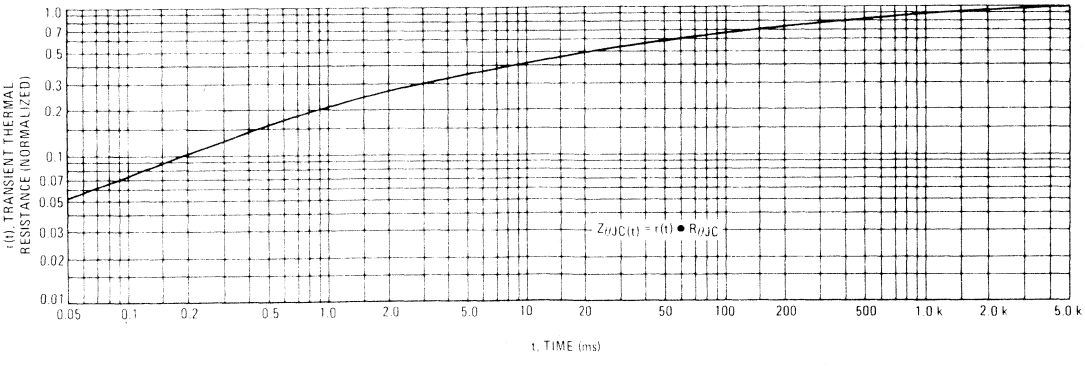


FIGURE 8 – GATE TRIGGER CURRENT

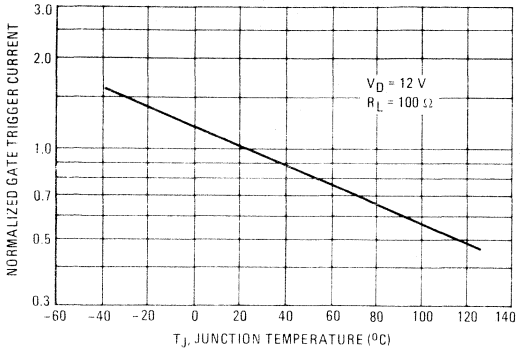


FIGURE 9 – GATE TRIGGER VOLTAGE

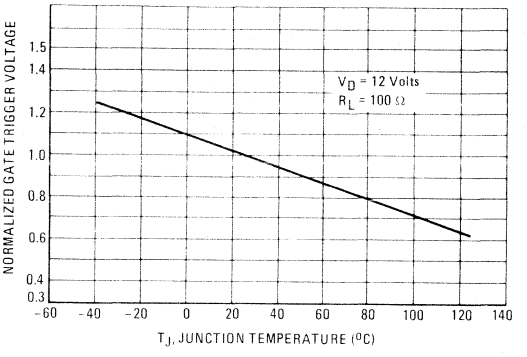
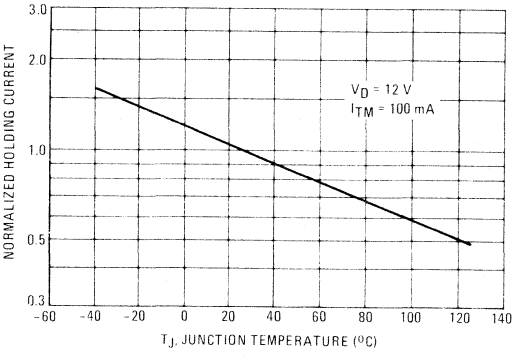


FIGURE 10 – HOLDING CURRENT



MOTOROLA Semiconductors

MJE13002
MJE13003

Designers▲ Data Sheet

1.5 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
40 WATTS

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

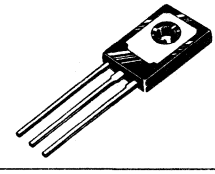
The MJE13002 and MJE13003 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- Reverse Biased SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 0.5 to 1.5 Amp, 25 and 100°C . . . t_c @ 1 A, 100°C is 290 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



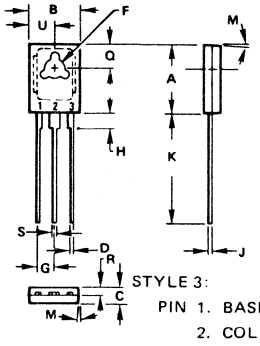
MAXIMUM RATINGS

Rating	Symbol	MJE13002	MJE13003	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	1.5 3		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	0.75 1.5		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	2.25 4.5		Adc
Total Power Dissipation@T_A = 25°C Derate above 25°C	P_D	1.42 11.5		Watts mW/°C
Total Power Dissipation@T_C = 25°C Derate above 25°C	P_D	40 320		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.12	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	88	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.



STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.80	11.05	0.425	0.435
B	7.49	7.75	0.295	0.305
C	2.41	2.67	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.92	3.00	0.115	0.118
G	2.31	2.46	0.091	0.097
H	2.16	2.41	0.085	0.095
J	0.38	0.64	0.015	0.025
K	15.37	16.64	0.605	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.14	1.40	0.045	0.055
S	0.64	0.89	0.025	0.035
U	3.68	3.94	0.145	0.155

CASE 77-03
Similar to TO-126

▲Trademark of Motorola Inc.

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***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS[1]						
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	MJE13002	$V_{CEO(sus)}$	300	–	–	Vdc
	MJE13003		400	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 1			Adc
ON CHARACTERISTICS[1]						
DC Current Gain		h_{FE}				–
(I_C = 0.5 Adc, V_{CE} = 2 Vdc)			8	–	40	
(I_C = 1 Adc, V_{CE} = 2 Vdc)			5	–	25	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 0.5 Adc, I_B = 0.1 Adc)			–	–	0.5	
(I_C = 1 Adc, I_B = 0.25 Adc)			–	–	1	
(I_C = 1.5 Adc, I_B = 0.5 Adc)			–	–	3	
(I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)			–	–	1	
Base-Emitter Sautration Voltage		$V_{BE(sat)}$				Vdc
(I_C = 0.5 Adc, I_B = 0.1 Adc)			–	–	1	
(I_C = 1 Adc, I_B = 0.25 Adc)			–	–	1.2	
(I_C = 1 Adc, I_B = 0.25 Adc, T_C = 100°C)			–	–	1.1	
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C = 100 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	5	10	–	MHz
Output Capacitance (V_{CB} - 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	21	–	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 1 A,	t_d	–	0.05	0.1	μs
Rise Time	I_{B1} = I_{B2} = 0.2 A, t_p - 25 μs,	t_r	–	0.5	1	μs
Storage Time	Duty Cycle ≤ 1%)	t_s	–	2	4	μs
Fall Time		t_f	–	0.4	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Voltage Storage Time	(I_C = 1 A, V_{clamp} = 300 Vdc,	t_{sv}	–	1.7	4	μs
Commutation Time	I_{B1} = 0.2 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.29	0.75	μs

[1] Pulse Test: Pulse width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATION AREA

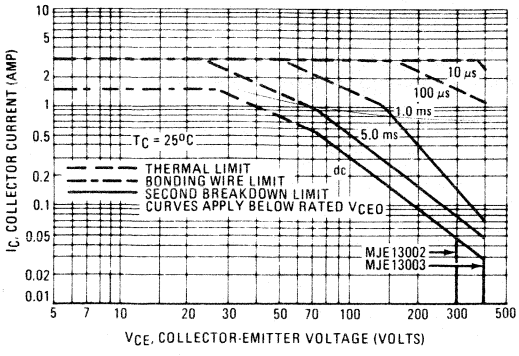
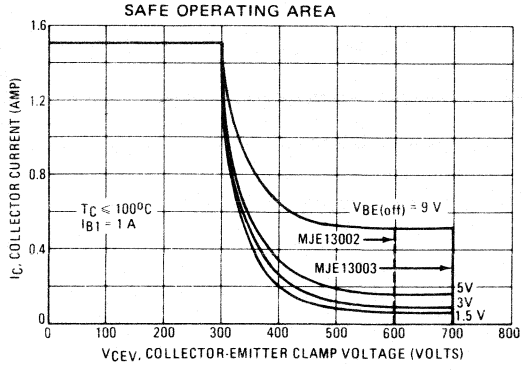
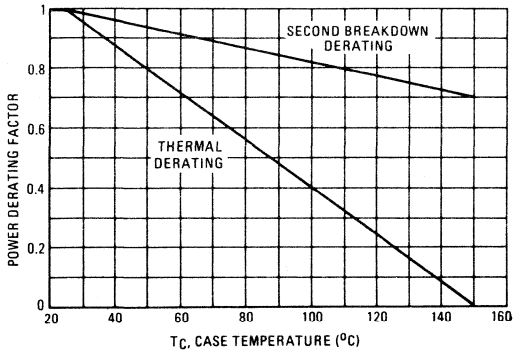


FIGURE 2 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 – FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 2) is discussed in the designer's application section.

FIGURE 4 – THERMAL RESPONSE

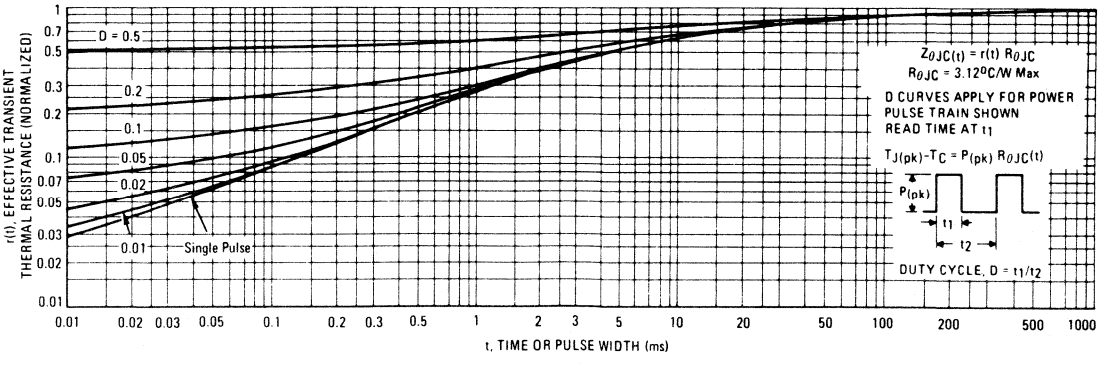


FIGURE 5 – DC CURRENT GAIN

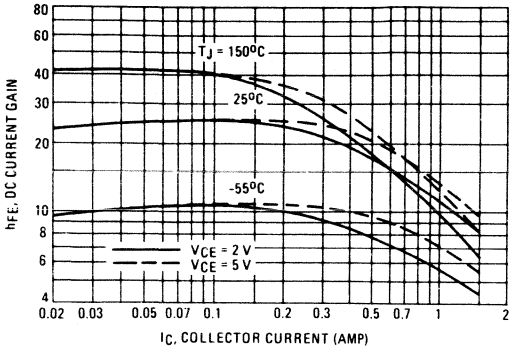


FIGURE 6 – COLLECTOR SATURATION REGION

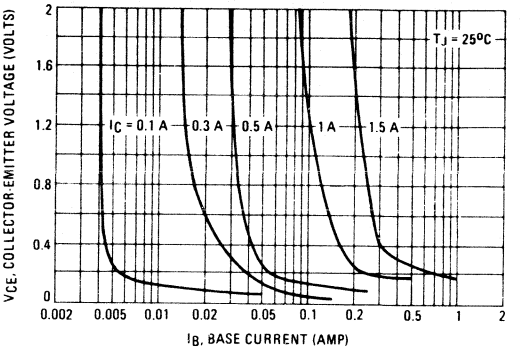


FIGURE 7 – BASE-EMITTER VOLTAGE

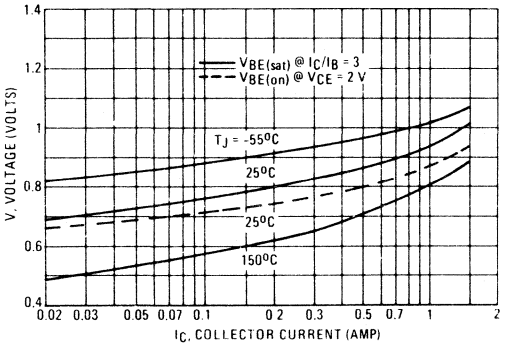


FIGURE 8 – COLLECTOR-EMITTER SATURATION REGION

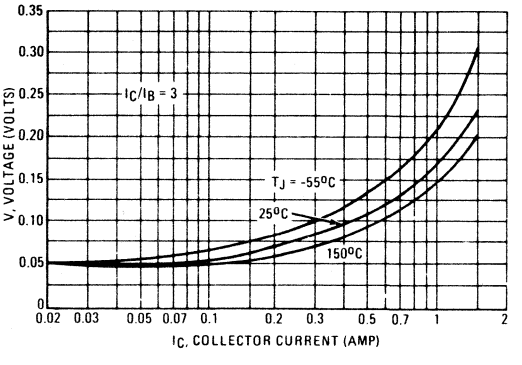


FIGURE 9 – COLLECTOR CUTOFF REGION

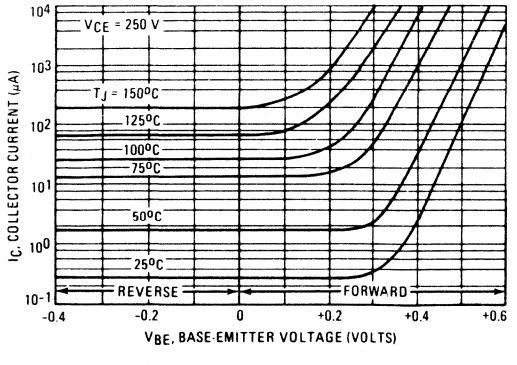


FIGURE 10 – CAPACITANCE

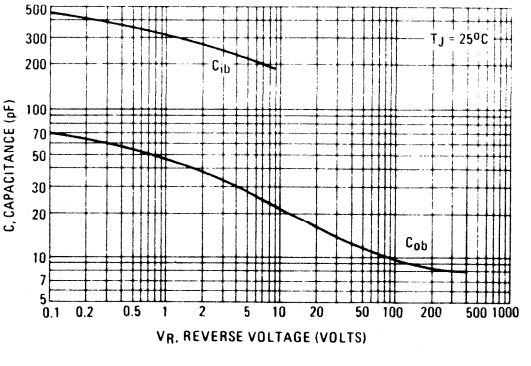
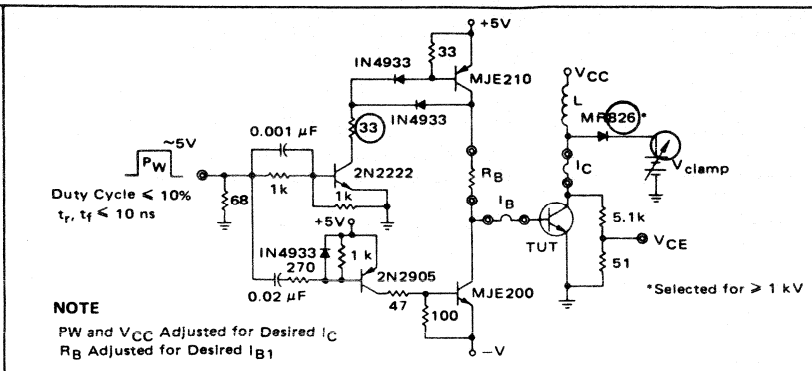
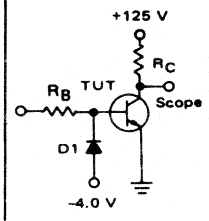
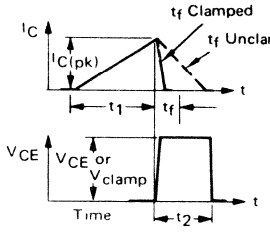
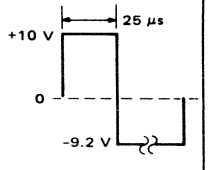


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	R_B SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 **NOTE** PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~200 Turns) #20 GAP for 30 mH/2A L_{coil} = 50 mH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 125 Ω D1 = 1N5820 or Equiv. R_B = 47 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope-Tektronics 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

DESIGNERS INFORMATION FOR APPLICATIONS AND SWITCHMODE▲ SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-588, AN-719, AN-737 and Engineering Bulletin EB-39.

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.
(2) The turn-on time or pulse width does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).
(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 1 ampere which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

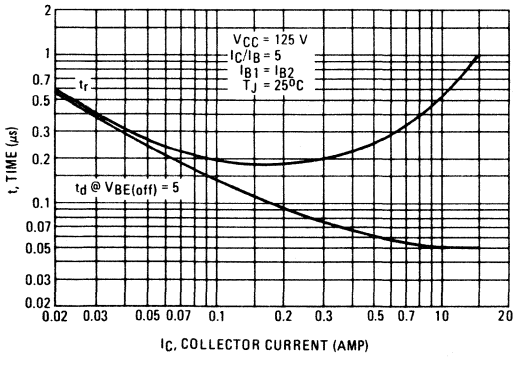


FIGURE 12 – TURN-OFF TIME

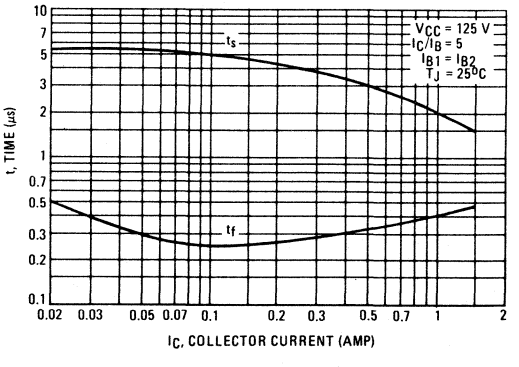


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

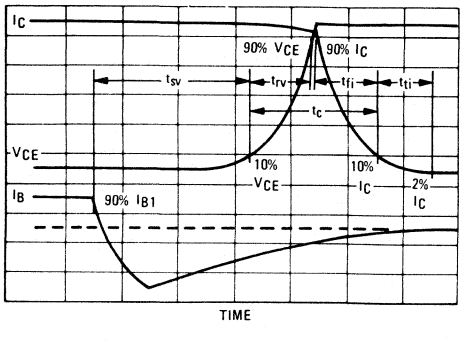


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS
(at 300 V and 1 A with I_{B1} = 0.2 A and $V_{BE(off)}$ = 5.0 V)

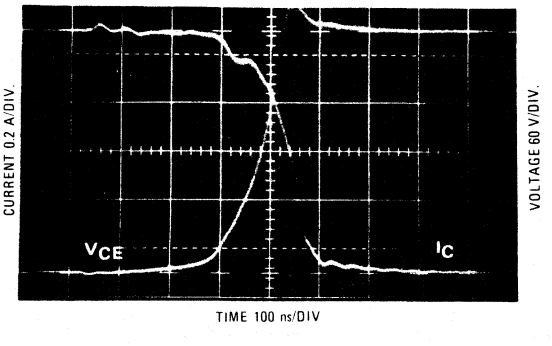


TABLE 2 — APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

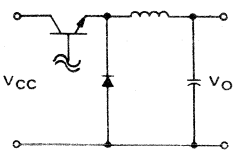
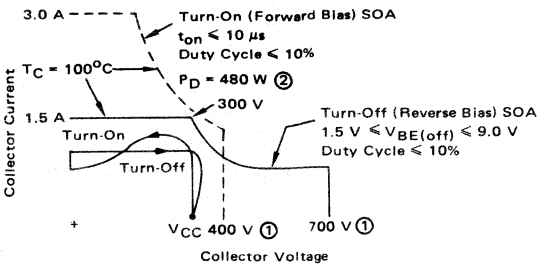
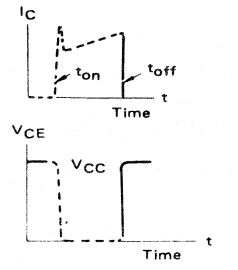
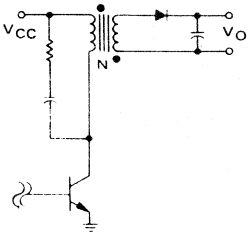
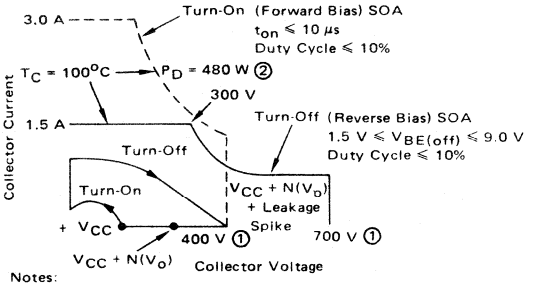
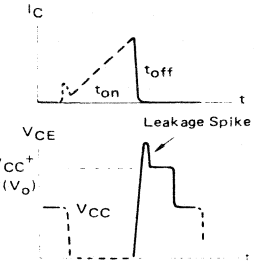
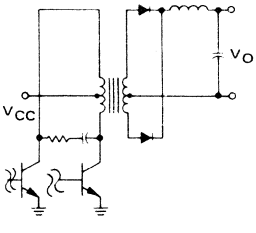
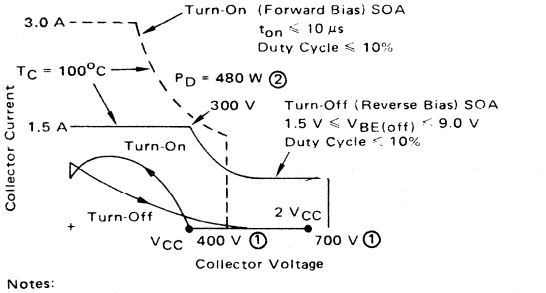
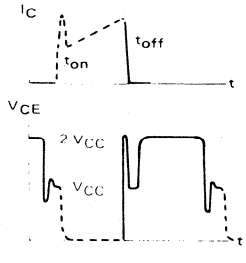
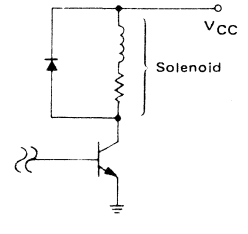
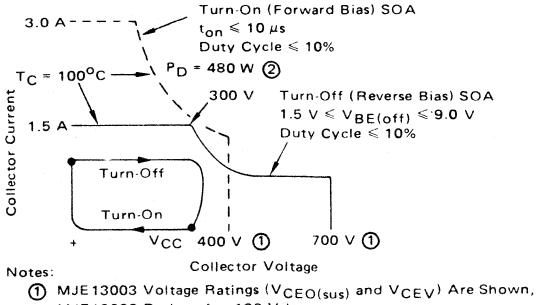
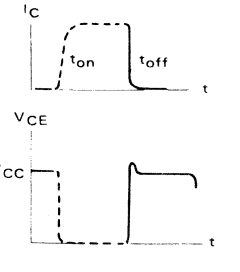
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13002 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
B	**RINGING CHOKE INVERTER** 	 Notes: ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown. MJE13002 Ratings Are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure	
C	**PWM PUSH-PULL INVERTER/CONVERTER** 	 Notes: ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13002 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: ① MJE13003 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13002 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} μs	t_{rv} μs	t_{fi} μs	t_{ti} μs	t_c μs
0.5	25	1.3	0.23	0.30	0.35	0.30
	100	1.6	0.26	0.30	0.40	0.36
1	25	1.5	0.10	0.14	0.05	0.16
	100	1.7	0.13	0.26	0.06	0.29
1.5	25	1.8	0.07	0.10	0.05	0.16
	100	3	0.08	0.22	0.08	0.28

NOTE: All Data Recorded in the Inductive Switching Circuit in Table 1

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{CE}
t_{rv} = Voltage Rise Time, 10-90% V_{CE}
t_{fi} = Current Fall Time, 90-10% I_C
t_{ti} = Current Tail, 10-2% I_C
t_c = Commutation Time, 10% V_{CE} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the commutation interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

TO-126 MOUNTING NOTE (CASE 77)

The preferred mounting technique for high-voltage applications is to direct mount the transistor and to insulate the heat sink. However, if the transistor must be insulated from the heat sink, a 4-40 screw with a compression washer and a 3 mil mica washer with grease (DC340) can be used to mount these TO-126 transistors. Typical hi-pot readings from the collector to this mounting hardware are 500 V dry and 1500 V with grease. For added safety, an insulated screw may be used.

MOTOROLA Semiconductors

MJE13004
MJE13005

Designers▲ Data Sheet

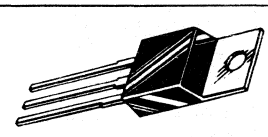
SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJE13004 and MJE13005 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switchmode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 2 to 4 Amp, 25 and 100°C
  . . . t_c @ 3A, 100°C is 180 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information.

4 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
75 WATTS



Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

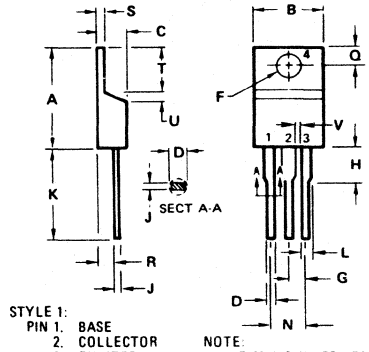
MAXIMUM RATINGS

Rating	Symbol	MJE13004	MJE13005	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	4 8		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2 4		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	6 12		Adc
Total Power Dissipation@T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation@T_C = 25°C Derate above 25°C	P_D	75 600		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14	-	0.045	-

CASE 221A-02
TO-220AB

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DS 3334

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
•OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	MJE13004	$V_{CEO(sus)}$	300	–	–	Vdc
	MJE13005		400	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$		See Figure 1		
Clamped Inductive SOA with Base Reverse Biased		–		See Figure 2		
•ON CHARACTERISTICS						
DC Current Gain		h_{FE}				–
(I_C = 1 Adc, V_{CE} = 5 Vdc)			10	–	60	
(I_C = 2 Adc, V_{CE} = 5 Vdc)			8	–	40	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)			–	–	0.5	
(I_C = 2 Adc, I_B = 0.5 Adc)			–	–	0.6	
(I_C = 4 Adc, I_B = 1 Adc)			–	–	1	
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)			–	–	1	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 1 Adc, I_B = 0.2 Adc)			–	–	1.2	
(I_C = 2 Adc, I_B = 0.5 Adc)			–	–	1.6	
(I_C = 2 Adc, I_B = 0.5 Adc, T_C = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	65	–	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 2 A,	t_d	–	0.025	0.1	μs
Rise Time	I_{B1} = I_{B2} = 0.4 A, t_p = 25 μs,	t_r	–	0.3	0.7	μs
Storage Time	Duty Cycle ≤ 1%)	t_s	–	1.7	3.5	μs
Fall Time		t_f	–	0.4	0.9	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Voltage Storage Time	(I_C = 2 A, V_{clamp} = 300 Vdc,	t_{sv}	–	0.9	2.3	μs
Crossover Time	I_{B1} = 0.4 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.32	0.9	μs

•Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA

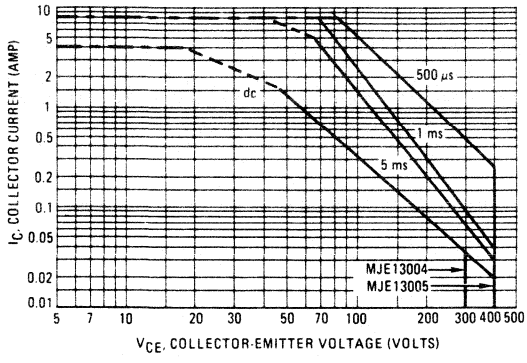
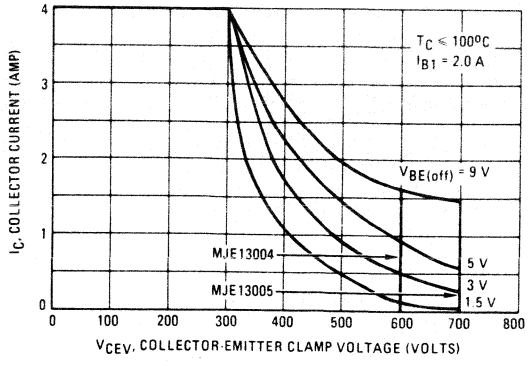
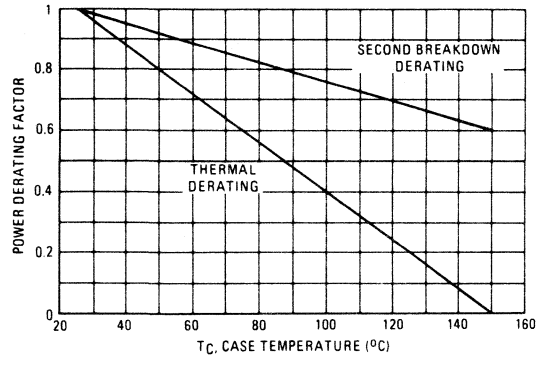


FIGURE 2 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 – FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

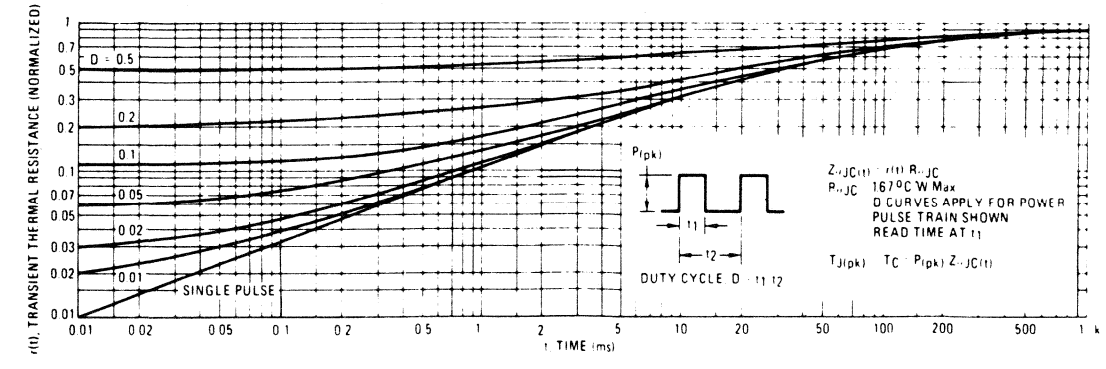


FIGURE 5 – DC CURRENT GAIN

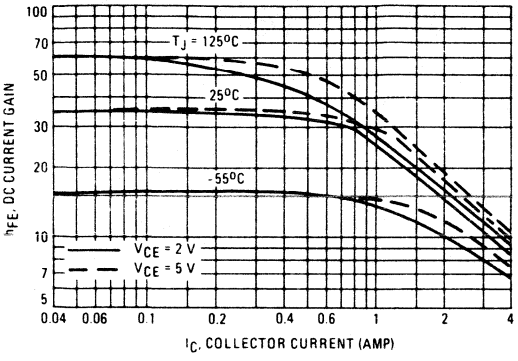


FIGURE 6 – COLLECTOR SATURATION REGION

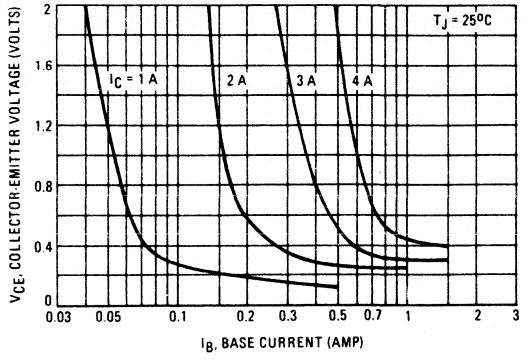


FIGURE 7 – BASE-EMITTER VOLTAGE

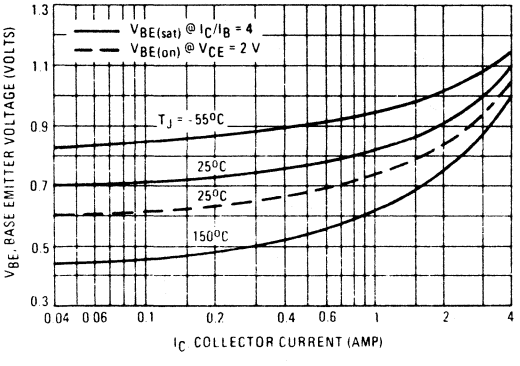


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

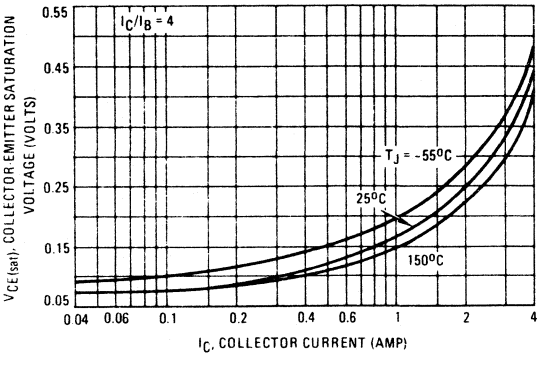


FIGURE 9 – COLLECTOR CUTOFF REGION

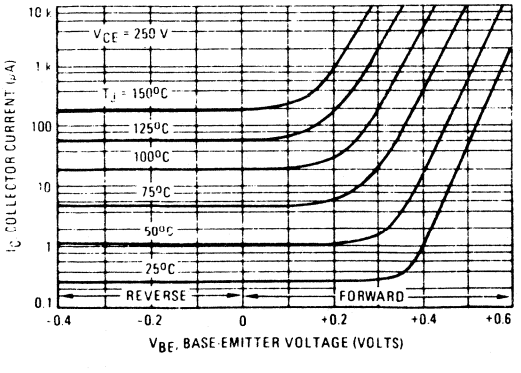


FIGURE 10 – CAPACITANCE

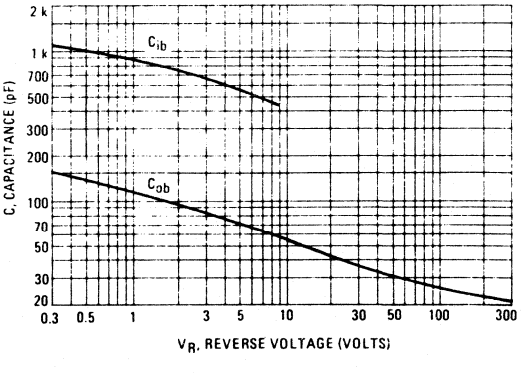
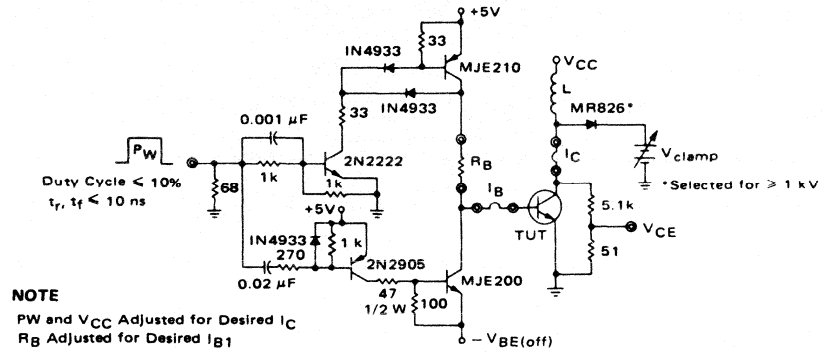
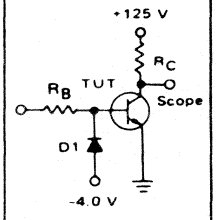
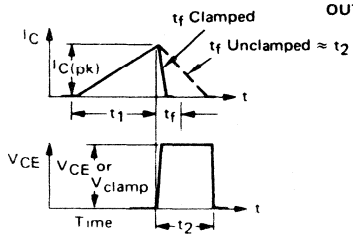
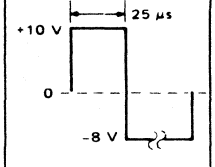


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS	 **NOTE** PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}	
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 µH/20A L_{coil} = 200 µH V_{CC} = 20 V V_{clamp} = 300 Vdc	V_{CC} = 125 V R_C = 62 Ω D1 = 1N5820 or Equiv R_B = 22 Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	 t_r, t_f < 10 ns Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C

APPLICATIONS INFORMATION FOR SWITCHMODE▲ SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737, AN-767, AN-752 and Engineering Bulletins EB-39, EB-65.

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).

(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

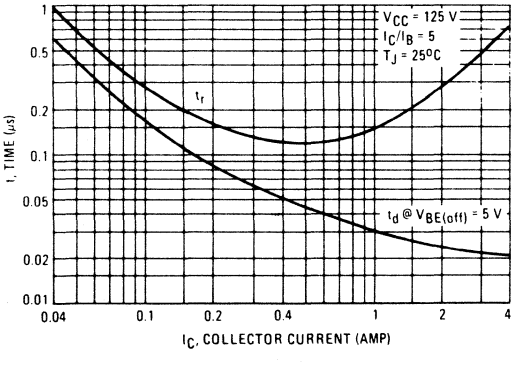


FIGURE 12 – TURN-OFF TIME

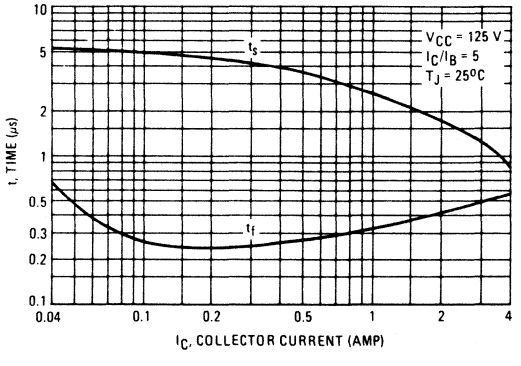


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

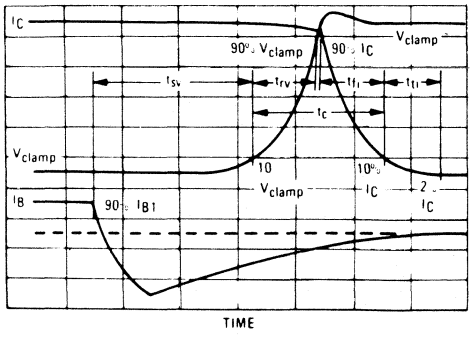


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS
(at 300 V and 4 A with I_{B1} = 0.8 A and $V_{BE(off)}$ = 5.0 V)

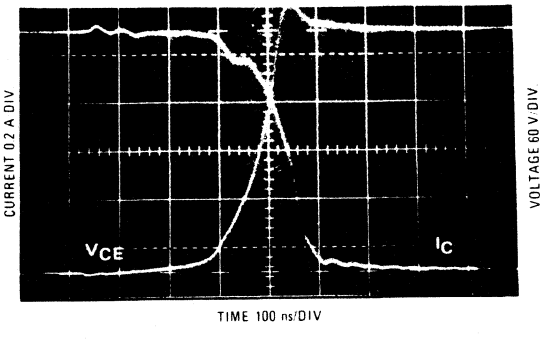


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

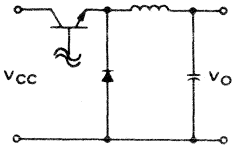
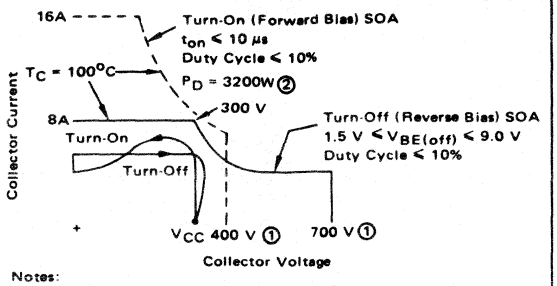
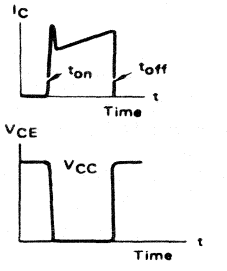
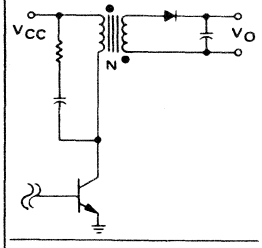
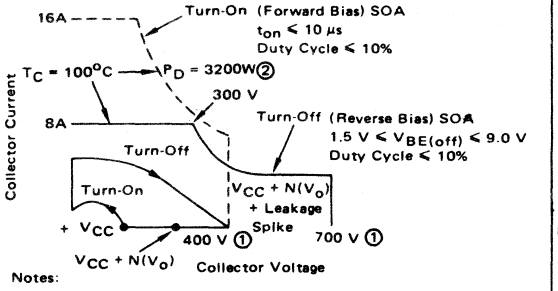
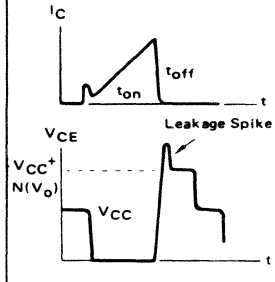
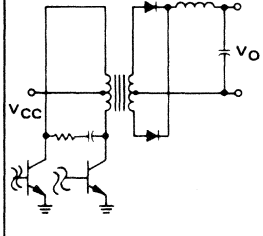
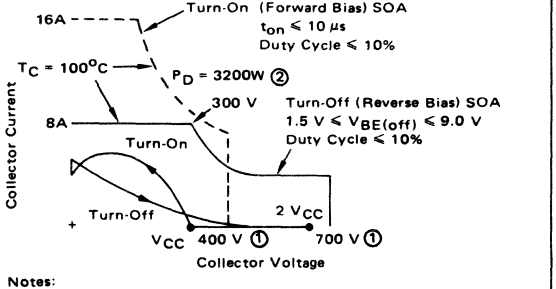
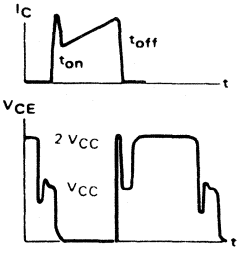
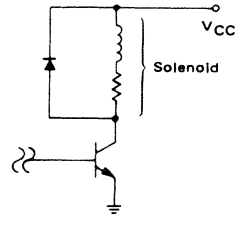
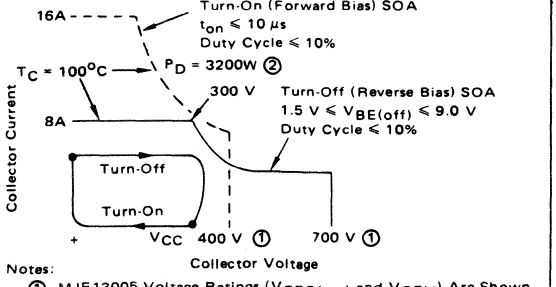
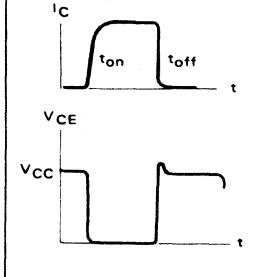
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: ① MJE13005 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13004 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
B	**RINGING CHOKE INVERTER** 	 Notes: ① MJE13005 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown. MJE13004 Ratings Are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure	
C	**PUSH-PULL INVERTER/CONVERTER** 	 Notes: ① MJE13005 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13004 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: ① MJE13005 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13004 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
2	25	600	70	100	80	180
	100	900	110	240	130	320
3	25	650	60	140	60	200
	100	950	100	330	100	350
4	25	550	70	160	100	220
	100	850	110	350	160	390

NOTE: All Data recorded in the Inductive Switching Circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

MOTOROLA Semiconductors

MJE13006
MJE13007

Designers▲ Data Sheet

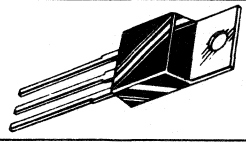
8 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
80 WATTS

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJE13006 and MJE13007 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switch-mode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 8 Amp, 25 and 100°C . . . t_c @ 5A, 100°C is 136 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.



Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

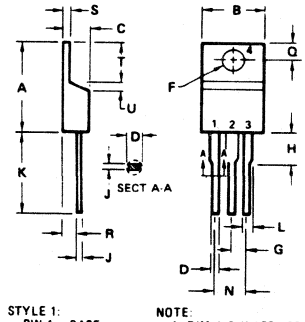
MAXIMUM RATINGS

Rating	Symbol	MJE13006	MJE13007	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	8 16		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	4 8		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	12 24		Adc
Total Power Dissipation@T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation@T_C = 25°C Derate above 25°C	P_D	80 640		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.56	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

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DS3315

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**					
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0) MJE13006 / MJE13007	$V_{CEO(sus)}$	300 / 400	– / –	– / –	Vdc
Collector Cutoff Current	I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		–	–	1	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)		–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)	I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased	$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased	–	See Figure 2			
***ON CHARACTERISTICS**					
DC Current Gain	h_{FE}				–
(I_C = 2 Adc, V_{CE} = 5 Vdc)		8	–	40	
(I_C = 5 Adc, V_{CE} = 5 Vdc)		6	–	30	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)		–	–	1	
(I_C = 5 Adc, I_B = 1 Adc)		–	–	1.5	
(I_C = 8 Adc, I_B = 2 Adc)		–	–	3	
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)		–	–	2	
Base-Emitter Saturation Voltage	$V_{BE(sat)}$				Vdc
(I_C = 2 Adc, I_B = 0.4 Adc)		–	–	1.2	
(I_C = 5 Adc, I_B = 1 Adc)		–	–	1.6	
(I_C = 5 Adc, I_B = 1 Adc, T_C = 100°C)		–	–	1.5	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	110	–	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time (V_{CC} = 125 Vdc, I_C = 5 A, I_{B1} = I_{B2} = 1 A, t_p = 25 μs, Duty Cycle ≤ 1%)	t_d	–	0.05	0.1	μs
Rise Time	t_r	–	0.5	1	μs
Storage Time	t_s	–	1	3	μs
Fall Time	t_f	–	0.15	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)					
Voltage Storage Time (I_C = 5 A, V_{clamp} = 300 Vdc, I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	0.86	2.3	μs
Crossover Time	t_c	–	0.14	0.7	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA

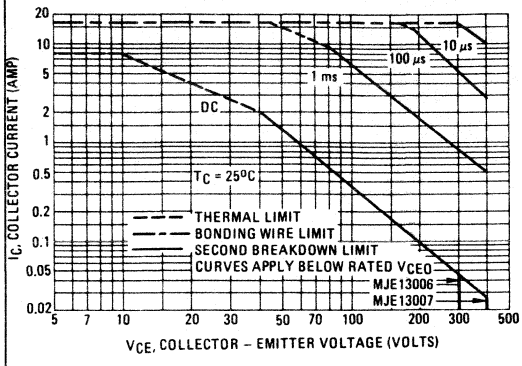
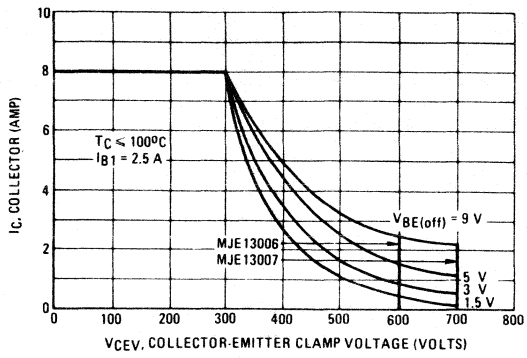
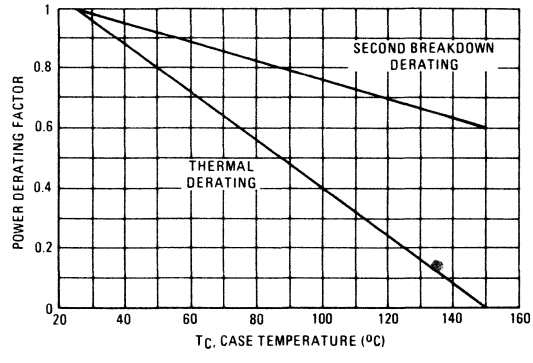


FIGURE 2 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 – FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

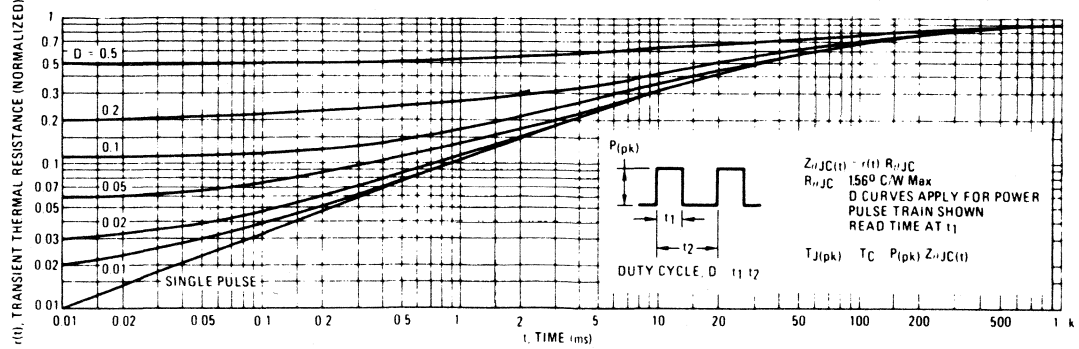


FIGURE 5 –DC CURRENT GAIN

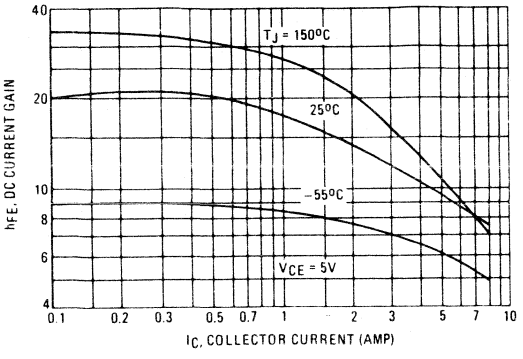


FIGURE 6 – COLLECTOR SATURATION REGION

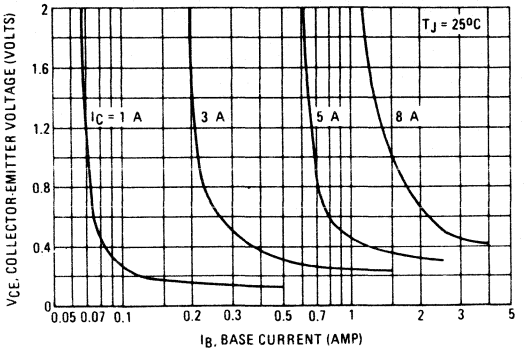


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE

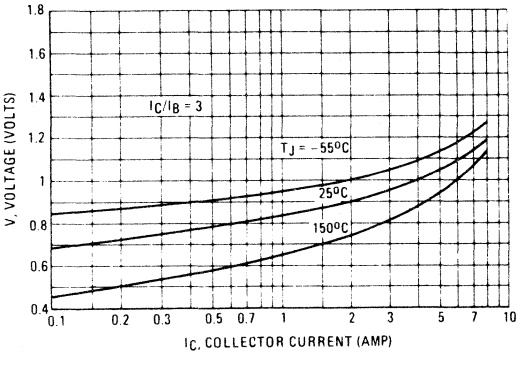


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

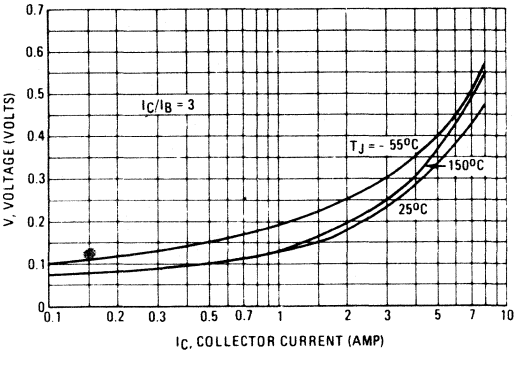


FIGURE 9 – COLLECTOR CUTOFF REGION

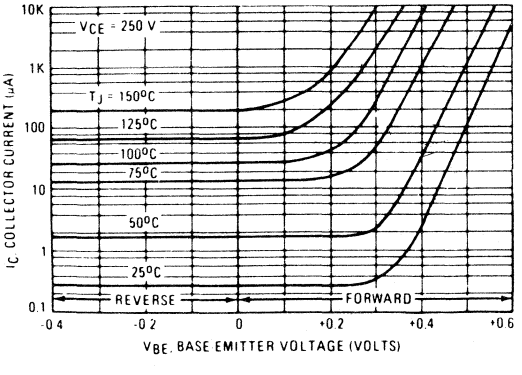


FIGURE 10 – CAPACITANCE

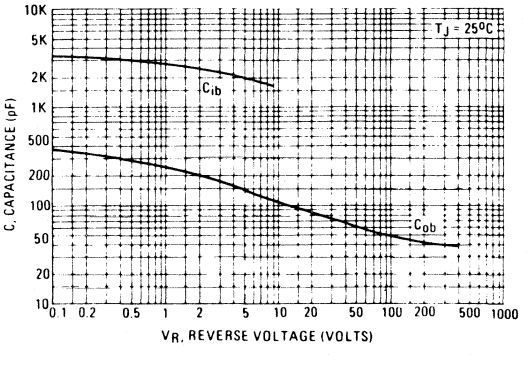
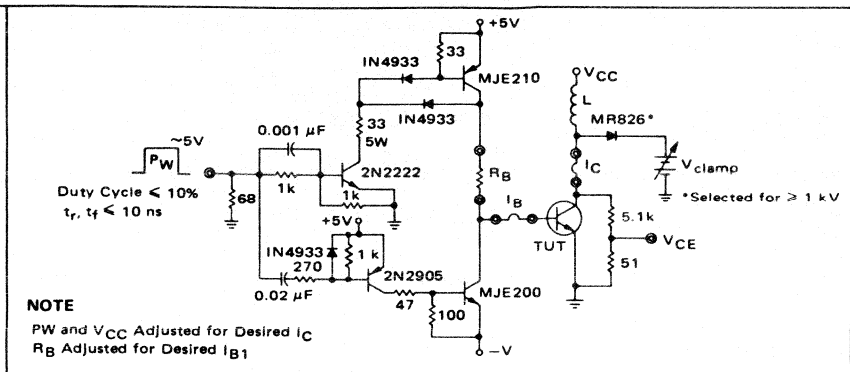
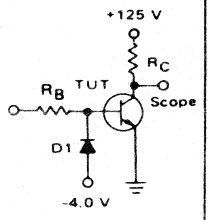
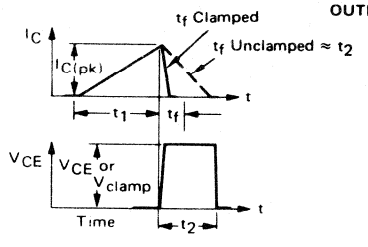
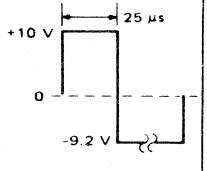


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 μH/20A Lcoil = 200 μH VCC = 20 V Vclamp = 300 Vdc	VCC = 125 V RC = 24.7 Ω D1 = 1N5820 or Equiv. RB = 10Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t1 Adjusted to Obtain IC $t_1 \approx \frac{L_{coil}(I_{Cpk})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{Cpk})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	 tr, tf < 10 ns Duty Cycle = 1.0% RB and RC adjusted for desired IB and IC

APPLICATIONS INFORMATION FOR SWITCHMODE▲ SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737, AN-767, AN-752 and Engineering Bulletins EB-39, EB-65.

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).

(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 5 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

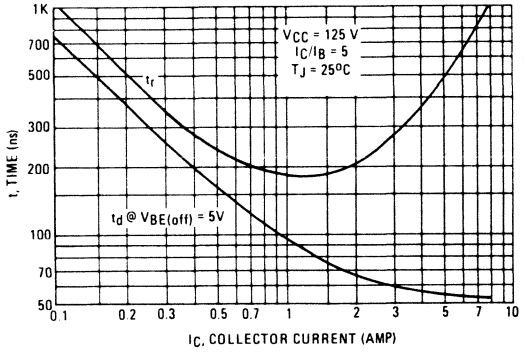


FIGURE 12 – TURN-OFF TIME

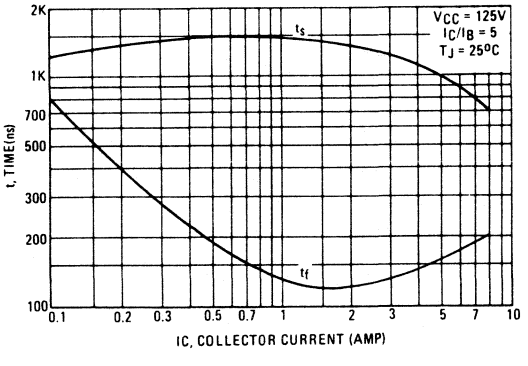


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

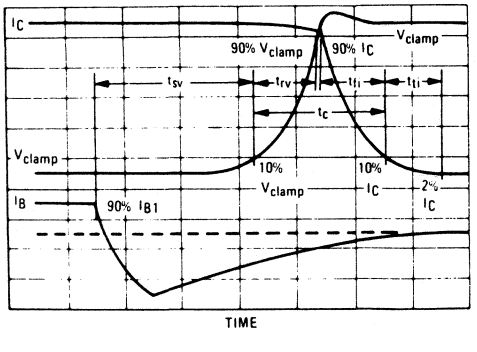


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS
(at 300 V and 8A with I_{B1} = 1.6A and $V_{BE(off)}$ = 5 V)

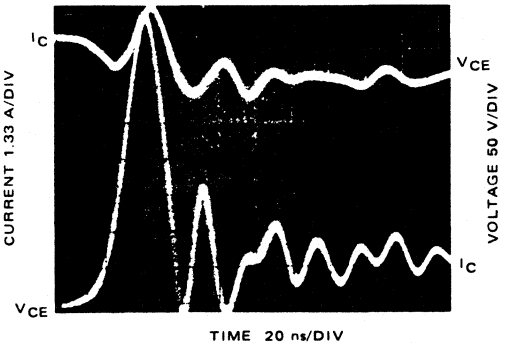


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

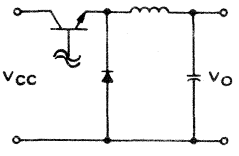
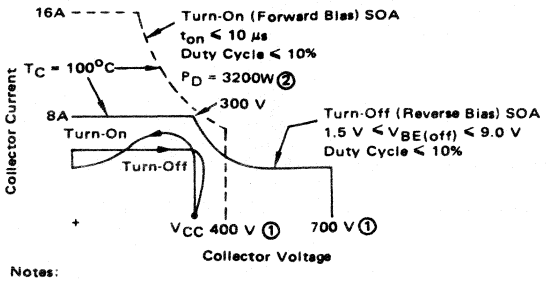
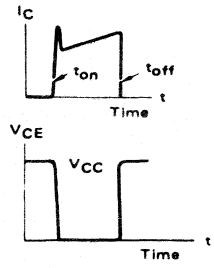
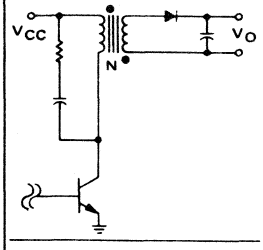
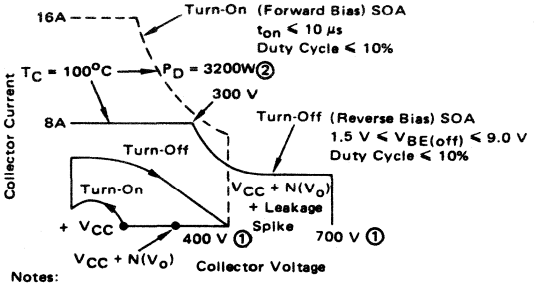
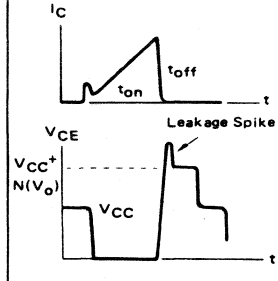
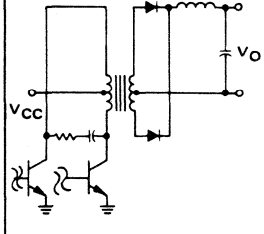
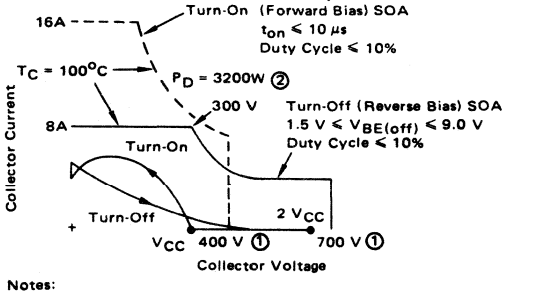
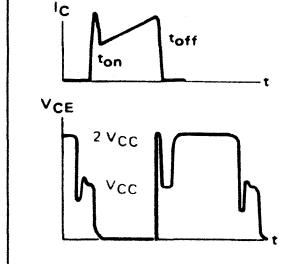
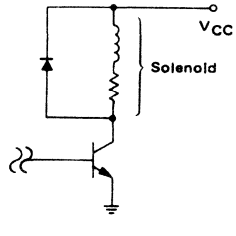
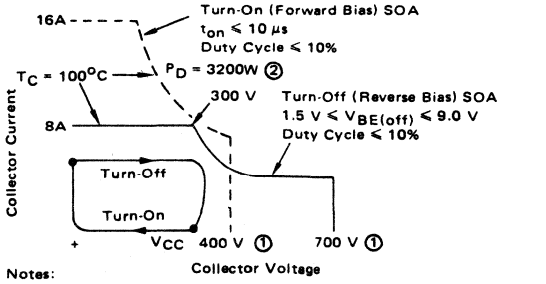
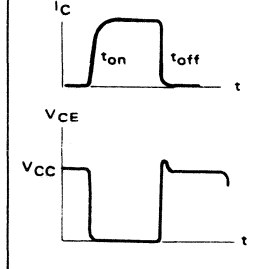
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are Shown, MJE13006 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
B	**RINGING CHOKE INVERTER** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown. MJE13006 Ratings Are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure	
C	**PUSH-PULL INVERTER/CONVERTER** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: ① MJE13007 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) Are Shown, MJE13006 Ratings Are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25	730	115	100	110	200
	100	1000	150	100	150	250
5	25	600	60	23	4	85
	100	860	84	50	10	136
8	25	650	25	26	4	42
	100	880	52	80	20	160

NOTE: All Data recorded in the inductive Switching Circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

MOTOROLA Semiconductors

MJE13008
MJE13009

Designers▲ Data Sheet

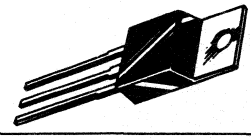
12 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
100 WATTS

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJE13008 and MJE13009 are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V switchmode applications such as Switching Regulators, Inverters, Motor Controls, Solenoid/Relay drivers and Deflectioncircuits.

SPECIFICATION FEATURES:

- $V_{CEO(sus)}$ 400 V and 300 V
- Reverse Bias SOA with Inductive Loads @ T_C = 100°C
- Inductive Switching Matrix 3 to 12 Amp, 25 and 100°C ... t_c @ 8 A, 100°C is 120 ns (Typ).
- 700 V Blocking Capability
- SOA and Switching Applications Information.



Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

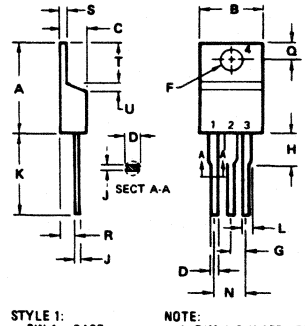
MAXIMUM RATINGS

Rating	Symbol	MJE13008	MJE13009	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EBO}	9		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	12 24		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	6 12		Adc
Emitter Current — Continuous — Peak (1)	I_E I_{EM}	18 36		Adc
Total Power Dissipation@T_A = 25°C Derate above 25°C	P_D	2 16		Watts mW/°C
Total Power Dissipation@T_C = 25°C Derate above 25°C	P_D	100 800		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

NOTE:
1. DIM. L & H APPLIES TO ALL LEADS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.78	10.03	0.385	0.395
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.27	0.045	0.050
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.14	1.39	0.045	0.055
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050

CASE 221A-02
TO-220AB

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
***OFF CHARACTERISTICS**						
Collector-Emitter Sustaining Voltage (I_C = 10 mA, I_B = 0)	MJE13008	$V_{CEO(sus)}$	300	–	–	Vdc
	MJE13009		400	–	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	–	1	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	–	5	
Emitter Cutoff Current (V_{EB} = 9 Vdc, I_C = 0)		I_{EBO}	–	–	1	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 1			
Clamped Inductive SOA with Base Reverse Biased		–	See Figure 2			
***ON CHARACTERISTICS**						
DC Current Gain (I_C = 5 Adc, V_{CE} = 5 Vdc)		h_{FE}	8	–	40	–
(I_C = 8 Adc, V_{CE} = 5 Vdc)			6	–	30	
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1Adc)		$V_{CE(sat)}$	–	–	1	Vdc
(I_C = 8 Adc, I_B = 1.6 Adc)			–	–	1.5	
(I_C = 12 Adc, I_B = 3 Adc)			–	–	3	
(I_C = 8 Adc. I_B = 1.8 Adc, T_C = 100°C)			–	–	2	
Base-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc)		$V_{BE(sat)}$	–	–	1.2	Vdc
(I_C = 8 Adc, I_B = 1.6 Adc)			–	–	1.6	
(I_C = 8 Adc, I_B = 1.6 Adc, T_C = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f = 1 MHz)		f_T	4	–	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	–	180	–	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 125 Vdc, I_C = 8 A,	t_d	–	0.06	0.1	μs
Rise Time	I_{B1} = I_{B2} = 1.6 A, t_p = 25 μs,	t_r	–	0.45	1	μs
Storage Time	Duty Cycle ≤ 1%)	t_s	–	1.3	3	μs
Fall Time		t_f	–	0.2	0.7	μs
Inductive Load, Clamped (Table 1, Figure 13)						
Voltage Storage Time	(I_C = 8 A, V_{clamp} = 300 Vdc,	t_{sv}	–	0.92	2.3	μs
Crossover Time	I_{B1} = 1.6 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.12	0.7	μs

*Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

FIGURE 1 – FORWARD BIAS SAFE OPERATING AREA

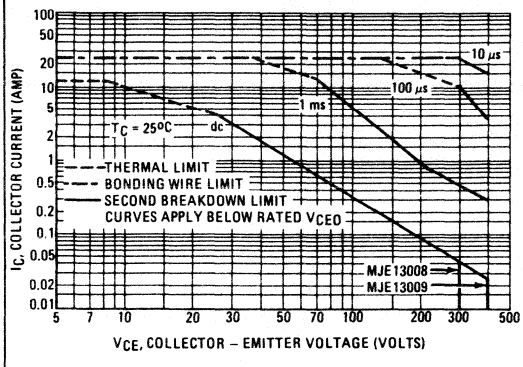
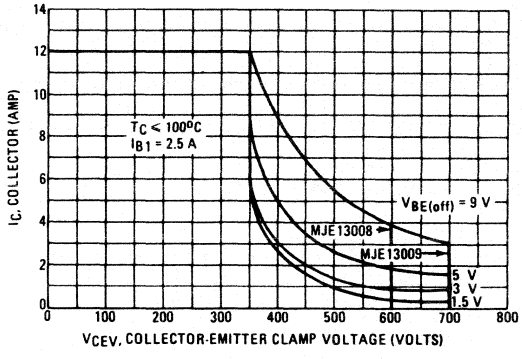
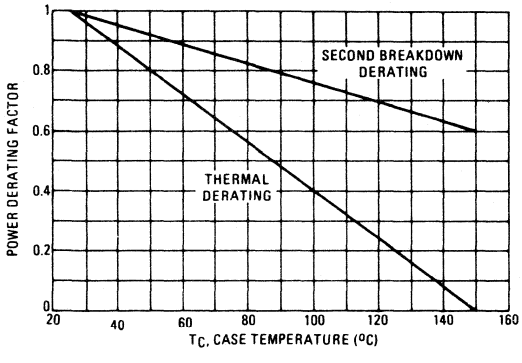


FIGURE 2 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



The Safe Operating Area figures shown in Figures 1 and 2 are specified ratings for these devices under the test conditions shown.

FIGURE 3 – FORWARD BIAS POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 1 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 1 may be found at any case temperature by using the appropriate curve on Figure 3.

$T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Use of reverse biased safe operating area data (Figure 2) is discussed in the applications information section.

FIGURE 4 – TYPICAL THERMAL RESPONSE [$Z_{\theta JC}(t)$]

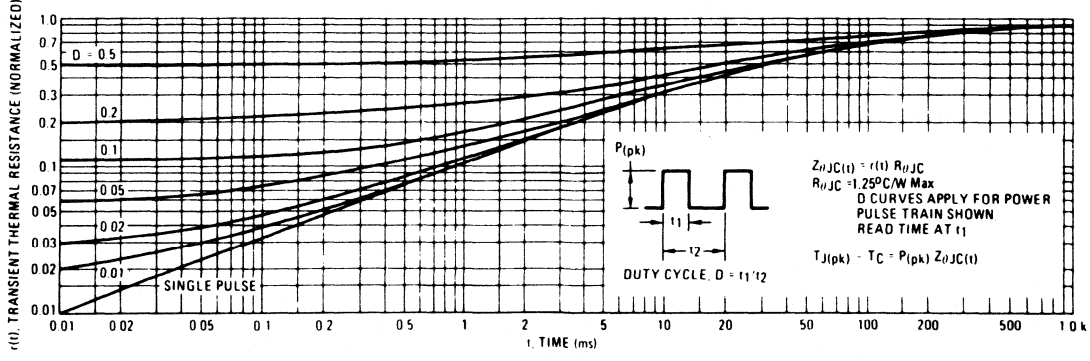


FIGURE 5 –DC CURRENT GAIN

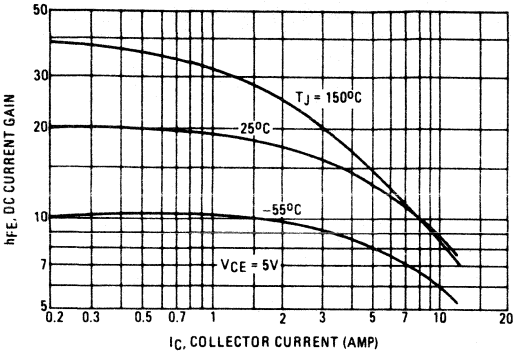


FIGURE 6 – COLLECTOR SATURATION REGION

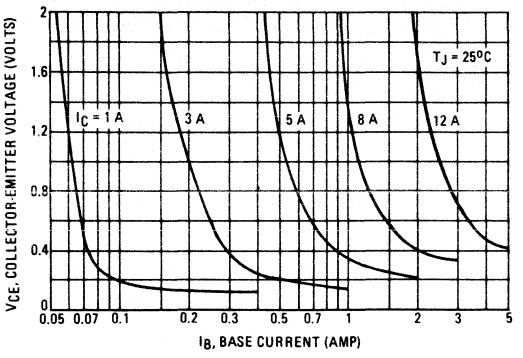


FIGURE 7 – BASE-EMITTER SATURATION VOLTAGE

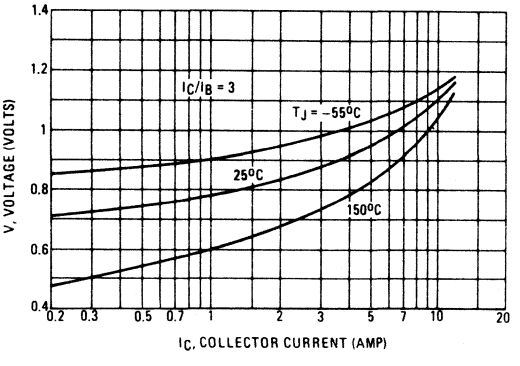


FIGURE 8 – COLLECTOR-EMITTER SATURATION VOLTAGE

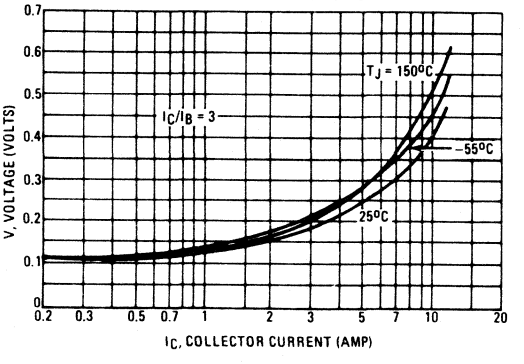


FIGURE 9 – COLLECTOR CUTOFF REGION

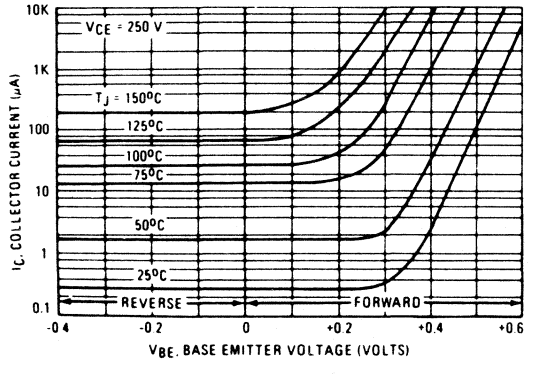


FIGURE 10 – CAPACITANCE

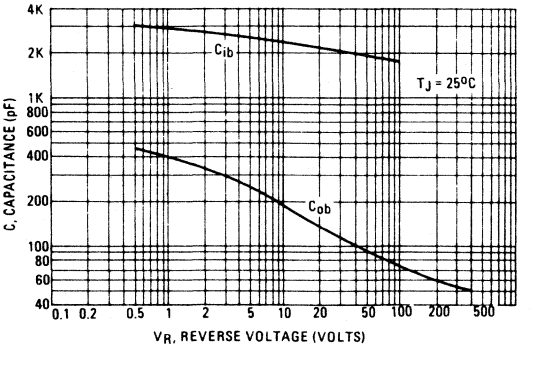
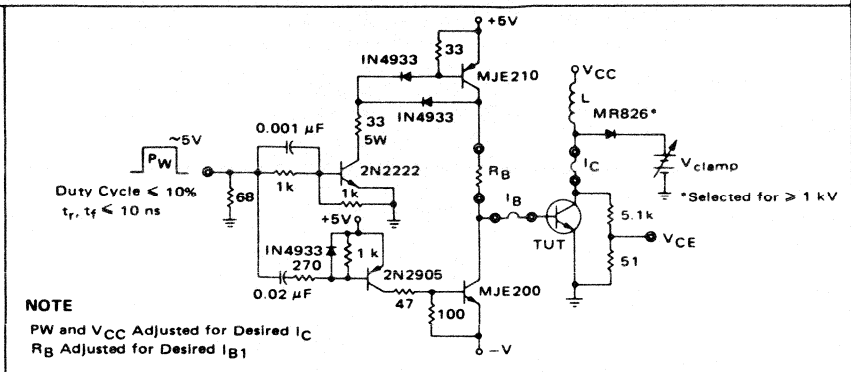
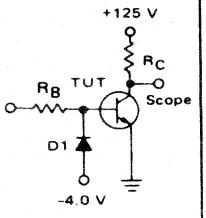
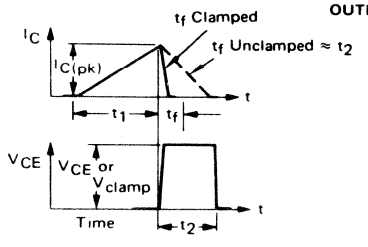
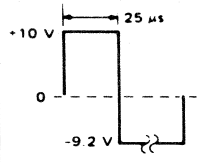


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
TEST CIRCUITS		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 µH/20A Lcoil = 200 µH VCC = 20 V Vclamp = 300 Vdc	VCC = 125 V RC = 15.4 Ω D1 = 1N5820 or Equiv RB = 5Ω
TEST WAVEFORMS	OUTPUT WAVEFORMS  t1 Adjusted to Obtain IC $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	 tr, tf < 10 ns Duty Cycle = 10% RB and RC adjusted for desired IB and IC

APPLICATIONS INFORMATION FOR SWITCHMODE ▲ SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for SWITCHMODE applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in SWITCHMODE applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 1) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as a Reverse Bias Safe Operating Area (Figure 2) which represents voltage-current conditions that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves.

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-719, AN-737, AN-767, AN-752 and Engineering Bulletins EB-39, EB-65.

VOLTAGE REQUIREMENTS (continued)

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output rectifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to keep the turn-off load line within the Reverse Bias SOA curve.

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.
(2) The turn-on time does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 1).
(3) The base drive conditions are within the specified limits shown on the Reverse Bias SOA curve (Figure 2).

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 8 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_{fi}). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 11 and Table 3 and resistive loads in Figures 13 and 14. Usually the inductive load component will be the dominant factor in SWITCHMODE applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 11 – TURN-ON TIME

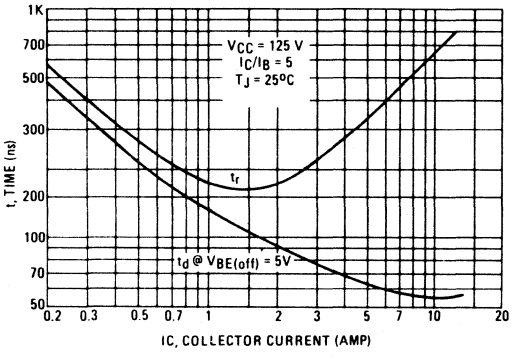


FIGURE 12 – TURN-OFF TIME

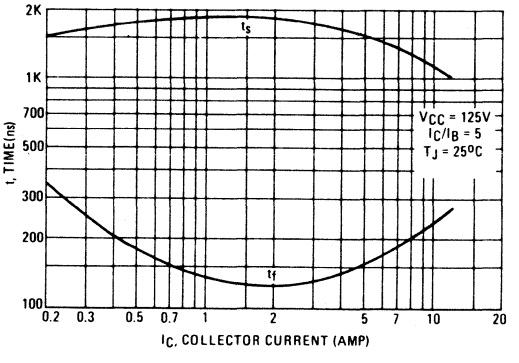


FIGURE 13 – INDUCTIVE SWITCHING MEASUREMENTS

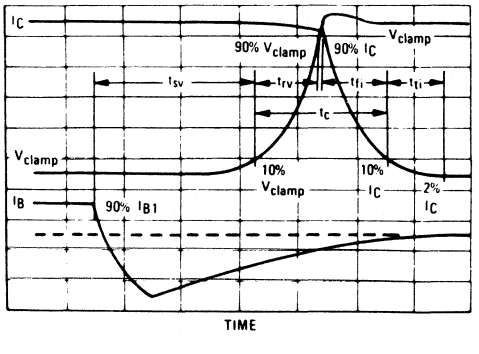


FIGURE 14 – TYPICAL INDUCTIVE SWITCHING WAVEFORMS
(at 300 V and 12 A with I_{B1} = 2.4 A and $V_{BE(off)}$ = 5 V)

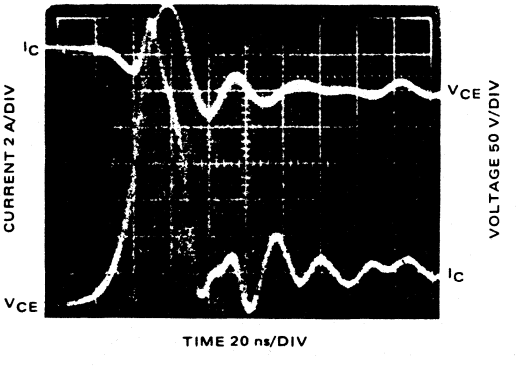


TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

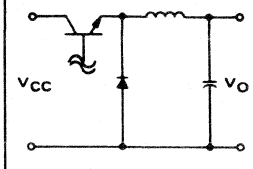
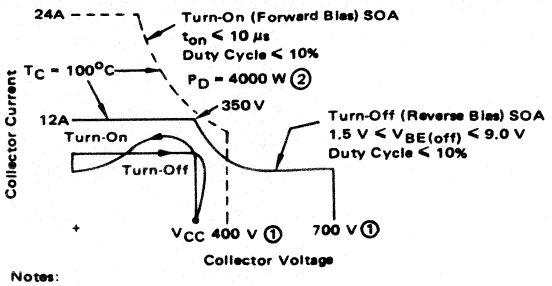
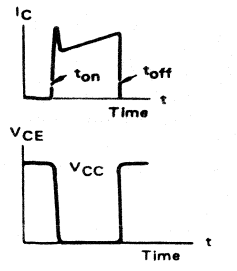
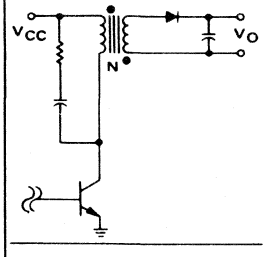
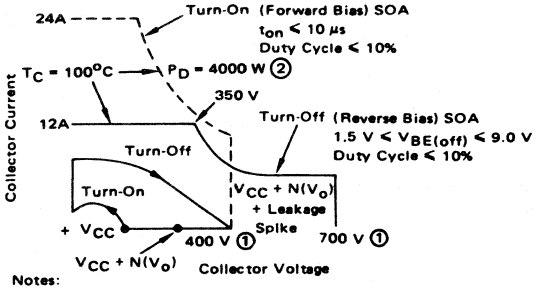
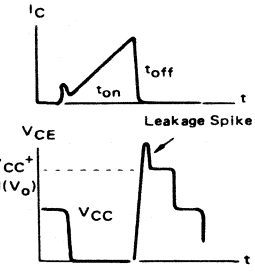
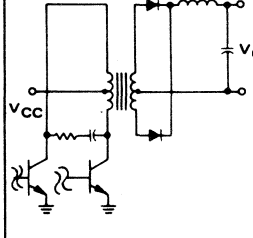
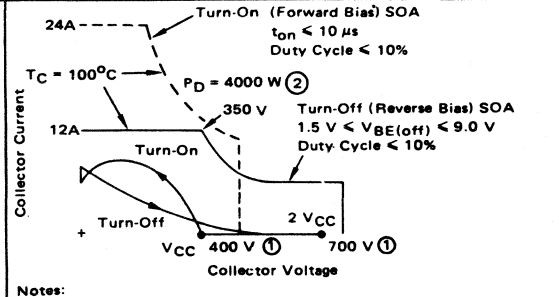
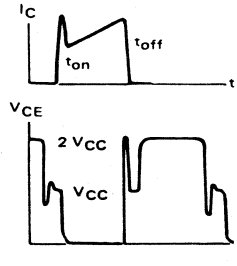
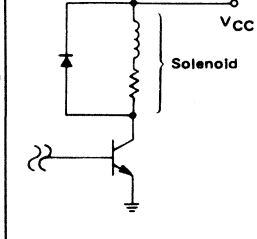
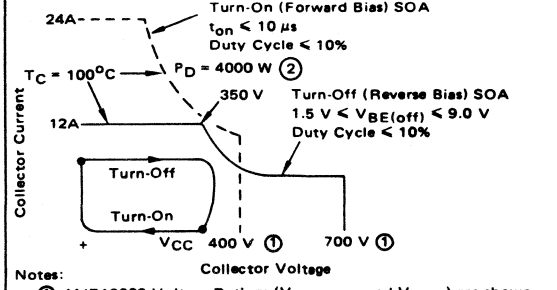
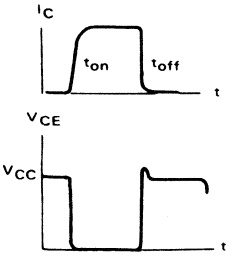
	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 	 Notes: ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
B	**RINGING CHOKE INVERTER** 	 Notes: ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 For Pulse Power Derating Procedure	
C	**PUSH-PULL INVERTER/CONVERTER** 	 Notes: ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	
D	**SOLENOID DRIVER** 	 Notes: ① MJE13009 Voltage Ratings ($V_{CEO(sus)}$ and V_{CEV}) are shown, MJE13008 Ratings are 100 V Lower. ② See AN-569 for Pulse Power Derating Procedure.	

TABLE 3 – TYPICAL INDUCTIVE SWITCHING PERFORMANCE

I_C AMP	T_C °C	t_{sv} ns	t_{rv} ns	t_{fi} ns	t_{ti} ns	t_c ns
3	25	770	100	150	200	240
	100	1000	230	160	200	320
5	25	630	72	26	10	100
	100	820	100	55	30	180
8	25	720	55	27	2	77
	100	920	70	50	8	120
12	25	640	20	17	2	41
	100	800	32	24	4	54

NOTE: All Data recorded in the Inductive Switching Circuit in Table 1.

SWITCHING TIME NOTES

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 13 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 14. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

MOTOROLA

SEMICONDUCTORS

Designers▲ Data Sheet

2N6542
2N6543

5 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
100 WATTS

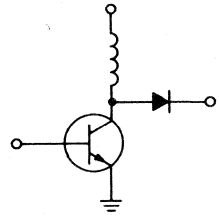
SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The 2N6542 and 2N6543 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

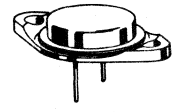
Specification Features –

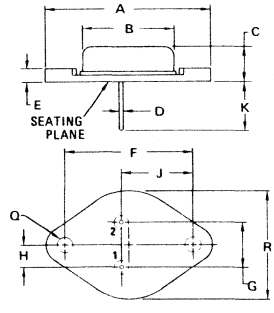
High Temperature Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents



Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03

***MAXIMUM RATINGS**

Rating	Symbol	2N6542	2N6543	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	9.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	5.0 10		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	5.0 10		Adc
Emitter Current – Continuous – Peak (1)	I_E I_{EM}	10 20		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	100 57.2 0.57		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.75	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

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C

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted:)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mA, I_B = 0)	2N6542		300	–	
	2N6543		400	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 13)		$V_{CEX(sus)}$			Vdc
(I_C = 2.6 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	2N6542		350	–	
	2N6543		450	–	
(I_C = 5.0 Adc, V_{clamp} = Rated V_{CEO} -100 V,	2N6542		200	–	
T_C = 100°C)	2N6543		300	–	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C			–	3.0	
Collector Cutoff Current		I_{CER}	–	3.0	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)					
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	0.2	–	Adc
t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 1.5 Adc, V_{CE} = 2.0 Vdc)			12	60	
(I_C = 3.0 Adc, V_{CE} = 2.0 Vdc)			7.0	35	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc)			–	1.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	5.0	
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C)			–	2.0	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 3.0 Adc, I_B = 0.6 Adc)			–	1.4	
(I_C = 3.0 Adc, I_B = 0.6 Adc, T_C = 100°C			–	1.4	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	6.0	28	MHz
(I_C = 200 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance		C_{ob}	50	200	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)					
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 250 Vdc, I_C = 3.0 A, I_{B1} = I_{B2} = 0.6 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05	μs
Rise Time		t_r	–	0.7	μs
Storage Time		t_s	–	4.0	μs
Fall Time		t_f	–	0.8	μs
Inductive Load, Clamped (Table 1)					
Storage Time	(I_C = 3.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 0.6 A, $V_{BE(off)}$ = 5.0 Vdc , T_C = 100°C)	t_s	–	4.0	μs
Fall Time		t_f	–	0.8	μs
			Typical		
Storage Time	(I_C = 3.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 0.6 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_s	1.1		μs
Fall Time		t_f	0.12		μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

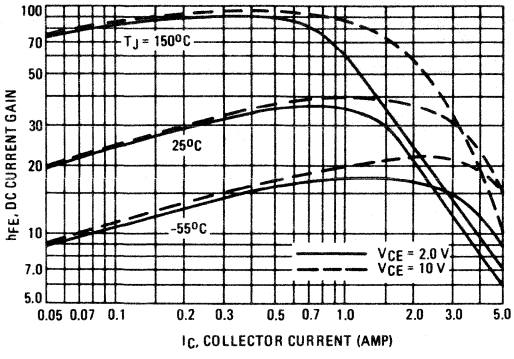


FIGURE 2 – COLLECTOR SATURATION REGION

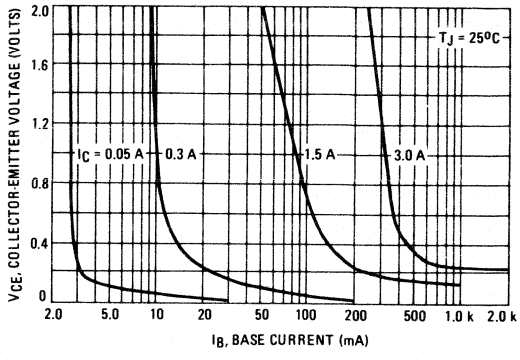


FIGURE 3 – "ON" VOLTAGE

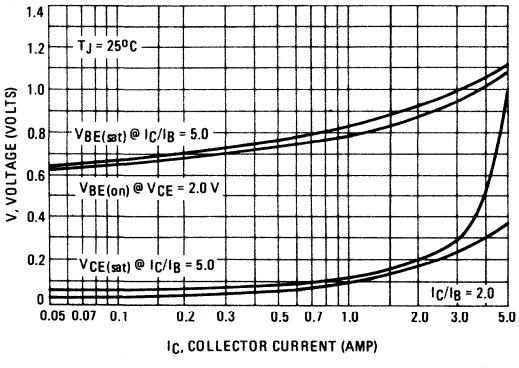


FIGURE 4 – TEMPERATURE COEFFICIENTS

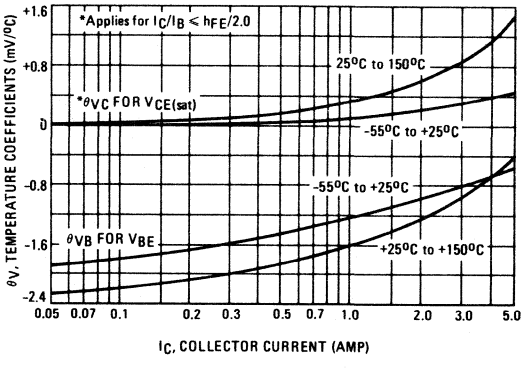


FIGURE 5 – COLLECTOR CUTOFF REGION

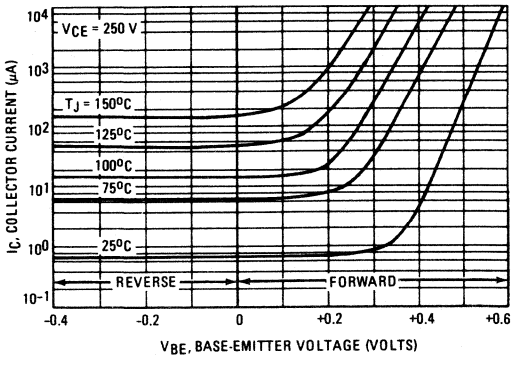


FIGURE 6 – CAPACITANCE

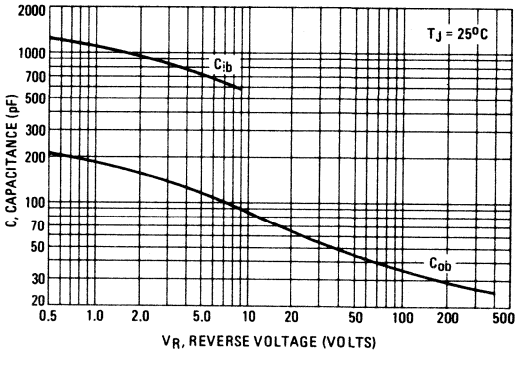
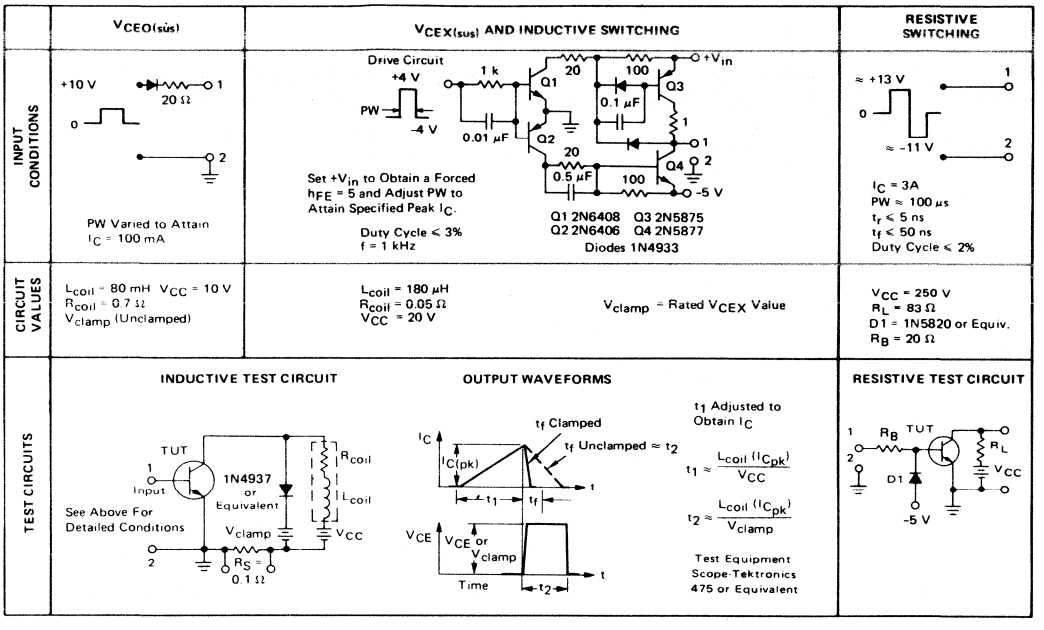


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE



DESIGNERS INFORMATION FOR APPLICATIONS AND SWITCHMODE▲ SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for switch-mode applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in switch-mode applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

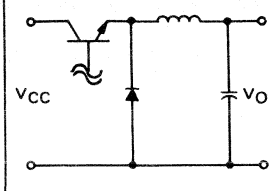
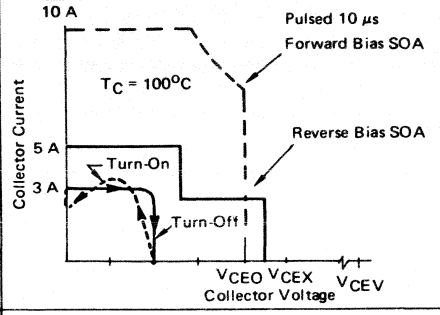
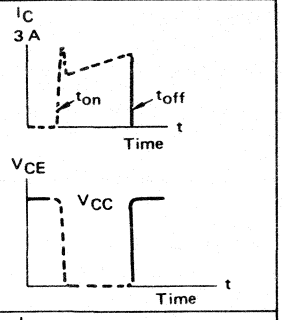
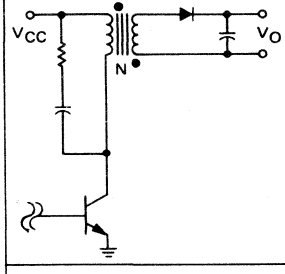
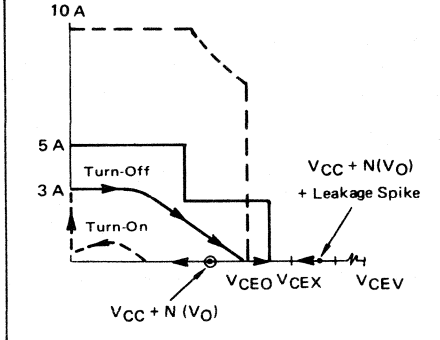
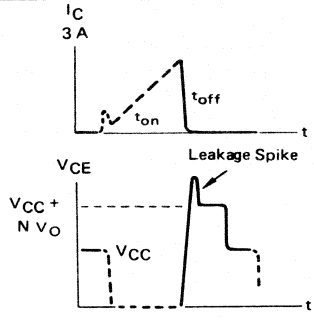
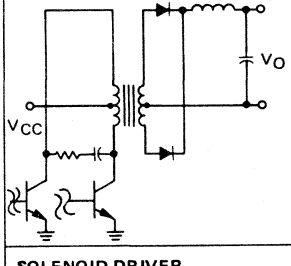
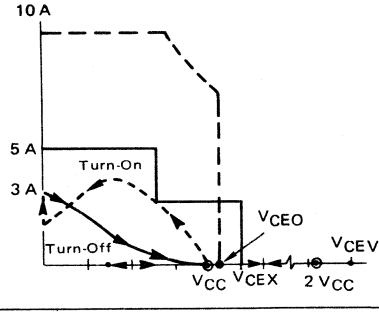
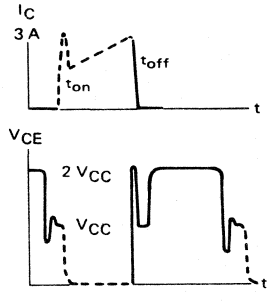
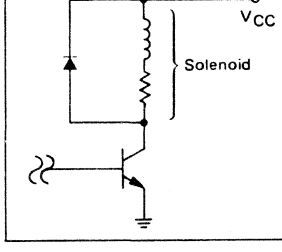
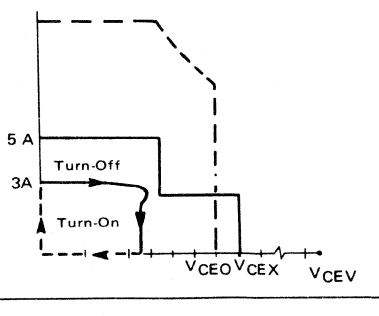
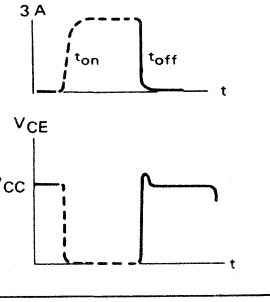
The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 12) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given high collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

As shown on the reverse bias SOA curve in Figure 13, two voltage levels are specified, one at the maximum continuous current level and one near the recommended operating level so that both normal and fault/transient

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-588, AN-719, AN-737, AN-752, AN-767 and Engineering Bulletins EB-39, EB-65.

TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	SERIES SWITCHING REGULATOR 		
B	RINGING CHOKE INVERTER 		
C	PUSH-PULL INVERTER/CONVERTER 		
D	SOLENOID DRIVER 		

conditions can be taken into consideration. In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves. Note that the boundary along the $I_C = 0$ axis extends to V_{CEV}.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output reactifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to limit the leakage spike to $< V_{CEX(sus)}$ during turn-off and $< V_{CEV}$ after turn-off (i.e. @ $I_C \leqslant I_{CEV}$).

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time or pulse width does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 12).

(3) The base drive conditions are similar to those specified on the data sheet (See Table 1), i.e., $V_{BE(off)} \leqslant 5$ V.

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 3 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_f). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 8 and Table 3 and resistive loads in Figures 9 and 10. Usually the inductive load component will be the dominant factor in switch-mode applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

SECONDARY BREAKDOWN REQUIRMENTS

Secondary breakdown capability is important in switching applications because of the turn-on and turn-off conditions that can exist during the switching cycle. Typically, forward biased secondary breakdown ($I_{S/b}$) is not a problem in switching applications because of the relatively higher current capability in the forward biased mode. The forward biased SOA curves provide adequate information for these conditions.

Reverse biased secondary breakdown ($E_{S/b}$) is quite different and a more complex situation from both design and specification standpoint. The $E_{S/b}$ rating is intended to define the amount of energy that the device can absorb while it is in a reverse biased avalanche mode (unclamped). The major problems in specifying $E_{S/b}$ are:

(1) Individual device capability can vary by more than an order of magnitude within the same production lot.

(2) Energy handling capability is not constant within the same device family when the test conditions are changed.

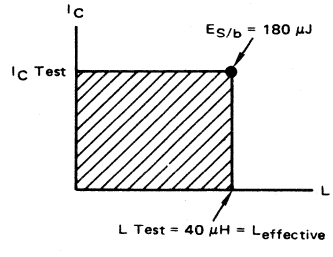
(3) $E_{S/b}$ testing is often destructive when a device actually goes into secondary breakdown.

(4) Some device families exhibit very limited capability in the avalanche condition.

(5) Depending on the device and test conditions, some devices may not reach the avalanche condition during the test.

For these reasons, the most reliable design approach is to avoid this mode of operation by clamping or snubbing the main inductive load component and minimizing leakage inductance whenever possible. The $E_{S/b}$ specification does provide a boundary condition represented in Figure 7.

FIGURE 7 – COLLECTOR CURRENT versus UNCLAMPED LOAD INDUCTANCE



Operation with an unclamped inductance is safe within the shaded area provided the base drive conditions are similar to or less severe than the specified conditions shown in Table 1, i.e., $V_{BE(off)} \leqslant 4$ V, $R_{BE} \geqslant 50\,\Omega$ and

$$L_{effective} = \frac{L_L(V_{CEX})}{V_{CEX}\text{-}V_{CC}}$$

where L_L = Circuit Leakage Reactance

TEMPERATURE REQUIREMENTS

The important parameters on this data sheet have been specified at a case temperature of 100°C to represent a recommended worst case design condition.

FIGURE 8 – TURN-OFF WAVEFORM

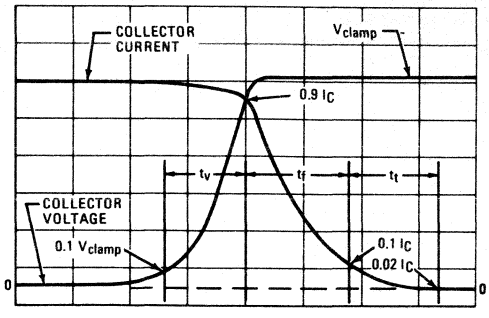


TABLE 3 – INDUCTIVE SWITCHING PERFORMANCE

I_C (A)	T_C °C	t_s µs	t_v µs	t_f µs	t_t µs	$t_v+t_f+t_t$ µs
1.0	25	0.70	0.22	0.21	0.23	0.66
	100	1.20	0.37	0.19	0.39	0.95
3.0	25	1.10	0.09	0.12	0.08	0.29
	100	1.60	0.42	0.19	0.40	1.01
5.0	25	1.10	0.16	0.19	0.11	0.46
	100	1.70	0.45	0.37	0.26	1.08

Note: All Data Recorded in the Inductive Switching Circuit Shown in Table 1.

To facilitate volume production testing, maximum inductive switching limits for these transistors are specified using conventional measurement techniques, e.g. t_s(max) is measured from the point where I_{B1} has decreased 10% to the point where I_C has decreased 10%, and t_f(max) is measured between the 90% and 10% points on the I_C waveform. In most applications, a large percentage of the total device power dissipation occurs during the fall time and t_f is normally used as a figure of merit when choosing a device for a switch-mode application. However, there are two portions of the turn-off waveform that can add losses and in some cases these losses can become a significant portion of the total device dissipation.

Figure 8 shows an enlarged portion of the inductive switching waveform during turn-off. The interval labeled t_v is part of the storage time interval (t_s) and is defined as voltage switching time. During this interval the transistor collector to emitter voltage changes from a saturation level to a level equal to or approaching the clamp voltage while the collector current has only changed by 10%. Typical values for this time interval at various current levels are shown in Table 3 at 25°C and 100°C case temperature.

The time interval labeled t_t occurs after the fall time and appears as a "tail" on the trailing edge of the collector current waveform. It is measured, for this discussion, from the 10% point to the 2% point; and during this interval the collector to emitter voltage is equal to the clamp voltage. Typical values for these time intervals are also shown in Table 3.

Since power dissipation occurs during the total time period $t_v + t_f + t_t$ and each interval can be affected by external conditions, some applications may require a specific analysis in order to accurately predict total device dissipation.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON TIME

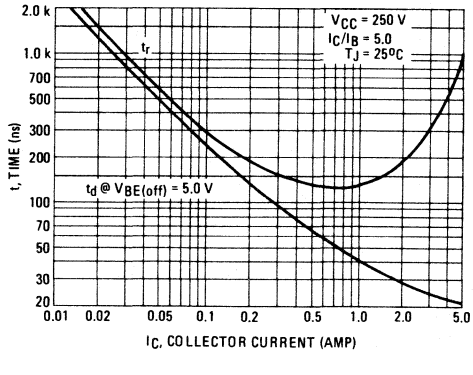


FIGURE 10 – TURN-OFF TIME

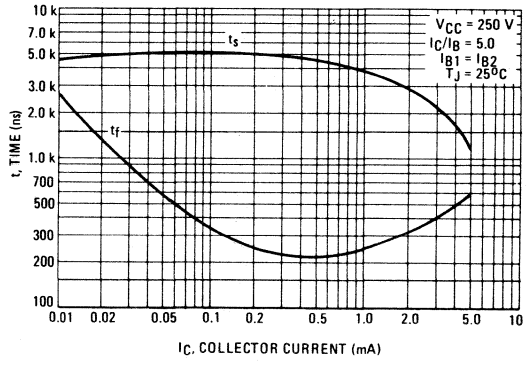


FIGURE 11 – THERMAL RESPONSE

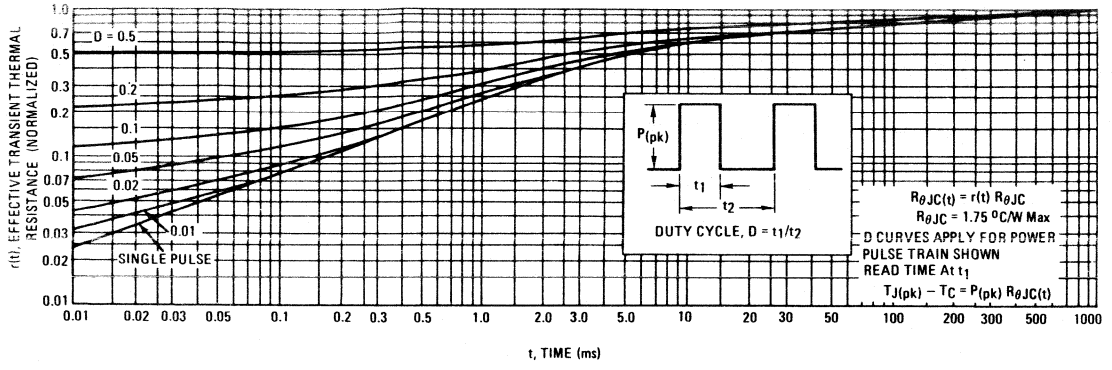


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

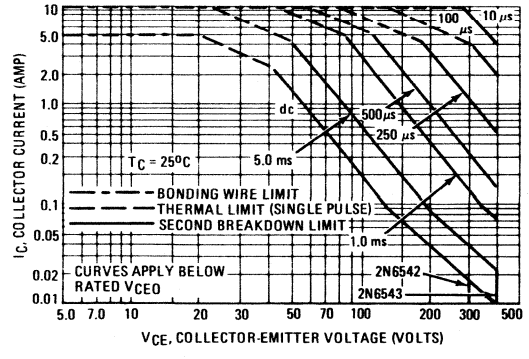


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

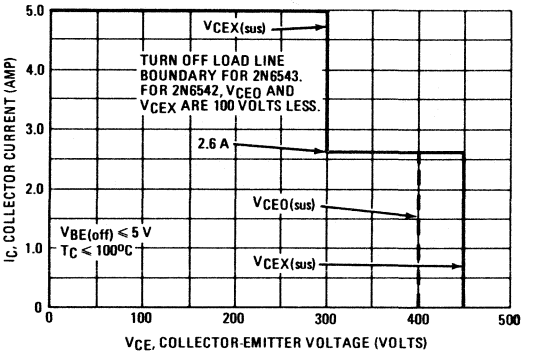
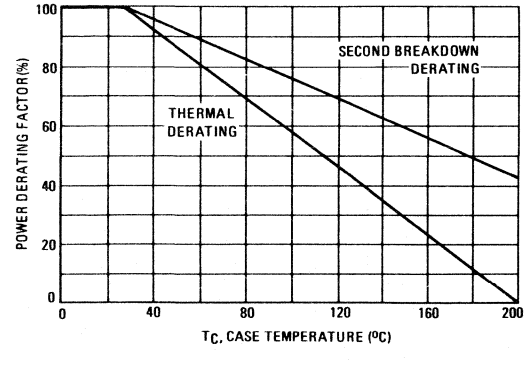


FIGURE 14 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 13) is discussed in the designer's application section.

MOTOROLA

SEMICONDUCTORS

Designers▲ Data Sheet

2N6544
2N6545

8 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
125 WATTS

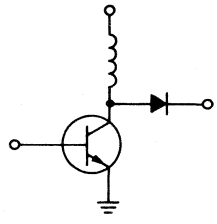
SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The 2N6544 and 2N6545 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

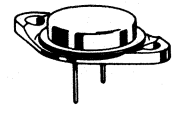
Specification Features –

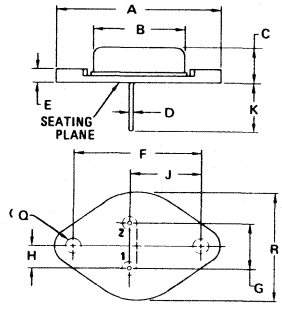
High Temperature Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03

***MAXIMUM RATINGS**

Rating	Symbol	2N6544	2N6545	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	9.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	8.0 16		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	8.0 16		Adc
Emitter Current – Continuous – Peak (1)	I_E I_{EM}	16 32		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	125 71.5 0.714		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

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***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mA, I_B = 0)	2N6544		300	–	
	2N6545		400	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 13)		$V_{CEX(sus)}$			Vdc
(I_C = 4.5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	2N6544		350	–	
	2N6545		450	–	
(I_C = 8.0 A, V_{clamp} = Rated V_{CEO} -100 V,	2N6544		200	–	
T_C = 100°C)	2N6545		300	–	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	0.5	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C			–	2.5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	3.0	mAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)		$I_{S/b}$	0.2	–	Adc
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 2.5 Adc, V_{CE} = 3.0 Vdc)			12	60	
(I_C = 5.0 Adc, V_{CE} = 3.0 Vdc)			7.0	35	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	1.5	
(I_C = 8.0 Adc, I_B = 2.0 Adc)			–	5.0	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C)			–	2.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 5.0 Adc, I_B = 1.0 Adc)			–	1.6	
(I_C = 5.0 Adc, I_B = 1.0 Adc, T_C = 100°C			–	1.6	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 300 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	6.0	28	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)		C_{ob}	75	300	pF
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = I_{B2} = 1.0 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05	μs
Rise Time		t_r	–	1.0	μs
Storage Time		t_s	–	4.0	μs
Fall Time		t_f	–	1.0	μs
Inductive Load, Clamped (Table 1)					
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_s	–	4.0	μs
Fall Time		t_f	–	0.9	μs
			Typical		
Storage Time	(I_C = 5.0 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_s	1.2		μs
Fall Time		t_f	0.18		μs

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

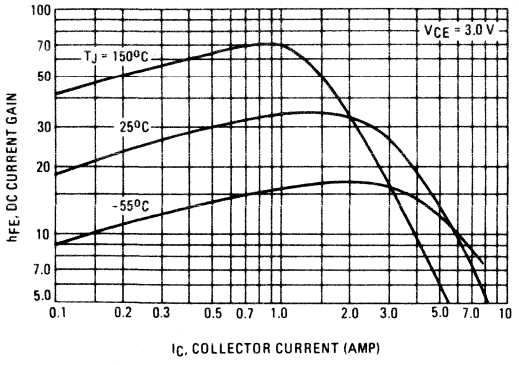


FIGURE 2 – COLLECTOR SATURATION REGION

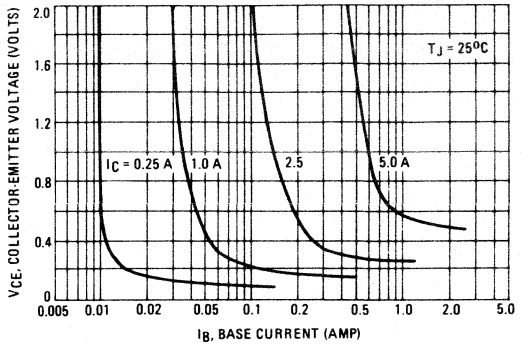


FIGURE 3 – "ON" VOLTAGE

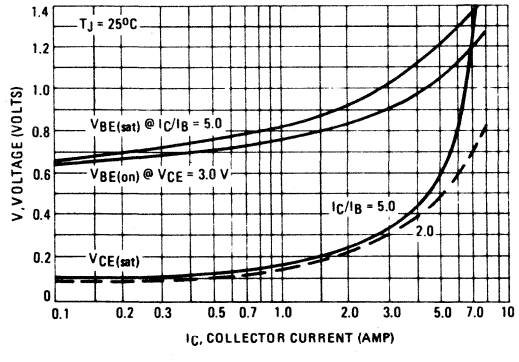


FIGURE 4 – TEMPERATURE COEFFICIENTS

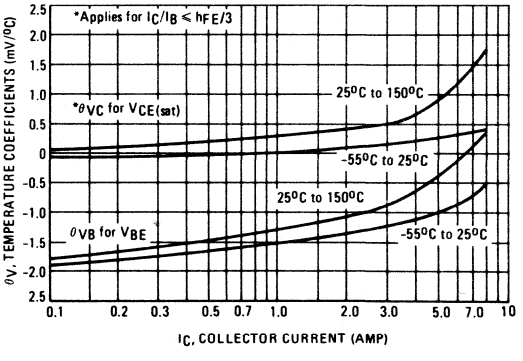


FIGURE 5 – COLLECTOR CUTOFF REGION

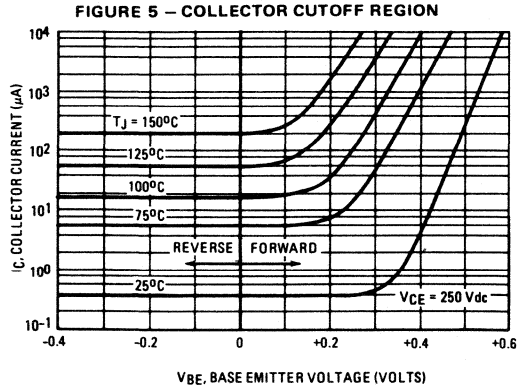


FIGURE 6 – CAPACITANCE

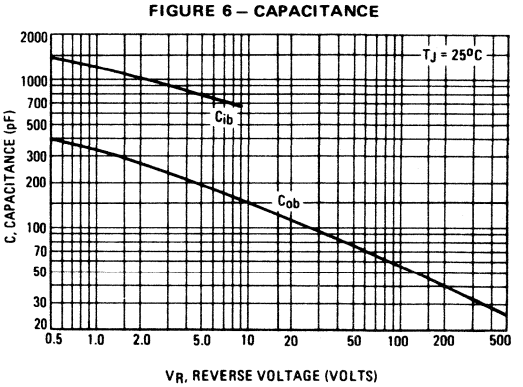


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20 Ω, 0, 1, 2 PW Varied to Attain I_C = 100 mA	Drive Circuit: +4 V, PW, -4 V, 1 k, 0.01 μF, 20, 100, +V_{in}, Q1, Q2, Q3, Q4, 0.1 μF, 0.5 μF, -5 V Set +V_{in} to Obtain a Forced h_{FE} = 5 and Adjust PW to Attain Specified Peak I_C. Duty Cycle ≤ 3% f = 1 kHz Q1 2N6408 Q3 2N5875 Q2 2N6406 Q4 2N5877 Diodes 1N4933	≈ +13 V, 0, ≈ -11 V, 1, 2 I_C = 5 A PW ≈ 100 μs t_r ≤ 5 ns t_f ≤ 50 ns Duty Cycle ≤ 2%
CIRCUIT VALUES	L_{coil} = 80 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} (Unclamped)	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω D1 = 1N5820 or Equiv. R_B = 12 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1, Input, 2, 1N4937 or Equivalent, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, R_S = 0.1 Ω, See Above For Detailed Conditions OUTPUT WAVEFORMS: t_f Clamped, t_f Unclamped ≈ t_2, I_C, $I_{C(pk)}$, t_1, t_f, V_{CE}, V_{clamp}, Time, t_2, t t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT: 1, 2, R_B, TUT, R_L, V_{CC}, D1, -5 V

DESIGNERS INFORMATION FOR APPLICATIONS AND SWITCHMODE▲ SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for switch-mode applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in switch-mode applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

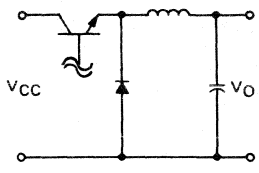
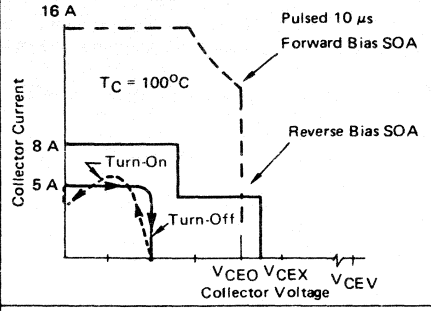
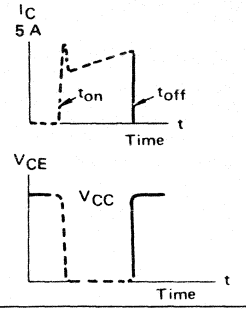
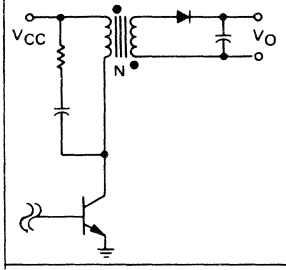
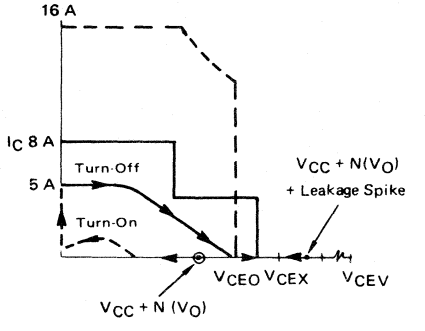
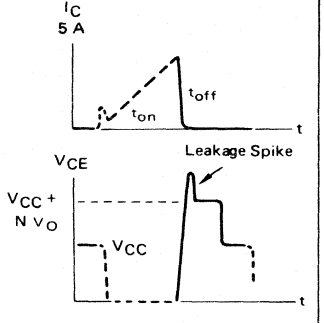
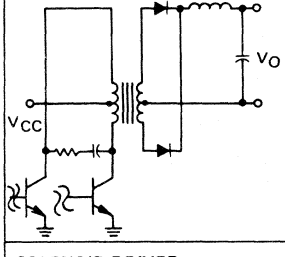
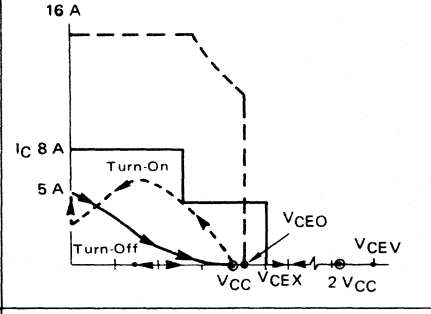
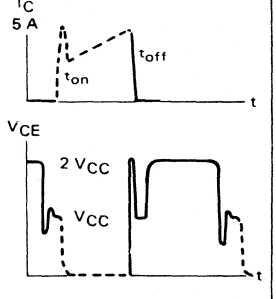
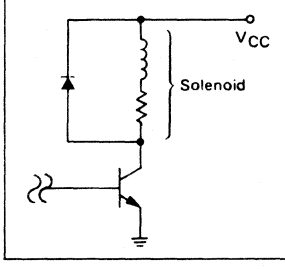
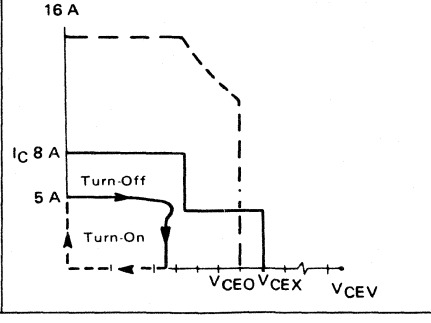
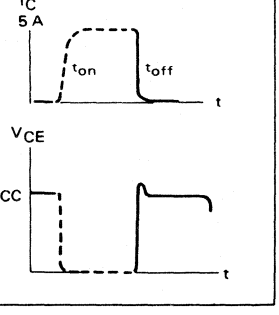
The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 12) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given high collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

As shown on the reverse bias SOA curve in Figure 13, two voltage levels are specified, one at the maximum continuous current level and one near the recommended operating level so that both normal and fault/transient

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-588, AN-719, AN-737, AN-752, AN-767 and Engineering Bulletins EB-39, EB-65.

TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 		
B	**RINGING CHOKE INVERTER** 		
C	**PUSH-PULL INVERTER/CONVERTER** 		
D	**SOLENOID DRIVER** 		

conditions can be taken into consideration. In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves. Note that the boundary along the $I_C = 0$ axis extends to V_{CEV}.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output reactifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to limit the leakage spike to $< V_{CEX(sus)}$ during turn-off and $< V_{CEV}$ after turn-off (i.e. @ $I_C \leq I_{CEV}$).

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time or pulse width does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 12).

(3) The base drive conditions are similar to those specified on the data sheet (See Table 1), i.e., $V_{BE(off)} \leq 5$ V.

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at **5** amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_f). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 8 and Table 3 and resistive loads in Figures 9 and 10. Usually the inductive load component will be the dominant factor in switch-mode applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

SECONDARY BREAKDOWN REQUIRMENTS

Secondary breakdown capability is important in switching applications because of the turn-on and turn-off conditions that can exist during the switching cycle. Typically, forward biased secondary breakdown ($I_{S/b}$) is not a problem in switching applications because of the relatively higher current capability in the forward biased mode. The forward biased SOA curves provide adequate information for these conditions.

Reverse biased secondary breakdown ($E_{S/b}$) is quite different and a more complex situation from both design and specification standpoint. The $E_{S/b}$ rating is intended to define the amount of energy that the device can absorb while it is in a reverse biased avalanche mode (unclamped). The major problems in specifying $E_{S/b}$ are:

(1) Individual device capability can vary by more than an order of magnitude within the same production lot.

(2) Energy handling capability is not constant within the same device family when the test conditions are changed.

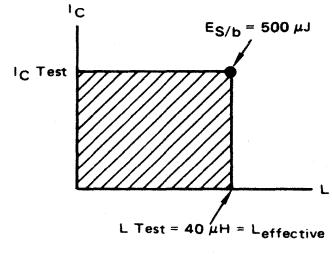
(3) $E_{S/b}$ testing is often destructive when a device actually goes into secondary breakdown.

(4) Some device families exhibit very limited capability in the avalanche condition.

(5) Depending on the device and test conditions, some devices may not reach the avalanche condition during the test.

For these reasons, the most reliable design approach is to avoid this mode of operation by clamping or snubbing the main inductive load component and minimizing leakage inductance whenever possible. The $E_{S/b}$ specification does provide a boundary condition represented in Figure 7.

FIGURE 7 – COLLECTOR CURRENT versus UNCLAMPED LOAD INDUCTANCE



Operation with an unclamped inductance is safe within the shaded area provided the base drive conditions are similar to or less severe than the specified conditions shown in Table 1, i.e., $V_{BE(off)} \leq 4$ V, $R_{BE} \geq 50\ \Omega$ and

$$L_{effective} = \frac{L_L(V_{CEX})}{V_{CEX}-V_{CC}}$$

where L_L = Circuit Leakage Reactance

TEMPERATURE REQUIREMENTS

The important parameters on this data sheet have been specified at a case temperature of 100°C to represent a recommended worst case design condition.

FIGURE 8 – TURN-OFF WAVEFORM

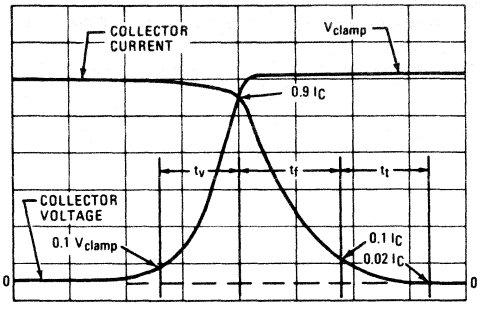


TABLE 3—INDUCTIVE SWITCHING PERFORMANCE

I_C Amps	T_C °C	t_s μs	t_v μs	t_f μs	t_t μs	$t_v+t_f+t_t$ μs
3.0	25	0.94	0.09	0.14	0.10	0.33
	100	1.40	0.30	0.44	0.06	0.80
5.0	25	1.20	0.17	0.18	0.10	0.45
	100	1.90	0.50	0.45	0.05	1.00
8.0	25	1.60	0.27	0.12	0.09	0.48
	100	1.80	0.57	0.17	0.30	1.04

Note: All Data Recorded in the Inductive Switching Circuit Shown in Table 1.

To facilitate volume production testing, maximum inductive switching limits for these transistors are specified using conventional measurement techniques, e.g. t_s(max) is measured from the point where I_{B1} has decreased 10% to the point where I_C has decreased 10%, and t_f(max) is measured between the 90% and 10% points on the I_C waveform. In most applications, a large percentage of the total device power dissipation occurs during the fall time and t_f is normally used as a figure of merit when choosing a device for a switch-mode application. However, there are two portions of the turn-off waveform that can add losses and in some cases these losses can become a significant portion of the total device dissipation.

Figure 8 shows an enlarged portion of the inductive switching waveform during turn-off. The interval labeled t_v is part of the storage time interval (t_s) and is defined as voltage switching time. During this interval the transistor collector to emitter voltage changes from a saturation level to a level equal to or approaching the clamp voltage while the collector current has only changed by 10%. Typical values for this time interval at various current levels are shown in Table 3 at 25°C and 100°C case temperature.

The time interval labeled t_t occurs after the fall time and appears as a "tail" on the trailing edge of the collector current waveform. It is measured, for this discussion, from the 10% point to the 2% point; and during this interval the collector to emitter voltage is equal to the clamp voltage. Typical values for these time intervals are also shown in Table 3.

Since power dissipation occurs during the total time period $t_v + t_f + t_t$ and each interval can be affected by external conditions, some applications may require a specific analysis in order to accurately predict total device dissipation.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON TIME

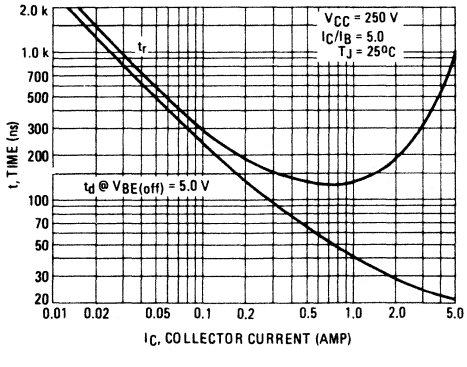


FIGURE 10 – TURN-OFF TIME

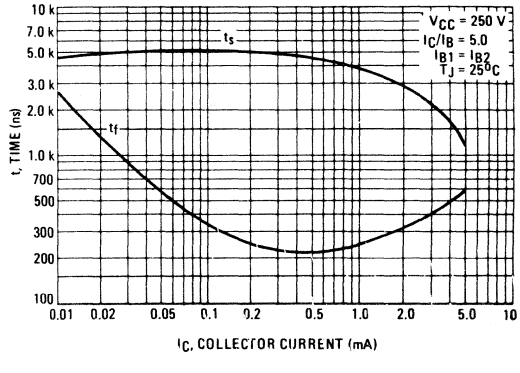


FIGURE 11 – THERMAL RESPONSE

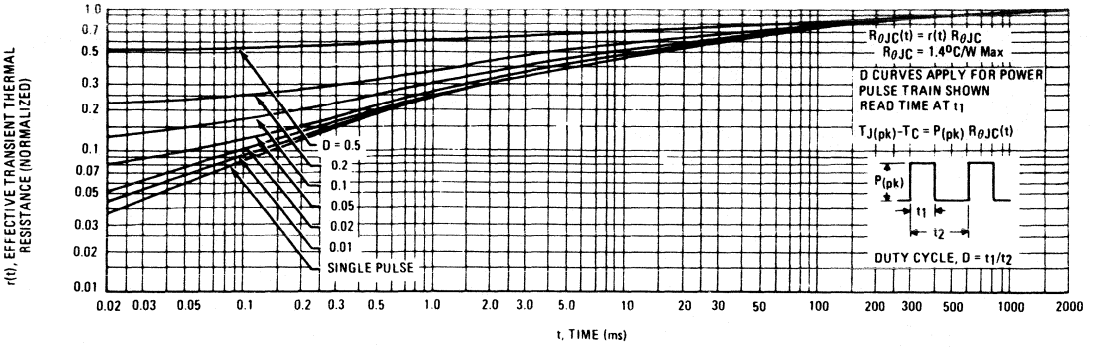


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

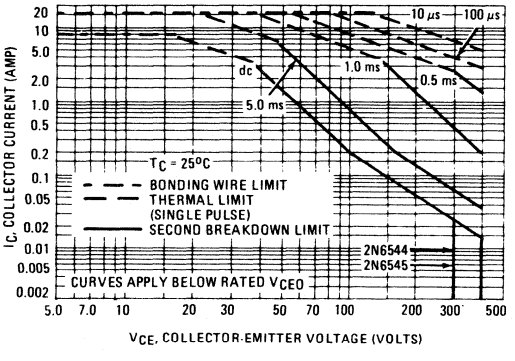


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

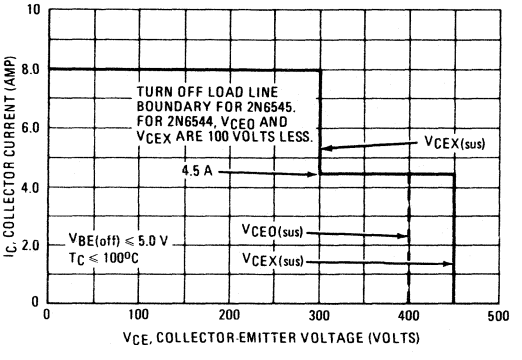
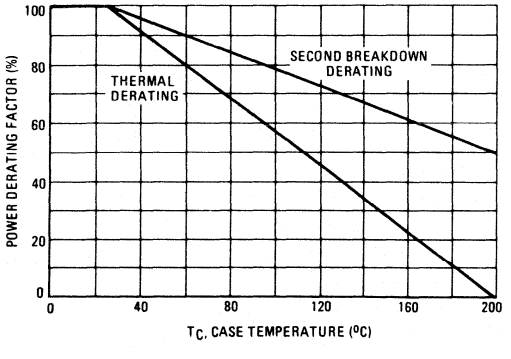


FIGURE 14 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^{\circ}C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^{\circ}C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 13) is discussed in the designer's application section.

MOTOROLA

SEMICONDUCTORS

Designers▲ Data Sheet

2N6546
2N6547

15 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
175 WATTS

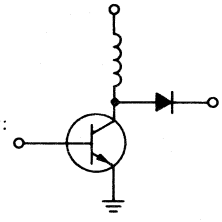
SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The 2N6546 and 2N6547 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

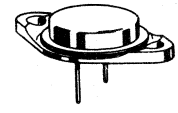
Specification Features –

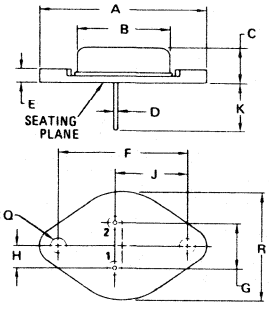
High Temperature Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents



Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03

***MAXIMUM RATINGS**

Rating	Symbol	2N6546	2N6547	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	9.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	15 30		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	10 20		Adc
Emitter Current – Continuous – Peak (1)	I_E I_{EM}	25 50		Adc
Total Power Dissipation @ $T_C = 25^oC$ @ $T_C = 100^oC$ Derate above 25^oC	P_D	175 100 1.0		Watts $W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		^oC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	$^oC/W$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	^oC

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

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***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$			Vdc
(I_C = 100 mA, I_B = 0)	2N6546		300	–	
	2N6547		400	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 13)		$V_{CEX(sus)}$			Vdc
(I_C = 8.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	2N6546		350	–	
	2N6547		450	–	
(I_C = 15 A, V_{clamp} = Rated V_{CEO} – 100 V,	2N6546		200	–	
T_C = 100°C)	2N6547		300	–	
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	1.0	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	4.0	
Collector Cutoff Current		I_{CER}	–	5.0	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)					
Emitter Cutoff Current		I_{EBO}	–	1.0	mAdc
(V_{EB} = 9.0 Vdc, I_C = 0)					
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	0.2	–	Adc
t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)					
ON CHARACTERISTICS (1)					
DC Current Gain		h_{FE}			–
(I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)			12	60	
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			6.0	30	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 2.0 Adc)			–	1.5	
(I_C = 15 Adc, I_B = 3.0 Adc)			–	5.0	
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)			–	2.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 Adc, I_B = 2.0 Adc)			–	1.6	
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C			–	1.6	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product		f_T	6.0	28	MHz
(I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)					
Output Capacitance		C_{ob}	125	500	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)					
SWITCHING CHARACTERISTICS					
Resistive Load (Table 1)					
Delay Time	(V_{CC} = 250 V, I_C = 10 A,	t_d	–	0.05	μs
Rise Time	I_{B1} = I_{B2} = 2.0 A, t_p = 100 μs,	t_r	–	1.0	μs
Storage Time	Duty Cycle ≤ 2.0%)	t_s	–	4.0	μs
Fall Time		t_f	–	0.7	μs
Inductive Load, Clamped (Table 1)					
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A,	t_s	–	5.0	μs
Fall Time	$V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_f	–	1.5	μs
			Typical		
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A,	t_s	2.0		μs
Fall Time	$V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_f	0.09		μs

*Indicates JEDEC Registered Data.

(1) Puse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

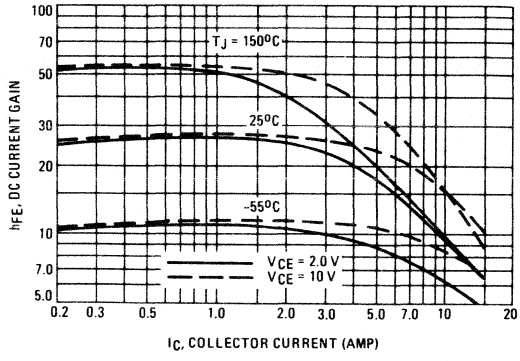


FIGURE 2 – COLLECTOR SATURATION REGION

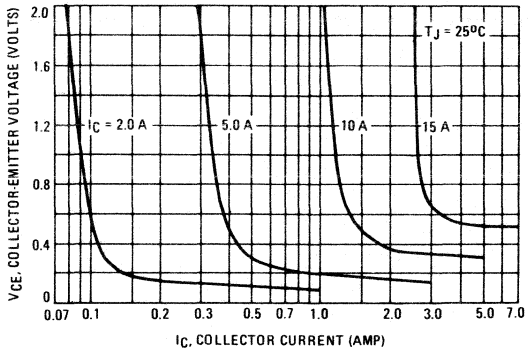


FIGURE 3 – "ON" VOLTAGE

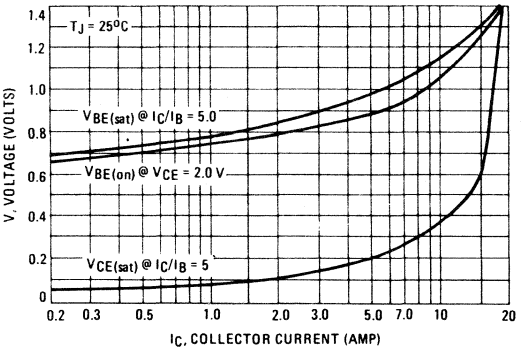


FIGURE 4 – TEMPERATURE COEFFICIENTS

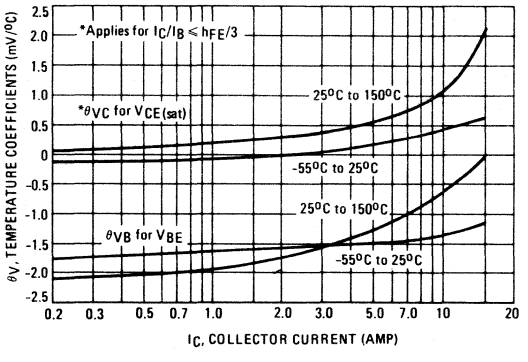


FIGURE 5 – COLLECTOR CUTOFF REGION

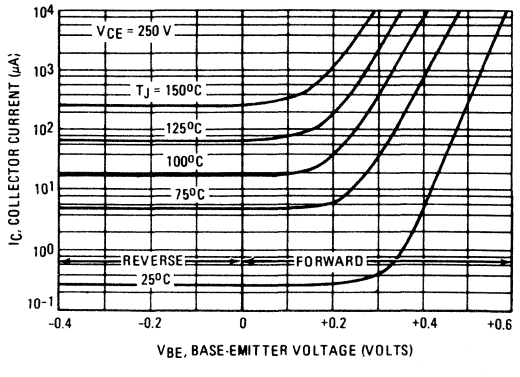


FIGURE 6 – CAPACITANCE

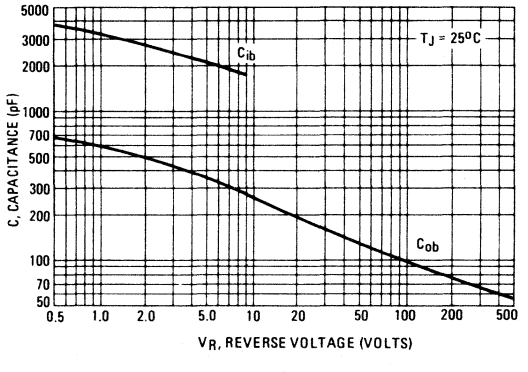


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20 Ω, 0, 1, 2 PW Varied to Attain I_C = 100 mA	Drive Circuit: +4 V, PW, −4 V, 1 k, 0.01 µF, 20, Q1, Q2, 100, Q3, 0.1 µF, 20, Q4, 0.5 µF, 100, $+V_{in}$, −5 V Set $+V_{in}$ to Obtain a Forced h_{FE} = 5 and Adjust PW to Attain Specified Peak I_C Duty Cycle ≤ 3% f = 1 kHz Q1 2N6408 Q3 2N5875 Q2 2N6406 Q4 2N5877 Diodes 1N4933	≈ +13 V, 0, ≈ −11 V, 1, 2 I_C = 10 A PW ≈ 100 µs t_r ≤ 5 ns t_f ≤ 50 ns Duty Cycle ≤ 2%
CIRCUIT VALUES	L_{coil} 80 mH V_{CC} = 10 V R_{coil} 0.7 Ω V_{clamp} (Unclamped)	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω D1 = 1N5820 or Equiv. R_B = 6 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1, Input, 1N4937 or Equivalent, See Above For Detailed Conditions, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, 2, R_S 0.1 Ω OUTPUT WAVEFORMS: I_C, $I_{C(pk)}$, t_f Clamped, t_f Unclamped ≈ t_2, t_1, t_f, t, V_{CE}, V_{CE} or V_{clamp}, Time, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment: Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT: 1, R_B, TUT, R_L, 2, D1, V_{CC}, −5 V

DESIGNERS INFORMATION FOR APPLICATIONS AND SWITCHMODE▲ SPECIFICATIONS

INTRODUCTION

The primary considerations when selecting a power transistor for switch-mode applications are voltage and current ratings, switching speed, and energy handling capability. In this section, these specifications will be discussed and related to the circuit examples illustrated in Table 2.(1)

VOLTAGE REQUIREMENTS

Both blocking voltage and sustaining voltage are important in switch-mode applications.

Circuits B and C in Table 2 illustrate applications that require high blocking voltage capability. In both circuits the switching transistor is subjected to voltages substantially higher than V_{CC} after the device is completely off (see load line diagrams at $I_C = I_{leakage} \approx 0$ in Table 2). The blocking capability at this point depends on the base to emitter conditions and the device junction temperature. Since the highest device capability occurs when the base to emitter junction is reverse biased (V_{CEV}), this is the recommended and specified use condition. Maximum I_{CEV} at rated V_{CEV} is specified at a relatively low reverse bias (1.5 Volts) both at 25°C and 100°C. Increasing the reverse bias will give some improvement in device blocking capability.

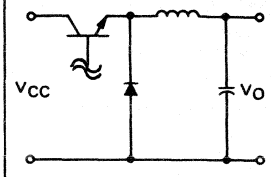
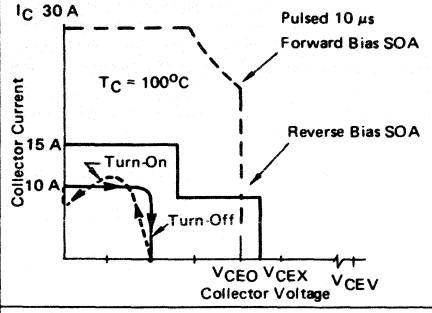
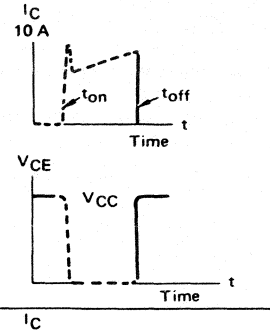
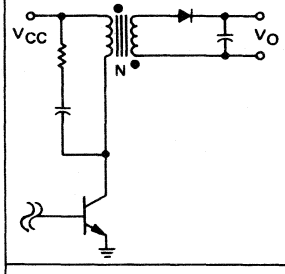
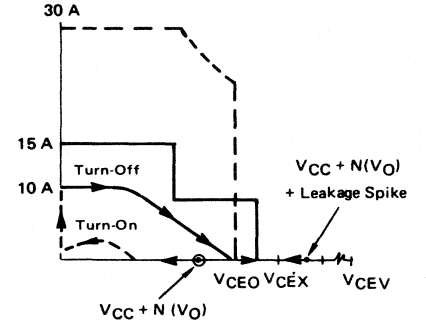
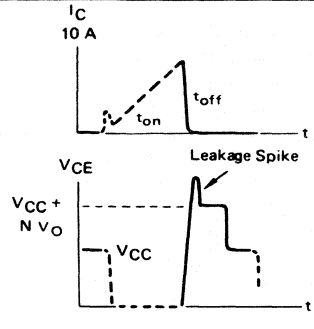
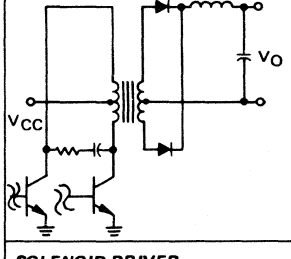
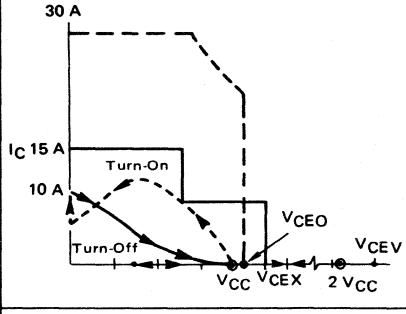
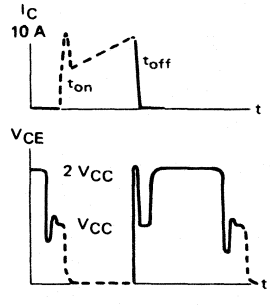
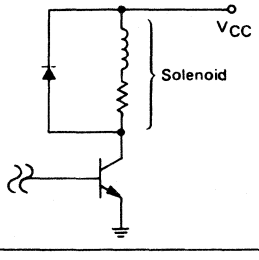
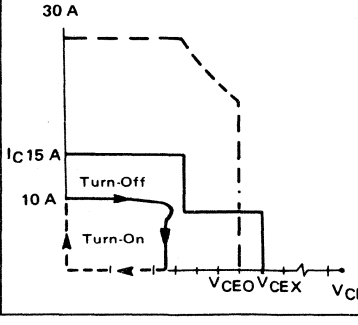
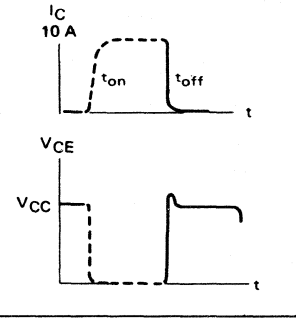
The sustaining or active region voltage requirements in switching applications occur during turn-on and turn-off. If the load contains a significant capacitive component, high current and voltage can exist simultaneously during turn-on and the pulsed forward bias SOA curves (Figure 12) are the proper design limits.

For inductive loads, high voltage and current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given high collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

As shown on the reverse bias SOA curve in Figure 13, two voltage levels are specified, one at the maximum continuous current level and one near the recommended operating level so that both normal and fault/transient

(1) For detailed information on specific switching applications, see Motorola Application Notes AN-588, AN-719, AN-737, AN-752, AN-767 and Engineering Bulletins EB-39, EB-65.

TABLE 2 – APPLICATIONS EXAMPLES OF SWITCHING CIRCUITS

	CIRCUIT	LOAD LINE DIAGRAMS	TIME DIAGRAMS
A	**SERIES SWITCHING REGULATOR** 		
B	**RINGING CHOKE INVERTER** 		
C	**PUSH-PULL INVERTER/CONVERTER** 		
D	**SOLENOID DRIVER** 		

conditions can be taken into consideration. In the four application examples (Table 2) load lines are shown in relation to the pulsed forward and reverse biased SOA curves. Note that the boundary along the $I_C = 0$ axis extends to V_{CEV}.

In circuits A and D, inductive reactance is clamped by the diodes shown. In circuits B and C the voltage is clamped by the output reactifiers, however, the voltage induced in the primary leakage inductance is not clamped by these diodes and could be large enough to destroy the device. A snubber network or an additional clamp may be required to limit the leakage spike to $< V_{CEX(sus)}$ during turn-off and $< V_{CEV}$ after turn-off (i.e. @ $I_C \leqslant I_{CEV}$).

Load lines that fall within the pulsed forward biased SOA curve during turn-on and within the reverse bias SOA curve during turn-off are considered safe, with the following assumptions:

(1) The device thermal limitations are not exceeded.

(2) The turn-on time or pulse width does not exceed 10 μs (see standard pulsed forward SOA curves in Figure 12).

(3) The base drive conditions are similar to those specified on the data sheet (See Table 1), i.e., $V_{BE(off)} \leqslant 5$ V.

CURRENT REQUIREMENTS

An efficient switching transistor must operate at the required current level with good fall time, high energy handling capability and low saturation voltage. On this data sheet, these parameters have been specified at 10 amperes which represents typical design conditions for these devices. The current drive requirements are usually dictated by the $V_{CE(sat)}$ specification because the maximum saturation voltage is specified at a forced gain condition which must be duplicated or exceeded in the application to control the saturation voltage.

SWITCHING REQUIREMENTS

In many switching applications, a major portion of the transistor power dissipation occurs during the fall time (t_f). For this reason considerable effort is usually devoted to reducing the fall time. The recommended way to accomplish this is to reverse bias the base-emitter junction during turn-off. The reverse biased switching characteristics for inductive loads are discussed in Figure 8 and Table 3 and resistive loads in Figures 9 and 10. Usually the inductive load component will be the dominant factor in switch-mode applications and the inductive switching data will more closely represent the device performance in actual application. The inductive switching characteristics are derived from the same circuit used to specify the reverse biased SOA curves, (See Table 1) providing correlation between test procedures and actual use conditions.

SECONDARY BREAKDOWN REQUIRMENTS

Secondary breakdown capability is important in switching applications because of the turn-on and turn-off conditions that can exist during the switching cycle. Typically, forward biased secondary breakdown ($I_{S/b}$) is not a problem in switching applications because of the relatively higher current capability in the forward biased mode. The forward biased SOA curves provide adequate information for these conditions.

Reverse biased secondary breakdown ($E_{S/b}$) is quite different and a more complex situation from both design and specification standpoint. The $E_{S/b}$ rating is intended to define the amount of energy that the device can absorb while it is in a reverse biased avalanche mode (unclamped). The major problems in specifying $E_{S/b}$ are:

(1) Individual device capability can vary by more than an order of magnitude within the same production lot.

(2) Energy handling capability is not constant within the same device family when the test conditions are changed.

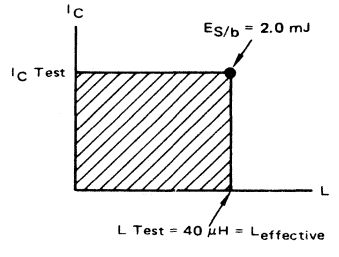
(3) $E_{S/b}$ testing is often destructive when a device actually goes into secondary breakdown.

(4) Some device families exhibit very limited capability in the avalanche condition.

(5) Depending on the device and test conditions, some devices may not reach the avalanche condition during the test.

For these reasons, the most reliable design approach is to avoid this mode of operation by clamping or snubbing the main inductive load component and minimizing leakage inductance whenever possible. The $E_{S/b}$ specification does provide a boundary condition represented in Figure 7.

FIGURE 7 – COLLECTOR CURRENT versus UNCLAMPED LOAD INDUCTANCE



Operation with an unclamped inductance is safe within the shaded area provided the base drive conditions are similar to or less severe than the specified conditions shown in Table 1, i.e., $V_{BE(off)} \leqslant 4$ V, $R_{BE} \geqslant 50\ \Omega$ and

$$L_{effective} = \frac{L_L(V_{CEX})}{V_{CEX}-V_{CC}}$$

where L_L = Circuit Leakage Reactance

TEMPERATURE REQUIREMENTS

The important parameters on this data sheet have been specified at a case temperature of 100°C to represent a recommended worst case design condition.

FIGURE 8 – TURN-OFF WAVEFORM

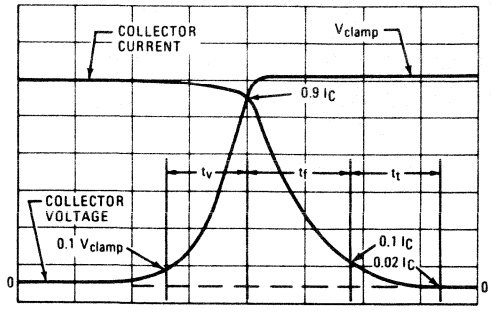


TABLE 3 – INDUCTIVE SWITCHING PERFORMANCE

I_C Amps	T_C °C	t_s μs	t_v μs	t_f μs	t_t μs	$t_v+t_f+t_t$ μs
3.0	25	1.30	0.17	0.05	0.20	0.42
	100	2.10	0.25	0.08	0.25	0.58
5.0	25	1.60	0.08	0.04	0.08	0.20
	100	2.40	0.16	0.08	0.23	0.48
10	25	2.00	0.09	0.09	0.20	0.38
	100	2.50	0.16	0.20	0.13	0.49

Note: All Data Recorded in the Inductive Switching Circuit Shown in Table 1.

To facilitate volume production testing, maximum inductive switching limits for these transistors are specified using conventional measurement techniques, e.g. t_s(max) is measured from the point where I_{B1} has decreased 10% to the point where I_C has decreased 10%, and t_f(max) is measured between the 90% and 10% points on the I_C waveform. In most applications, a large percentage of the total device power dissipation occurs during the fall time and t_f is normally used as a figure of merit when choosing a device for a switch-mode application. However, there are two portions of the turn-off waveform that can add losses and in some cases these losses can become a significant portion of the total device dissipation.

Figure 8 shows an enlarged portion of the inductive switching waveform during turn-off. The interval labeled t_v is part of the storage time interval (t_s) and is defined as voltage switching time. During this interval the transistor collector to emitter voltage changes from a saturation level to a level equal to or approaching the clamp voltage while the collector current has only changed by 10%. Typical values for this time interval at various current levels are shown in Table 3 at 25°C and 100°C case temperature.

The time interval labeled t_t occurs after the fall time and appears as a "tail" on the trailing edge of the collector current waveform. It is measured, for this discussion, from the 10% point to the 2% point; and during this interval the collector to emitter voltage is equal to the clamp voltage. Typical values for these time intervals are also shown in Table 3.

Since power dissipation occurs during the total time period $t_v + t_f + t_t$ and each interval can be affected by external conditions, some applications may require a specific analysis in order to accurately predict total device dissipation.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 9 – TURN-ON TIME

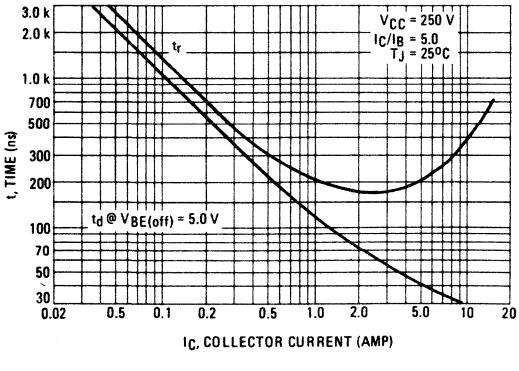


FIGURE 10 – TURN-OFF TIME

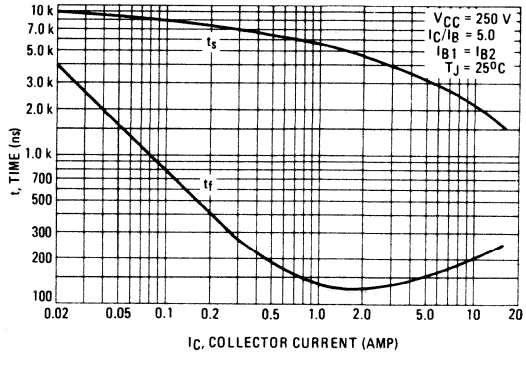


FIGURE 11 – THERMAL RESPONSE

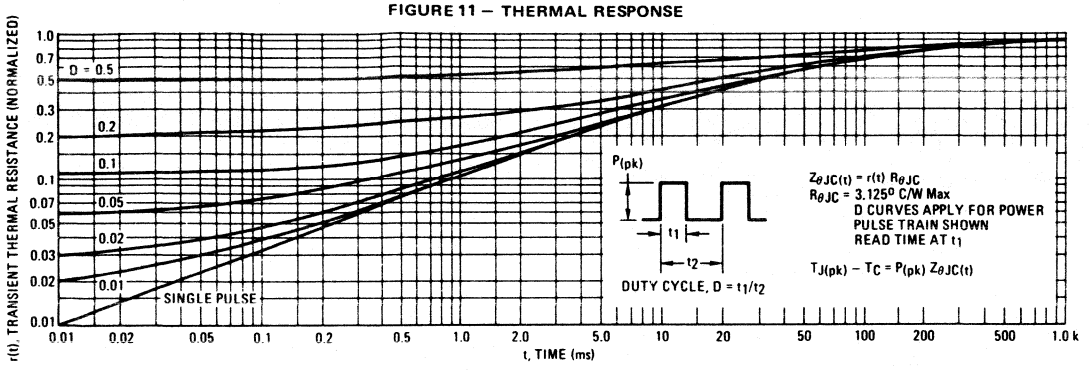


FIGURE 12 – FORWARD BIAS SAFE OPERATING AREA

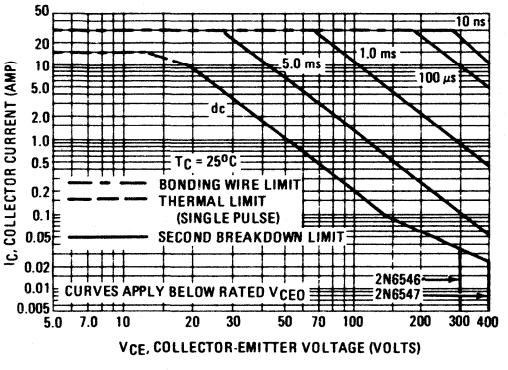


FIGURE 13 – REVERSE BIAS SAFE OPERATING AREA

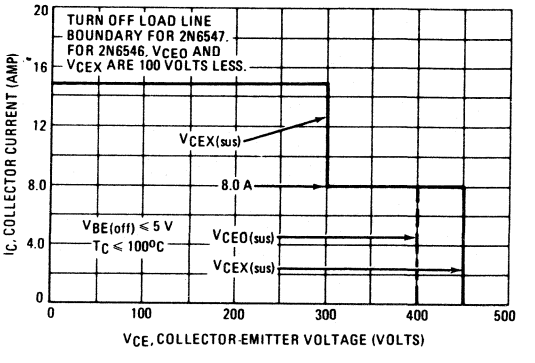
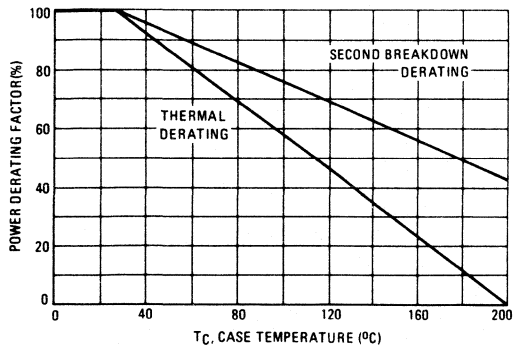


FIGURE 14 – POWER DERATING



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. Use of reverse biased safe operating area data (Figure 13) is discussed in the designer's application section.

MOTOROLA Semiconductors

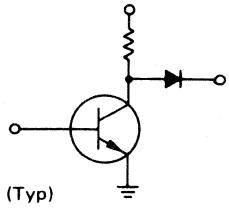
MJ13014
MJ13015

Designers▲ Data Sheet

SWITCHMODE▲ SERIES
NPN SILICON POWER TRANSISTORS

The MJ13014 and MJ13015 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times:
300 ns Inductive Crossover Time @ 25°C (Typ)
1.2 μs Inductive Storage Time @ 25°C (Typ)

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

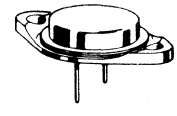
10 AMPERE

NPN SILICON POWER TRANSISTORS

350 AND 400 VOLTS
150 WATTS

Designer's Data for "Worst Case" Conditions

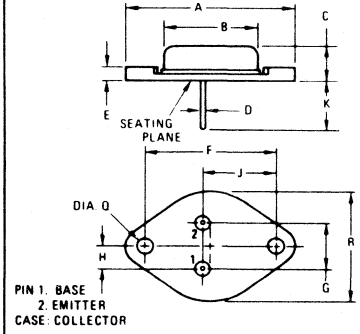
The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



Rating	Symbol	MJ13014	MJ13015	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	500	Vdc
Collector-Emitter Voltage	V_{CEV}	550	600	Vdc
Emitter Base Voltage	V_{EB}	6.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	10 20		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	5.0 10		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 85.5 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	–	39.37	–	1.550
B	–	22.23	–	0.875
C	6.35	11.43	0.250	0.450
D	0.97	1.09	0.038	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

CASE 11-03

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DS 3332

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 100 mA, I_B = 0)	MJ13014		350	–	–	
	MJ13015		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)		$V_{CEX(sus)}$				Vdc
(I_C = 2.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ13014		450	–	–	
	MJ13015		500	–	–	
(I_C = 5.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ13014		325	–	–	
	MJ13015		375	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.5	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	2.5	
Collector Cutoff Current		I_{CER}	–	–	3.0	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)						
Emitter Cutoff Current		I_{EBO}	–	–	1.0	mAdc
(V_{EB} = 6.0 Vdc, I_C = 0)						
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (1)						
DC Current Gain		h_{FE}				–
(I_C = 2.5 Adc, V_{CE} = 5 Vdc)			12	–	40	
(I_C = 5 Adc, V_{CE} = 5 Vdc)			8.0	–	20	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1.0 Adc)			–	–	1.4	
(I_C = 10 Adc, I_B = 2.0 Adc)			–	–	5.0	
(I_C = 5 Adc, I_B = 1.0 Adc, T_C = 100°C)			–	–	2.4	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 1.0 Adc)			–	–	1.5	
(I_C = 5 Adc, I_B = 1.0 Adc, T_C = 100°C)			–	–	1.5	
DYNAMIC CHARACTERISTICS						
Output Capacitance		C_{ob}	50	–	350	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 kHz),						
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 1.0 A,	t_d	–	0.01	0.1	μs
Rise Time	t_p = 25 μs, Duty Cycle ≤ 2%)	t_r	–	0.085	0.5	μs
Storage Time	(V_{CC} = 250 Vdc, I_C = 5.0 A, I_{B1} = 1.0 A,	t_s	–	0.8	2.0	μs
Fall Time	$V_{BE(off)}$ = 5.0 Vdc, t_p = 25 μs, Duty Cycle ≤ 2%)	tf	–	0.095	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 5 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 1 A,	t_{sv}	–	1.8	3.5	μs
Crossover Time	$V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	0.6	1.5	μs
Storage Time	(I_C = 5 A (pk), V_{clamp} = 250 Vdc, I_{B1} = 1 A,	t_{sv}	–	1.2	–	μs
Crossover Time	$V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_c	–	0.3	–	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

FIGURE 1 – DC CURRENT GAIN

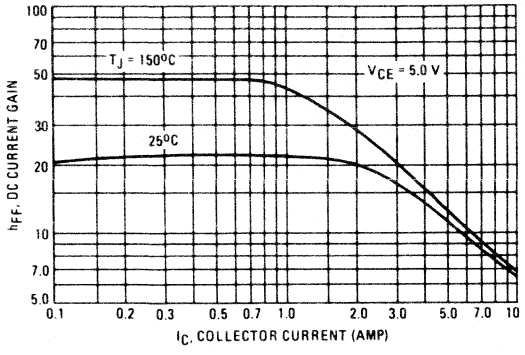


FIGURE 2 – COLLECTOR SATURATION REGION

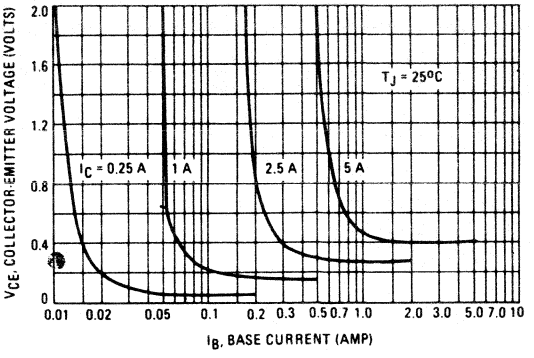


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

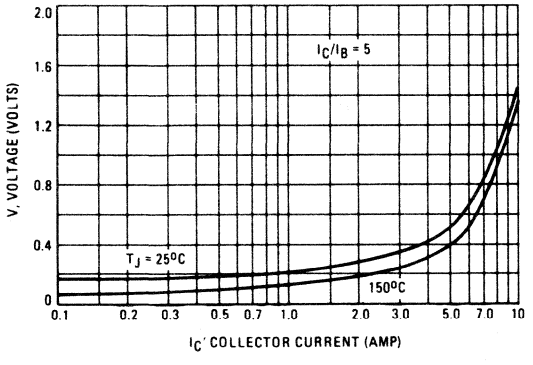


FIGURE 4 – BASE-EMITTER VOLTAGE

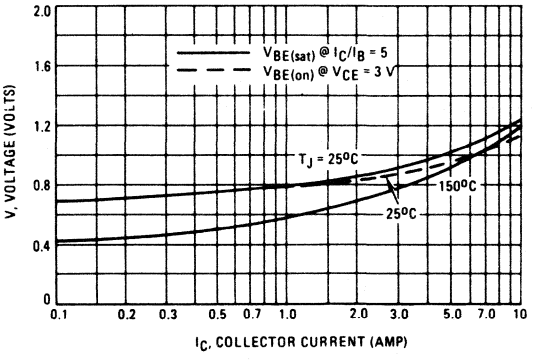


FIGURE 5 – COLLECTOR CUTOFF REGION

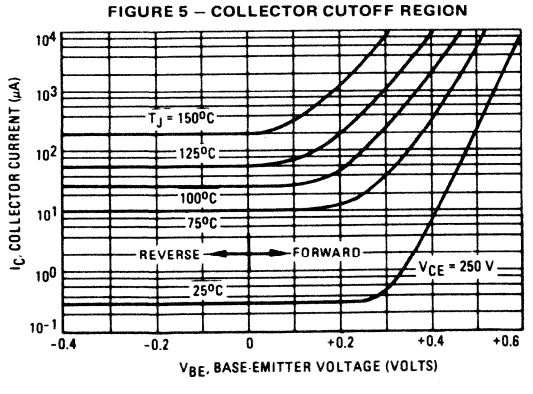


FIGURE 6 – CAPACITANCE

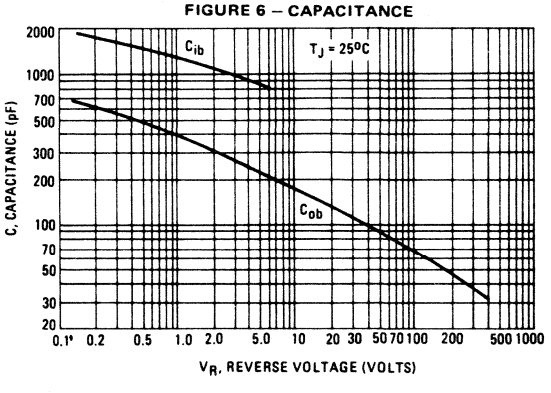
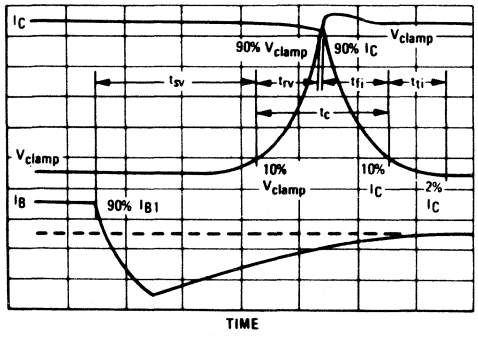


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	PW Varied to Attain I_C = 100 mA	Set $-V_2$ to obtain $V_{BE(off)}$ = 5 V. Set $+V_1$ to obtain a forced H_{FE} = 5 and adjust PW to attain specified peak I_C. Duty Cycle ≤ 2% INDUCTIVE SWITCHING DRIVER Q_1 2N6186 Q_2 2N5346 Diodes 1N4937	TURN-ON TIME I_{B1} adjusted to obtain the forced h_{FE} desired TURN-OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH R_{coil} = 0.7 Ω V_{CC} = 10 V	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 50 Ω
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT See Above For Detailed Conditions OUTPUT WAVEFORMS t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

FIGURE 8 – TURN-ON SWITCHING TIMES

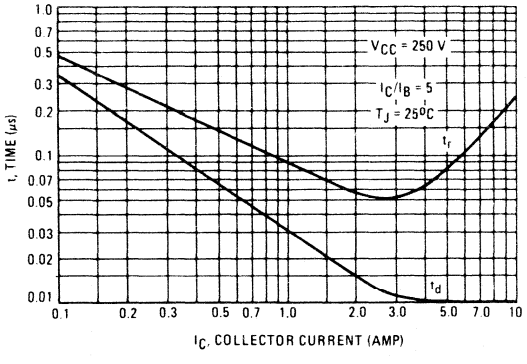


FIGURE 9 – TURN-OFF TIME

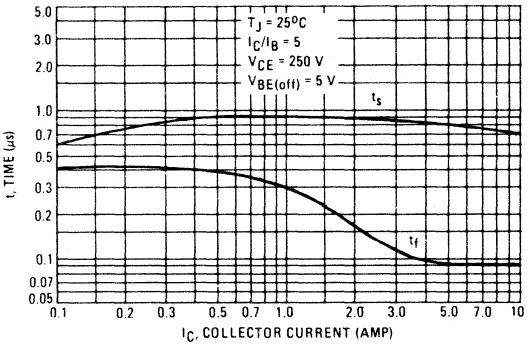
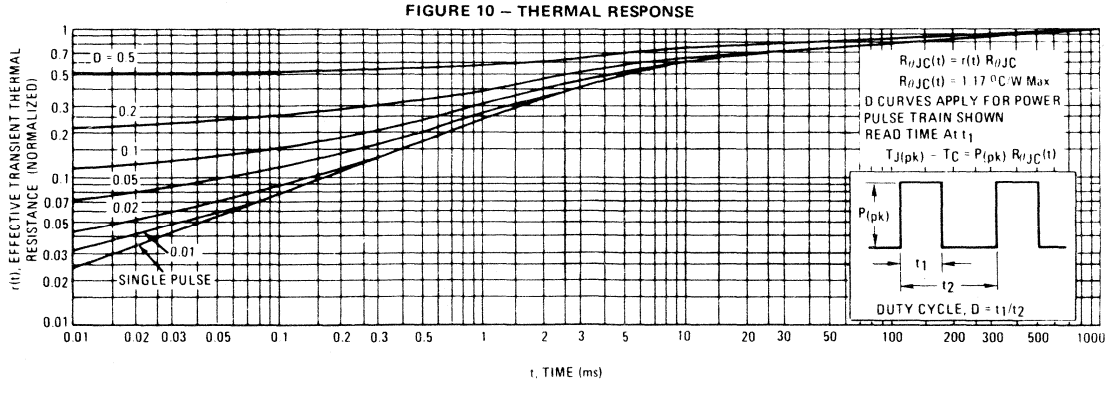


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

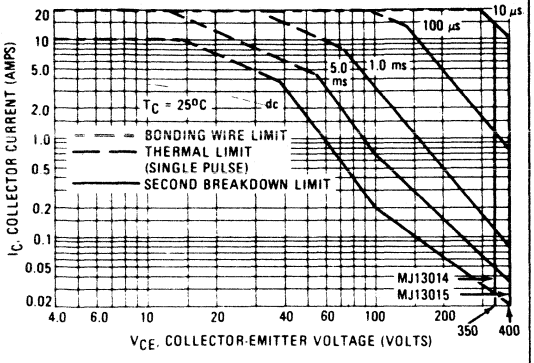
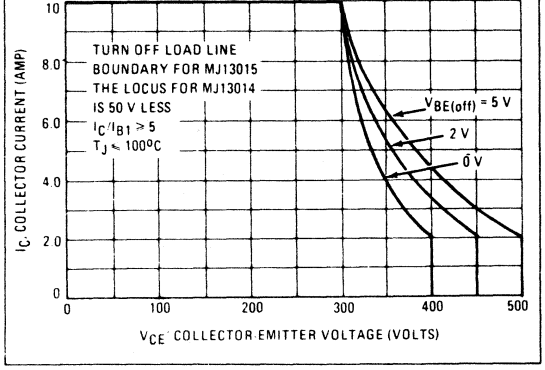


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

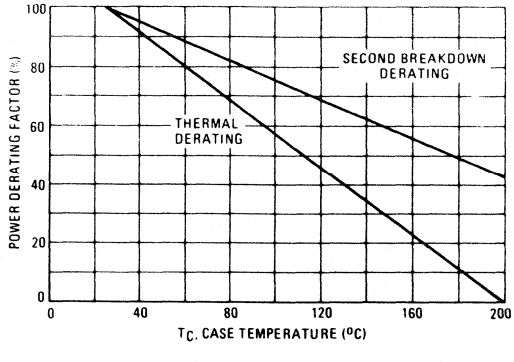
The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



MOTOROLA Semiconductors

MJ10000
MJ10001

Designers▲ Data Sheet

20 AMPERE
NPN SILICON

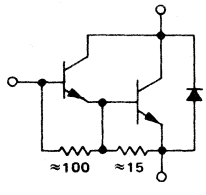
POWER DARLINGTON TRANSISTORS

350 and 400 VOLTS
175 WATTS

SWITCHMODE▲ SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10000 and MJ10001 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times With Inductive Loads — 210 ns Inductive Fall Time (Typ)
- Saturation Voltages
- Leakage Currents

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

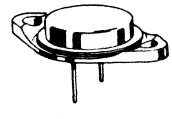
MAXIMUM RATINGS

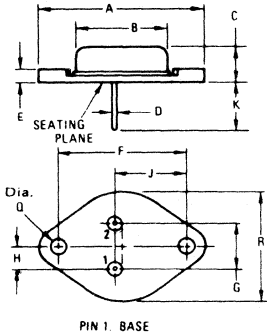
Rating	Symbol	MJ10000	MJ10001	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	20 30		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.





PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO 3

▲ Trademark of Motorola Inc.

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DS 3285 R1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10000		350	–	–	
	MJ10001		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)		$V_{CEX(sus)}$				Vdc
I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C	MJ10000		400	–	–	
	MJ10001		450	–	–	
I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C	MJ10000		275	–	–	
	MJ10001		325	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5	
Collector Cutoff Current		I_{CER}	–	–	5	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)						
Emitter Cutoff Current		I_{EBO}	–	–	150	mAdc
(V_{EB} = 8 Vdc, I_C = 0)						
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			Adc
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				–
(I_C = 5 Adc, V_{CE} = 5 Vdc)			50	–	600	
(I_C = 10 Adc, V_{CE} = 5 Vdc)			40	–	400	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 400 mAdc)			–	–	1.9	
(I_C = 20 Adc, I_B = 1 Adc)			–	–	3	
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)			–	–	2	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 400 mAdc)			–	–	2.5	
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)			–	–	2.5	
Diode Forward Voltage (1)		V_f	–	3	5	Vdc
(I_F = 10 Adc)						
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain		$\lvert h_{fe} \rvert$	10		–	–
(I_C = 10 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)						
Output Capacitance		C_{ob}	100		325	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)						
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A,	t_d	–	0.12	0.2	μs
Rise Time	I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs,	t_r	–	0.20	0.6	μs
Storage Time	Duty Cycle ≤ 2%).	t_s	–	1.5	3.5	μs
Fall Time		t_f	–	1.1	2.4	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA,	t_{sv}	–	3.5	5.5	μs
Crossover Time	$V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_c	–	1.5	3.7	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA,	t_{sv}	–	1.0	–	μs
Crossover Time	$V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_c	–	0.7	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

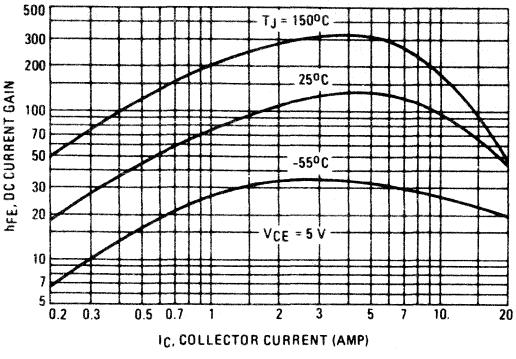


FIGURE 2 – COLLECTOR SATURATION REGION

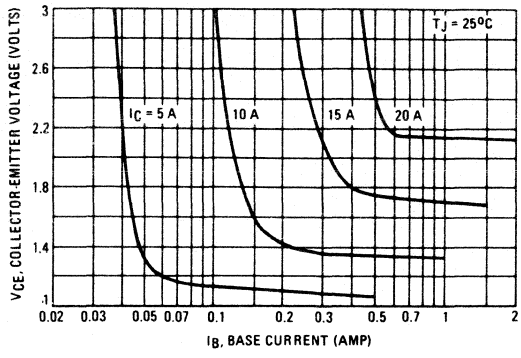


FIGURE 3 – COLLECTOR EMMITTER SATURATION VOLTAGES

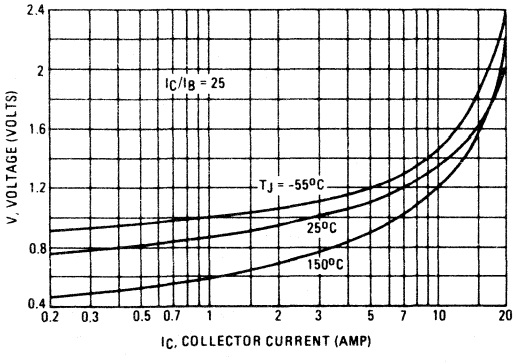


FIGURE 4 – BASE-EMITTER VOLTAGE

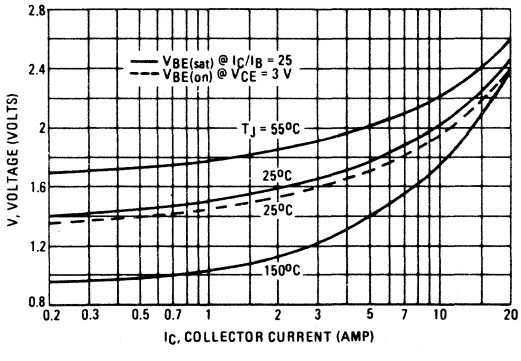


FIGURE 5 – COLLECTOR CUTOFF REGION

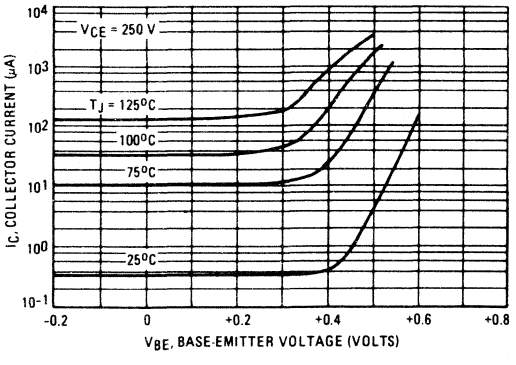


FIGURE 6 – OUTPUT CAPACITANCE

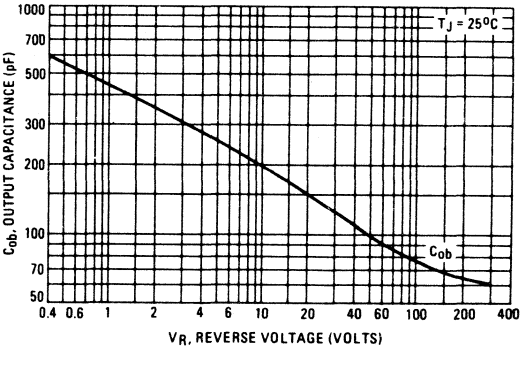
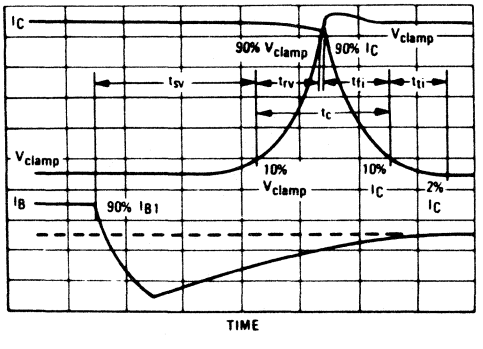


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	PW Varied to Attain I_C = 250 mA	Adjust R1 to obtain a forced h_{FE} = 25; Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs); Duty Cycle < 3%	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT See Above For Detailed Conditions	OUTPUT WAVEFORMS t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

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t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c)\ f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

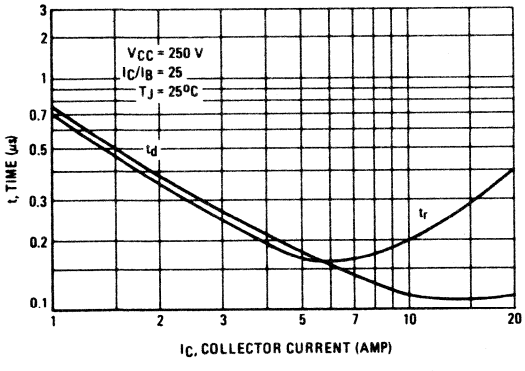


FIGURE 9 – TURN-OFF TIME

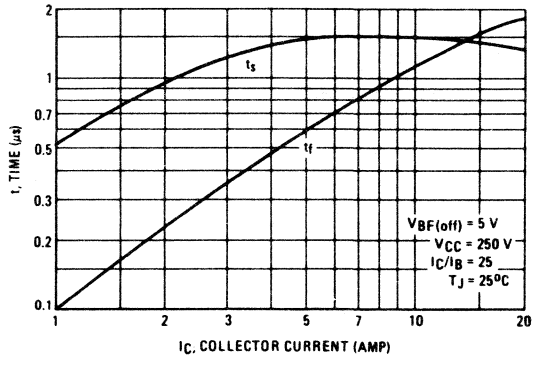
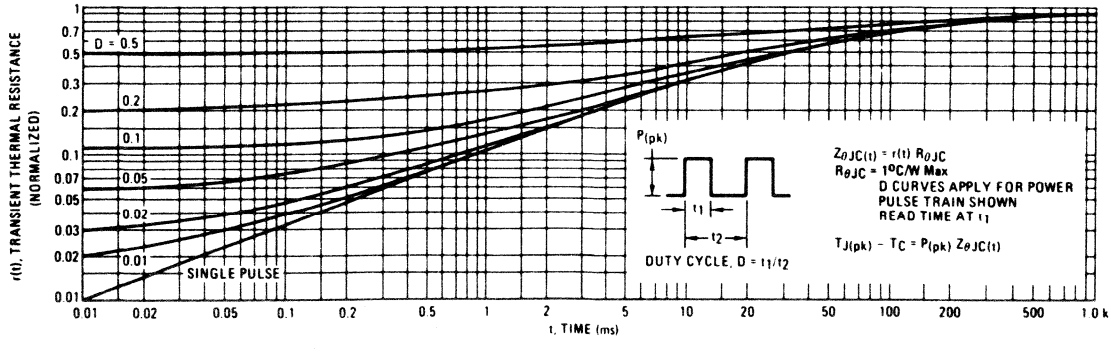


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

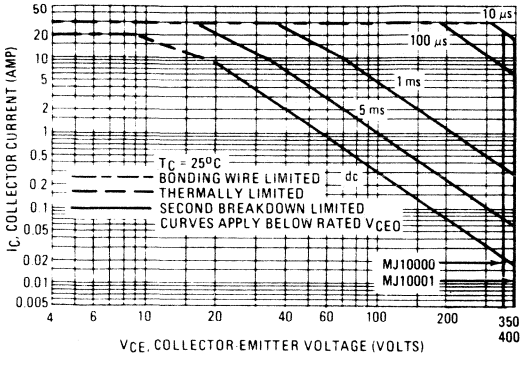
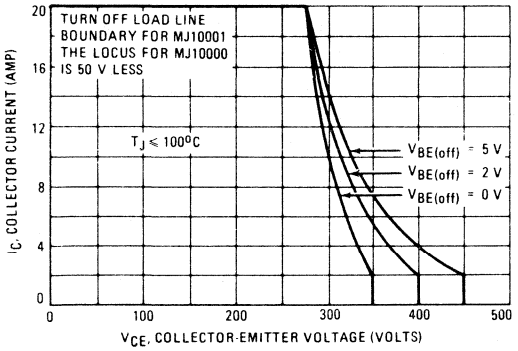


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

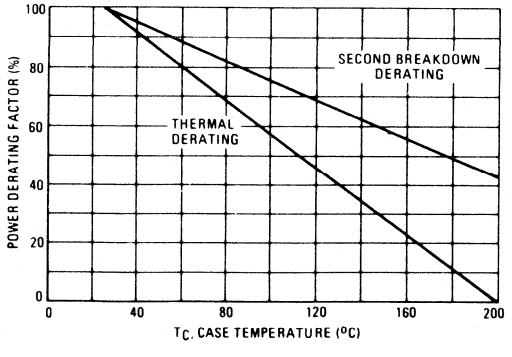
The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



MOTOROLA Semiconductors

MJ10002
MJ10003

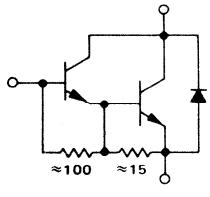
Designers▲ Data Sheet

10 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
350 and 400 VOLTS
150 WATTS

SWITCHMODE▲ SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10002 and MJ10003 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switch-mode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads

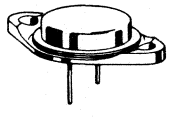
Switching Times with Inductive Loads — 140 ns Inductive Fall Time (Typ)

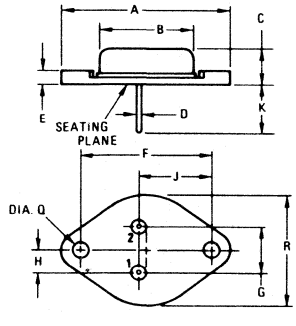
Saturation Voltages

Leakage Currents

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.





PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

MAXIMUM RATINGS

Rating	Symbol	MJ10002	MJ10003	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 20		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	150 100 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted).

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (2)						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10002		350	–	–	
	MJ10003		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)		$V_{CEX(sus)}$				Vdc
(I_C = 1 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10002		400	–	–	
	MJ10003		450	–	–	
(I_C = 5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10002		275	–	–	
	MJ10003		325	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 8 Vdc, I_C = 0)		I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			Adc
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				–
(I_C = 2.5 Adc, V_{CE} = 5 Vdc)			40	–	500	
(I_C = 5 Adc, V_{CE} = 5 Vdc)			30	–	300	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 250 mAdc)			–	–	1.9	
(I_C = 10 Adc, I_B = 1 Adc)			–	–	2.9	
(I_C = 5 Adc, I_B = 250 mAdc, T_C = 100°C)			–	–	2	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 250 mAdc)			–	–	2.5	
(I_C = 5 Adc, I_B = 250 mAdc, T_C = 100°C)			–	–	2.5	
Diode Forward Voltage (1) (I_F = 5.0 Adc)		V_f	–	3	5	Vdc
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		$\lvert h_{fe} \rvert$	10	–	–	–
Output Capacitance (V_{CB} = 50 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	60	–	275	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 5 A, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%).	t_d	–	0.05	0.2	μs
Rise Time		t_r	–	0.25	0.6	μs
Storage Time		t_s	–	1.2	3.0	μs
Fall Time		t_f	–	0.6	1.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 5 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	2.1	5	μs
Crossover Time		t_c	–	1.3	3.3	μs
Storage Time	(I_C = 5 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	0.92	–	μs
Crossover Time		t_c	–	0.5	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

DC CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

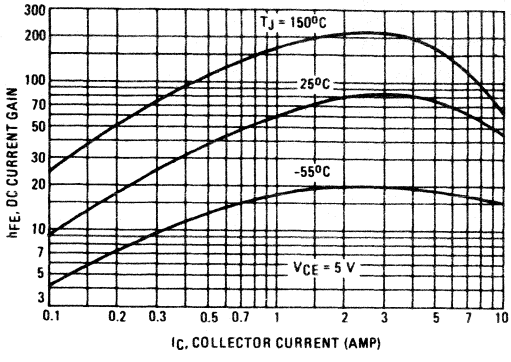


FIGURE 2 – COLLECTOR SATURATION REGION

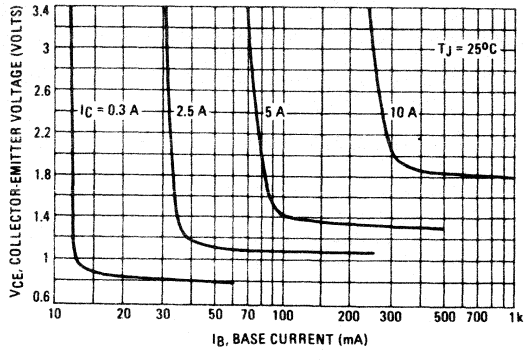


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

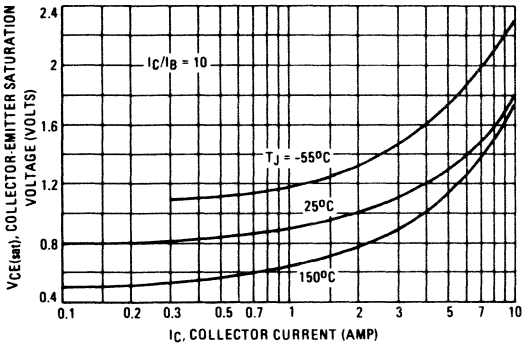


FIGURE 4 – BASE-EMITTER VOLTAGE

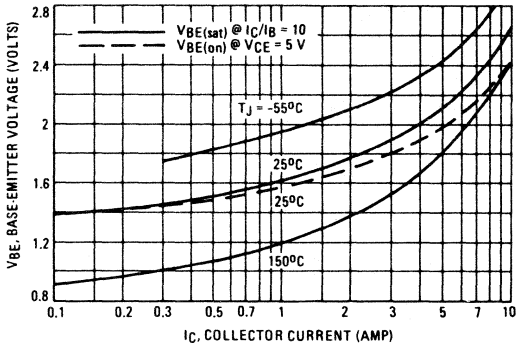


FIGURE 5 – COLLECTOR CUT-OFF REGION

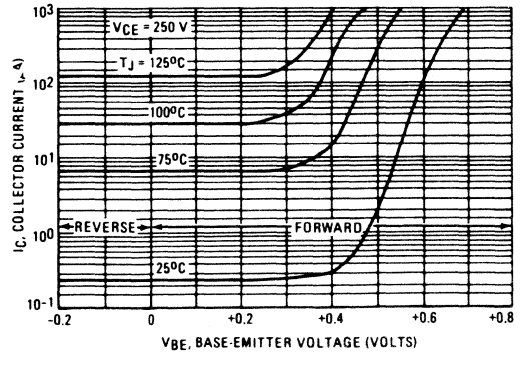


FIGURE 6 – OUTPUT CAPACITANCE

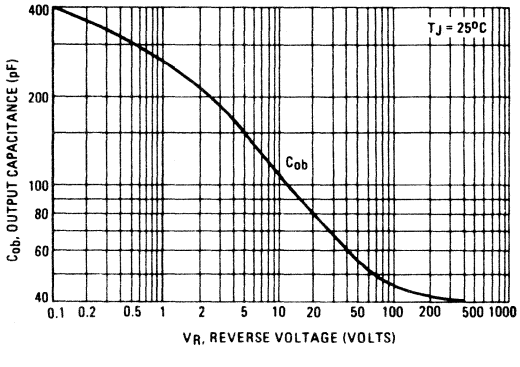


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	PW Varied to Attain I_C = 250 mA	Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs)	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT See Above For Detailed Conditions	OUTPUT WAVEFORMS t_1 Adjusted to Obtain I_C Test Equipment Scope-Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT

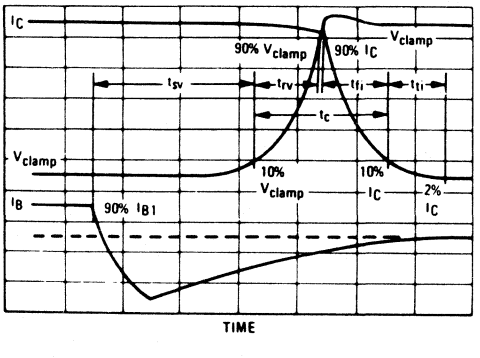


FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

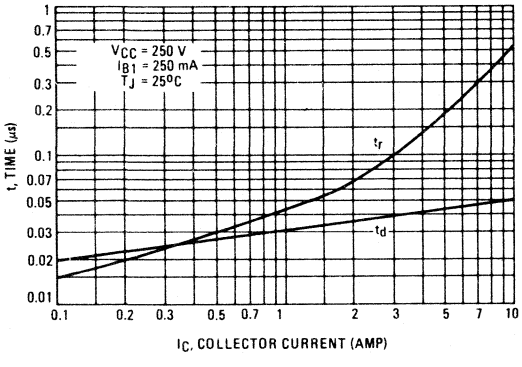


FIGURE 9 – TURN-OFF TIME

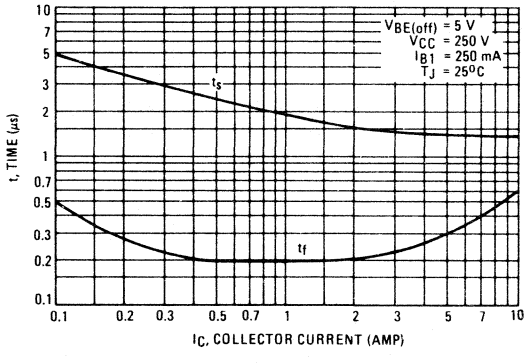
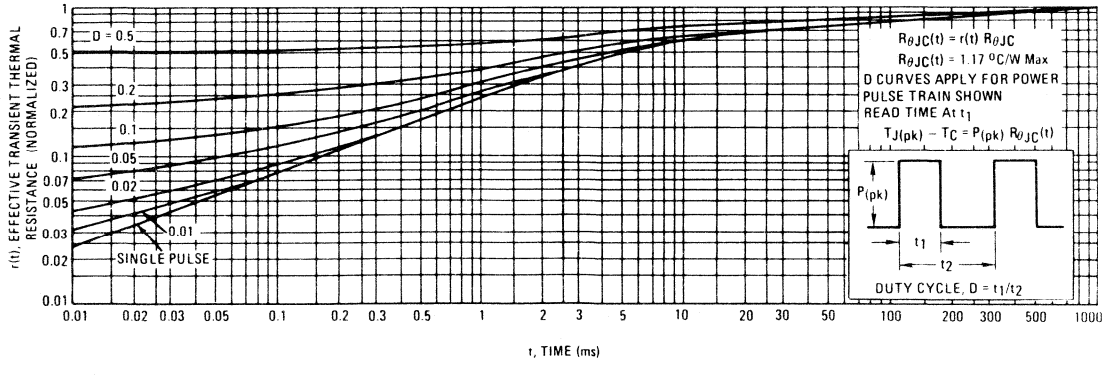


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – ACTIVE-REGION SAFE OPERATING AREA

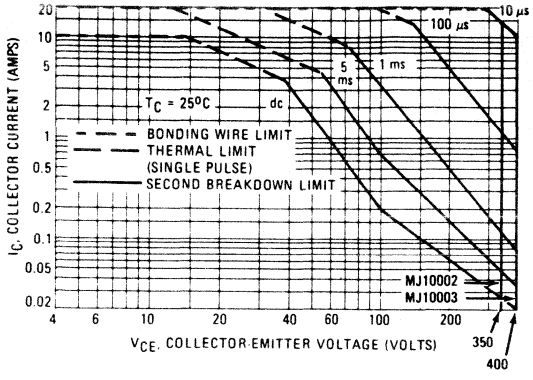
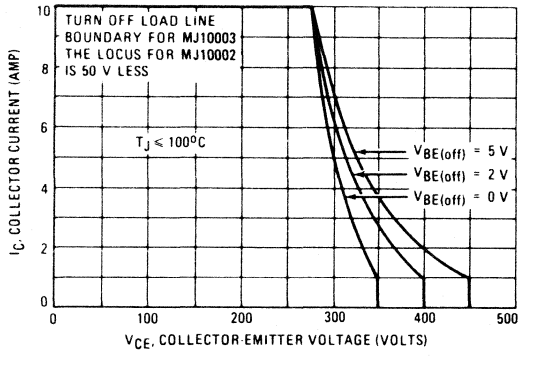


FIGURE 12 – REVERSE BIASED SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

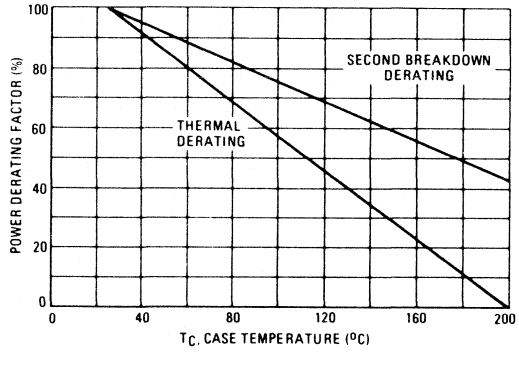
The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



MOTOROLA Semiconductors

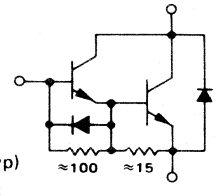
MJ10004
MJ10005

Designers▲ Data Sheet

SWITCHMODE▲ SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10004 and MJ10005 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
- 40 ns Inductive Fall Time – 25°C (Typ)
- 650 ns Inductive Storage Time – 25°C (Typ)

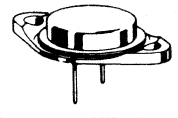
Operating Temperature Range -65 to +200°C

100°C Performance Specified for:
- Reversed Biased SOA with Inductive Loads
- Switching Times with Inductive Loads
- Saturation Voltages
- Leakage Currents

20 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
350 and 400 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

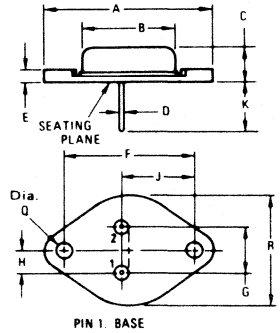


MAXIMUM RATINGS

Rating	Symbol	MJ10004	MJ10005	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous – Peak	I_C I_{CM}	20 30		Adc
Base Current – Continuous – Peak	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C



PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case
CASE 11-01
TO-3

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DS3300

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10004		350	–	–	
	MJ10005		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)		$V_{CEX(sus)}$				Vdc
(I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10004		400	–	–	
	MJ10005		450	–	–	
(I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10004		275	–	–	
	MJ10005		325	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)		I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				–
(I_C = 5 Adc, V_{CE} = 5 Vdc)			50	–	600	
(I_C = 10 Adc, V_{CE} = 5 Vdc)			40	–	400	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 400 mAdc)			–	–	1.9	
(I_C = 20 Adc, I_B = 1 Adc)			–	–	3	
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)			–	–	2	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 400 mAdc)			–	–	2.5	
(I_C = 10 Adc, I_B = 400 mAdc, T_C = 100°C)			–	–	2.5	
Diode Forward Voltage (1) (I_F = 10 Adc)		V_f	–	3	5	Vdc
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		$\lvert h_{fe} \rvert$	10	–	–	–
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	100	–	325	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%).	t_d	–	0.12	0.2	μs
Rise Time		t_r	–	0.2	0.5	μs
Storage Time		t_s	–	0.6	1.25	μs
Fall Time		t_f	–	0.15	0.35	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_s	–	0.85	2	μs
Fall Time		t_f	–	0.1	0.25	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_s	–	0.65	–	μs
Fall Time		t_f	–	0.04	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

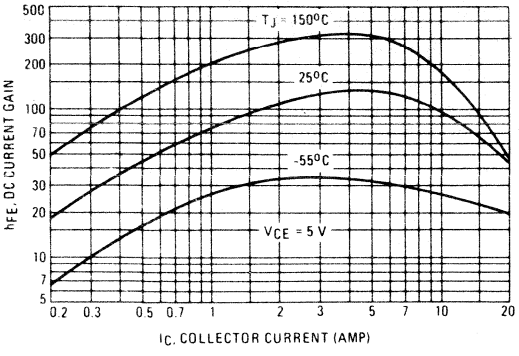


FIGURE 2 – COLLECTOR SATURATION REGION

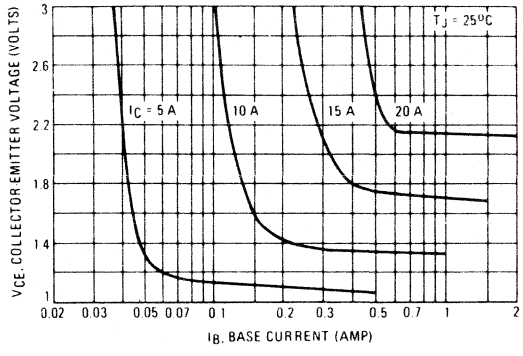


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

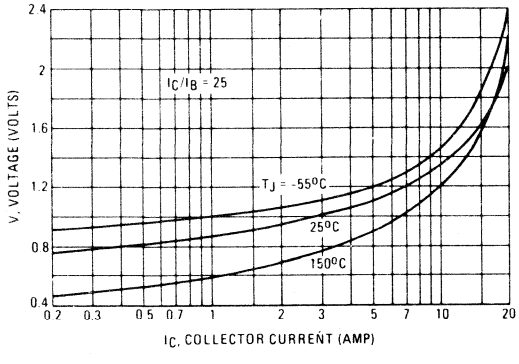


FIGURE 4 – BASE-EMITTER VOLTAGE

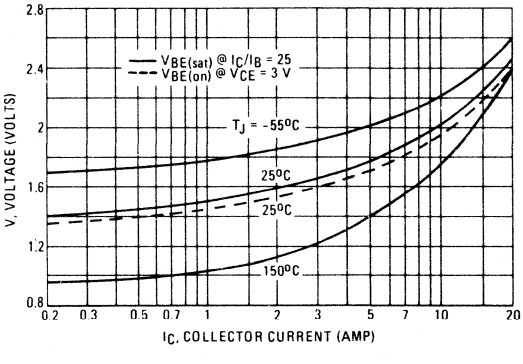


FIGURE 5 – COLLECTOR CUTOFF REGION

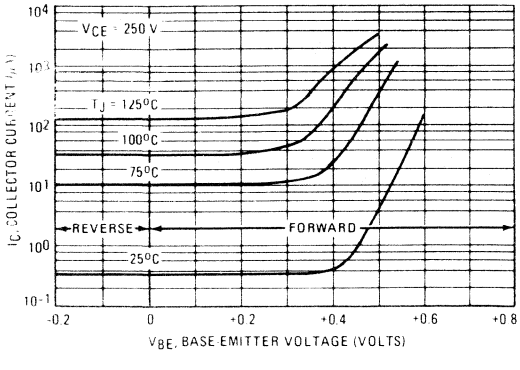


FIGURE 6 – OUTPUT CAPACITANCE

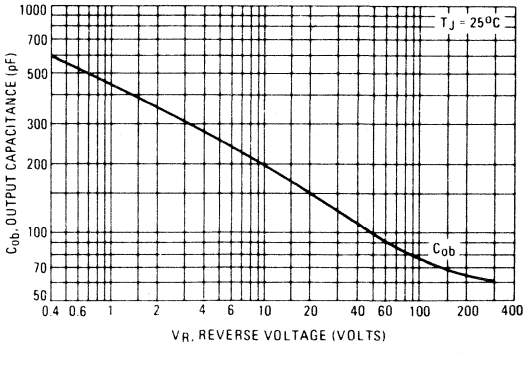


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

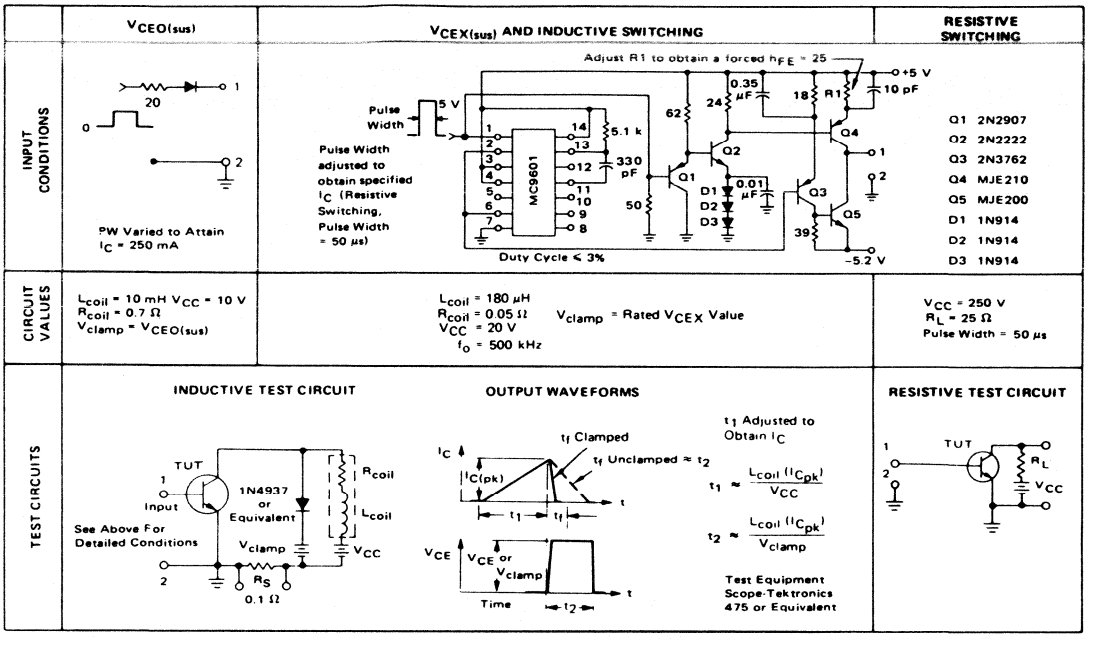


FIGURE 7 – TYPICAL TURN-OFF WAVEFORMS

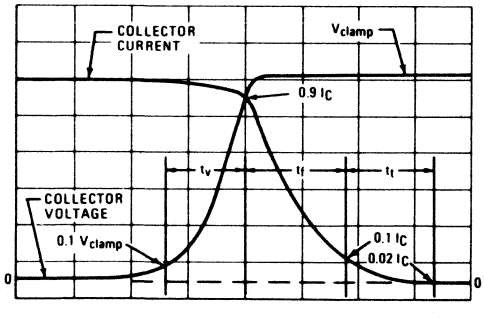


TABLE 2 – INDUCTIVE SWITCHING PERFORMANCE

IC Amps	TC °C	ts μs	tv μs	tf μs	tt μs	tv+tf+tt μs
5	25	0.52	0.08	0.02	0.05	0.15
	100	0.68	0.09	0.08	0.10	0.27
10	25	0.65	0.10	0.04	0.02	0.16
	100	0.85	0.11	0.10	0.03	0.24
15	25	0.83	0.12	0.10	0.02	0.24
	100	1.16	0.14	0.22	0.04	0.40

Note: All Data Recorded in the Inductive Switching Circuit shown in Table 1.

SWITCHING TIMES NOTE

To facilitate volume production testing, maximum inductive switching limits for these transistors are specified using conventional measurement techniques, e.g. t_s(max) is measured from the point where I_{B1} has decreased 10% to the point where I_C has decreased 10%, and t_f(max) is measured between the 90% and 10% points on the I_C waveform. In most applications, a large percentage of the total device power dissipation occurs during the fall time and t_f is normally used as a figure of merit when choosing a device for a switch-mode application. However, there are two portions of the turn-off waveform that can add losses and in some cases these losses can become a significant portion of the total device dissipation.

Figure 7 shows an enlarged portion of the inductive switching waveform during turn-off. The interval labeled t_v is part of the storage time interval (t_s) and is defined as voltage switching time. During this interval the transistor collector to emitter voltage changes from a saturation level to a level equal to or approaching the clamp voltage while the collector current has only changed by 10%. Typical values for this time interval at various current levels are shown in Table 2 at 25°C and 100°C case temperature.

– continued –

TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

The time interval labeled t_t occurs after the fall time and appears as a "tail" on the trailing edge of the collector current waveform. It is measured, for this discussion, from the 10% point to the 2% point; and during this interval the collector to emitter voltage is equal to the clamp voltage. Typical values for these time intervals are also shown in Table 2.

Since power dissipation occurs during the total time period $t_v + t_f + t_t$ and each interval can be affected by external conditions, some applications may require a specific analysis in order to accurately predict total device dissipation.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

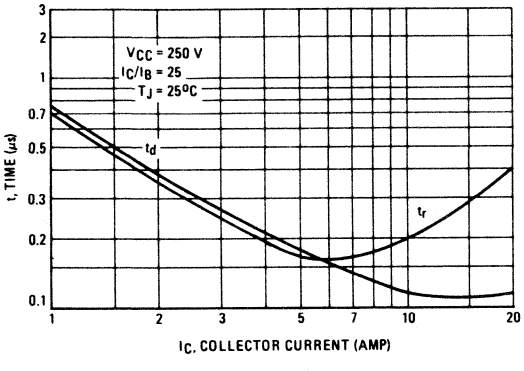


FIGURE 9 – TURN-OFF TIME

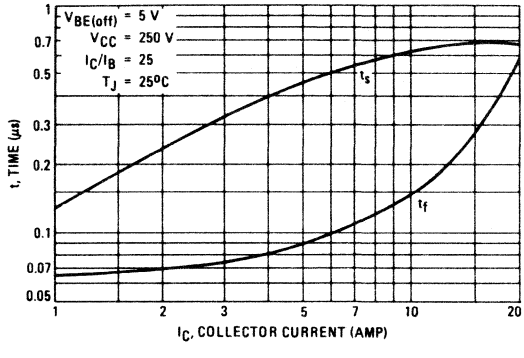
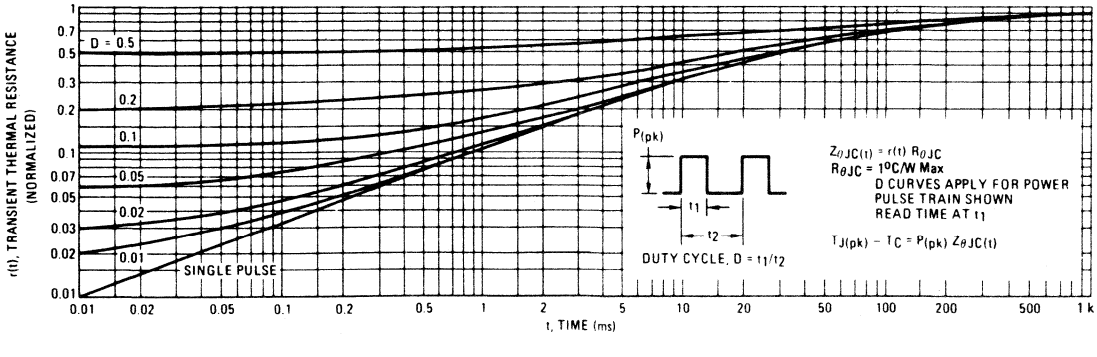


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

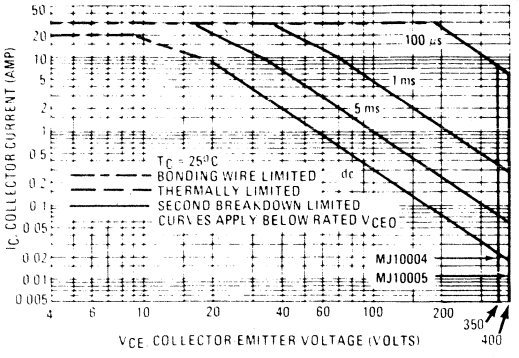
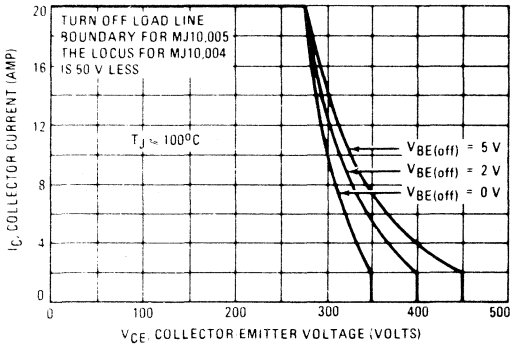


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

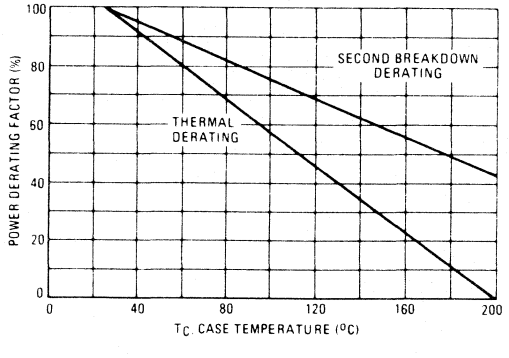
The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



MOTOROLA

SEMICONDUCTORS

MJ10006
MJ10007

Designers Data Sheet

10 AMPERE

NPN SILICON

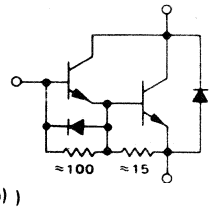
POWER DARLINGTON TRANSISTORS

350 AND 400 VOLTS
150 WATTS

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10006 and MJ10007 darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

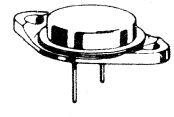
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times
30 ns Inductive Fall Time – 25°C (Typ)
500 ns Inductive Storage Time – 25°C (Typ))
Operating Temperature Range -65 to +200°C
100°C Performance Specified for:
Reversed Biased SOA with Inductive Loads
Switching Times with Inductive Loads
Saturation Voltages
Leakage Currents

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



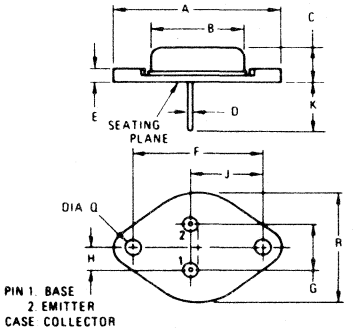
MAXIMUM RATINGS

Rating	Symbol	MJ10006	MJ10007	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	350	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	400	450	Vdc
Collector-Emitter Voltage	V_{CEV}	450	500	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	10 20		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	150 100 0.86		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

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DS3299 R1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 250 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10006		350	–	–	
	MJ10007		400	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)		$V_{CEX(sus)}$				Vdc
(I_C = 1 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10006		400	–	–	
	MJ10007		450	–	–	
(I_C = 5 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	MJ10006		275	–	–	
	MJ10007		325	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	–	5	mAdc
Emitter Cutoff Current (V_{EB} = 2 Vdc, I_C = 0)		I_{EBO}	–	–	175	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				–
(I_C = 2.5 Adc, V_{CE} = 5 Vdc)			40	–	500	
(I_C = 5 Adc, V_{CE} = 5 Vdc)			30	–	300	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 250 mAdc)			–	–	1.9	
(I_C = 10 Adc, I_B = 1 Adc)			–	–	2.9	
(I_C = 5 Adc, I_B = 250 mAdc, T_C = 100°C)			–	–	2	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 5 Adc, I_B = 250 mAdc)			–	–	2.5	
(I_C = 5 Adc, I_B = 250 mAdc, T_C = 100°C)			–	–	2.5	
Diode Forward Voltage (1) (I_F = 5 Adc)		V_f	–	3	5	Vdc
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)		$\lvert h_{fe} \rvert$	10	–	–	
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	60	–	275	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 5 A, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05	0.2	μs
Rise Time		t_r	–	0.25	0.6	μs
Storage Time		t_s	–	0.5	1.5	μs
Fall Time		t_f	–	0.06	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 5 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	0.8	2.0	μs
Crossover Time		t_c	–	0.6	1.5	μs
Storage Time	(I_C = 5 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 250 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_{sv}	–	0.5	–	μs
Crossover Time		t_c	–	0.3	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

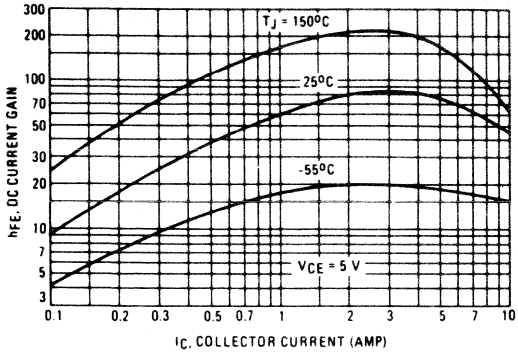


FIGURE 2 – COLLECTOR SATURATION REGION

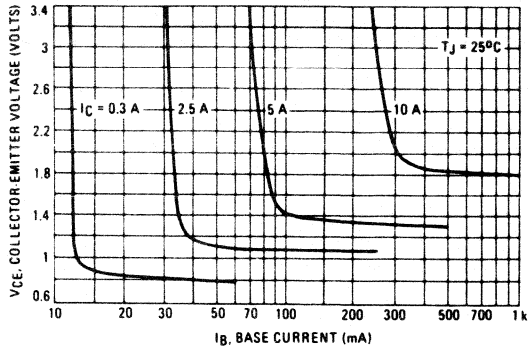


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

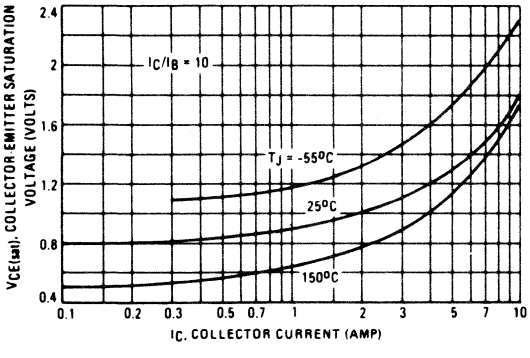


FIGURE 4 – BASE-EMITTER VOLTAGE

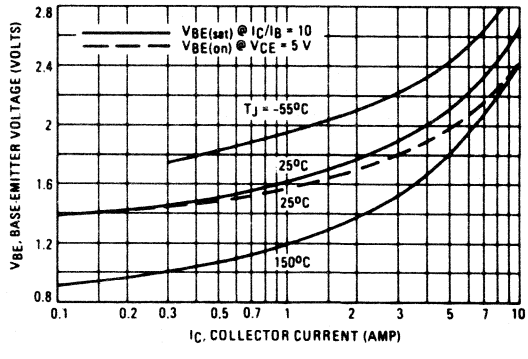


FIGURE 5 – COLLECTOR CUTOFF REGION

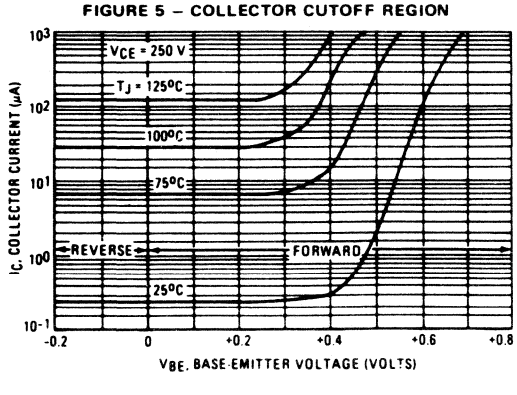


FIGURE 6 – OUTPUT CAPACITANCE

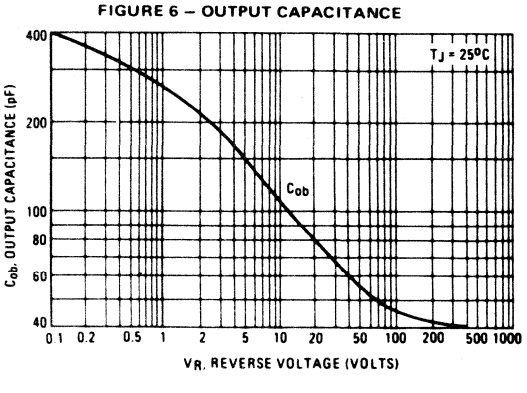
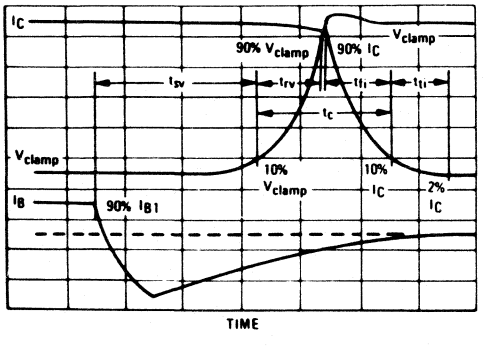


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	PW Varied to Attain I_C = 250 mA	Adjust R1 to obtain a forced h_{FE} = 20; Pulse Width adjusted to obtain I_C (Resistive Switching, Pulse Width = 50 μs); Duty Cycle < 3%	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V f_o = 500 kHz V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT See Above For Detailed Conditions	OUTPUT WAVEFORMS t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$ Test Equipment Scope-Tektronix 475 or Equipment	RESISTIVE TEST CIRCUIT

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

TYPICAL CHARACTERISTICS

SWITCHING TIME NOTES (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

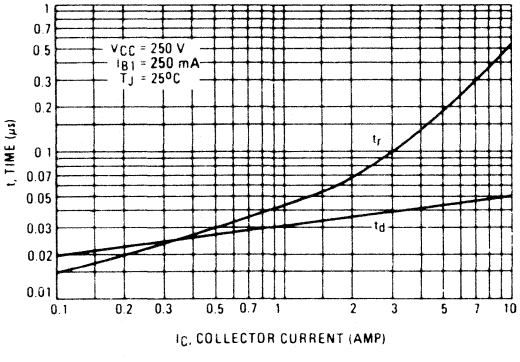


FIGURE 9 – TURN-OFF TIME

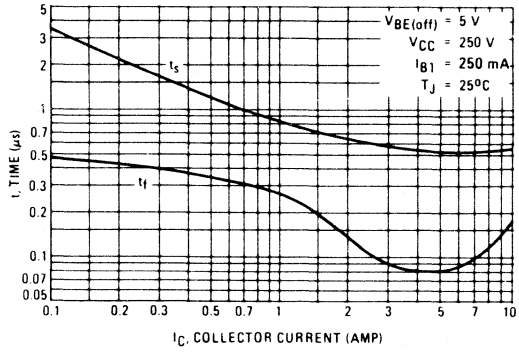
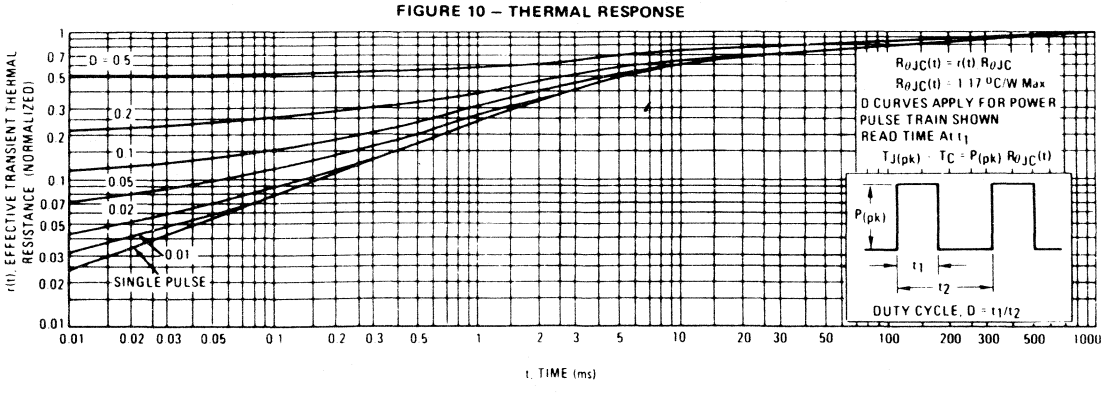


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

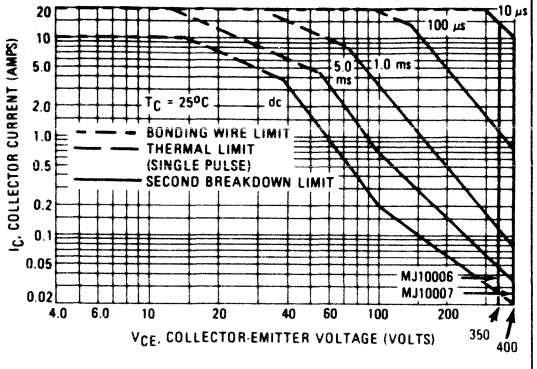
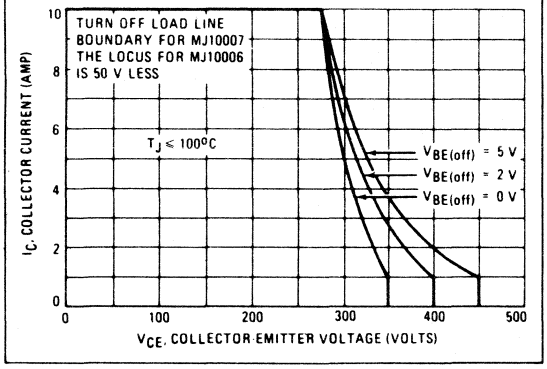


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

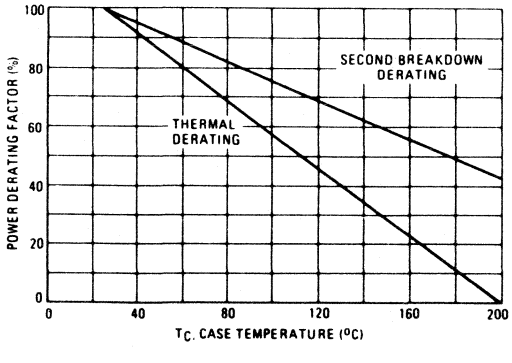
The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



MOTOROLA Semiconductors

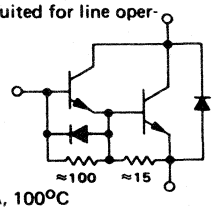
MJ10008
MJ10009

Designers▲ Data Sheet

SWITCHMODE▲ SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS
WITH BASE-EMITTER SPEEDUP DIODE

The MJ10008 and MJ10009 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



Fast Turn-Off Times

1.6 μs (max) Inductive Crossover Time – 10 A, 100°C

3.5 μs (max) Inductive Storage Time – 10 A, 100°C

Operating Temperature Range -65 to +200°C

100°C Performance Specified for:

Reversed Biased SOA with Inductive Loads

Switching Times with Inductive Loads

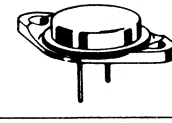
Saturation Voltages

Leakage Currents

20 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
450 and 500 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers▲ Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.



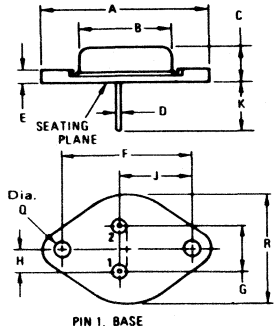
MAXIMUM RATINGS

Rating	Symbol	MJ10008	MJ10009	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	450	500	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	450	500	Vdc
Collector-Emitter Voltage	V_{CEV}	650	700	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	20 30		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	2.5 5		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

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DS 3327

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10008		450	–	–	
	MJ10009		500	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)		$V_{CEX(sus)}$				Vdc
(I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C,	MJ10008		450	–	–	
$V_{BE(off)}$ = 5 V)	MJ10009		500	–	–	
(I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C,	MJ10008		325	–	–	
$V_{BE(off)}$ = 5 V)	MJ10009		375	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.25	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5	
Collector Cutoff Current		I_{CER}	–	–	5	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)						
Emitter Cutoff Current		I_{EBO}	–	–	175	mAdc
(V_{EB} = 2 Vdc, I_C = 0)						
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				–
(I_C = 5 Adc, V_{CE} = 5 Vdc)			40	–	400	
(I_C = 10 Adc, V_{CE} = 5 Vdc)			30	–	300	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 500 mAdc)			–	–	2	
(I_C = 20 Adc, I_B = 2 Adc)			–	–	3.5	
(I_C = 10 Adc, I_B = 500 mAdc, T_C = 100°C)			–	–	2.5	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 500 mAdc)			–	–	2.5	
(I_C = 10 Adc, I_B = 500 mAdc, T_C = 100°C)			–	–	2.5	
Diode Forward Voltage (1)		V_f	–	3	5	Vdc
(I_F = 10 Adc)						
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain		$\|h_{fe}\|$	8	–	–	–
(I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)						
Output Capacitance		C_{ob}	100	–	325	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)						
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 25 μs Duty Cycle ≤ 2%).	t_d	–	0.12	0.25	μs
Rise Time		t_r	–	0.5	1.5	μs
Storage Time		t_s	–	0.8	2.0	μs
Fall Time		t_f	–	0.2	0.6	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 V, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_{sv}	–	1.5	3.5	μs
Crossover Time		t_c	–	0.36	1.6	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 V, I_{B1} = 500 mA, $V_{BE(off)}$ = 5 Vdc)	t_{sv}	–	0.8	–	μs
Crossover Time		t_c	–	0.18	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

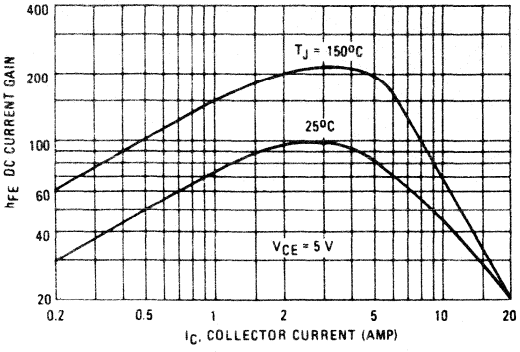


FIGURE 2 – COLLECTOR SATURATION REGION

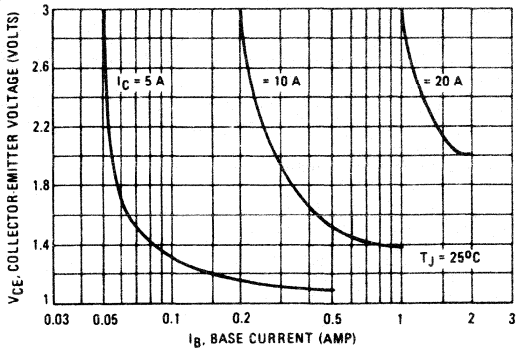


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

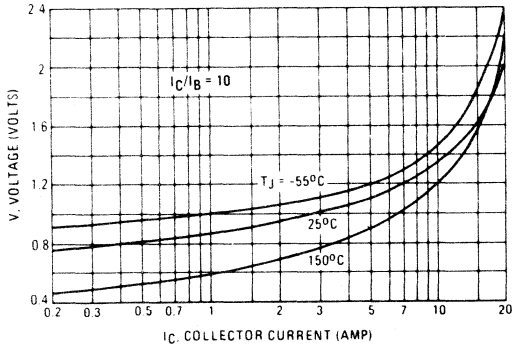


FIGURE 4 – BASE-EMITTER VOLTAGE

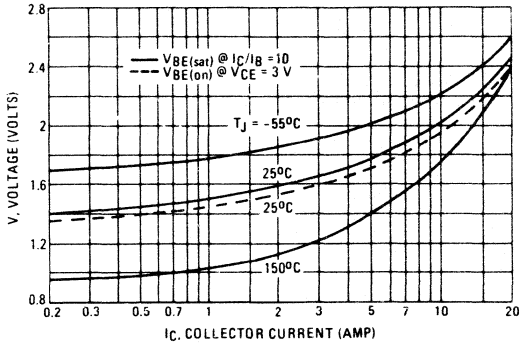


FIGURE 5 – COLLECTOR CUTOFF REGION

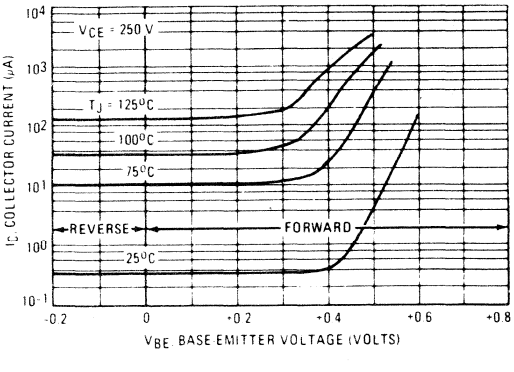


FIGURE 6 – OUTPUT CAPACITANCE

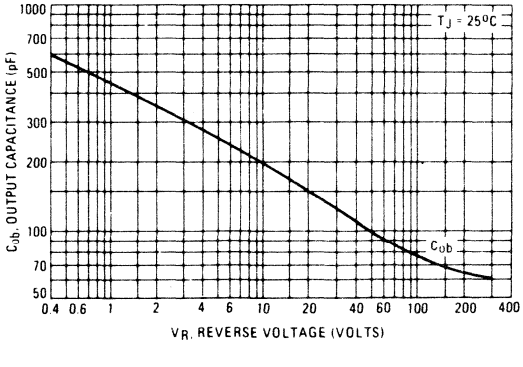
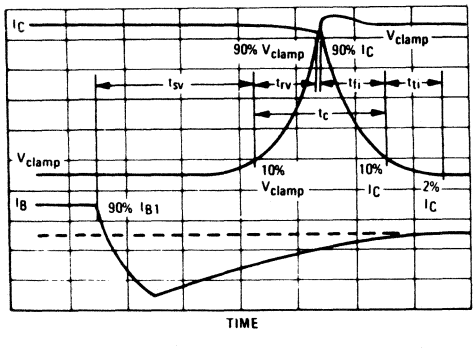


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	PW Varied to Attain I_C = 100 mA	Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 25 μs)	TURN-ON TIME: I_{B1} adjusted to obtain the forced h_{FE} desired. TURN-OFF TIME: Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1N4937 or Equivalent, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, R_S 0.1 Ω, See Above For Detailed Conditions	OUTPUT WAVEFORMS: t_f Clamped, t_f Unclamped ≈ t_2, t_1 Adjusted to Obtain I_C; $t_1 \approx \frac{L_{coil} I_{C(pk)}}{V_{CC}}$; $t_2 \approx \frac{L_{coil} I_{C(pk)}}{V_{clamp}}$; Test Equipment: Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT: TUT, R_L, V_{CC}

*Adjust –V such that $V_{BE(off)}$ = 5 V except as required for RB SOA (Figure 12).

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

– continued –

TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c)\ f$$

Typical inductive switching waveforms are shown in Figure 7. In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at $T_C = 25^oC$ and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at $T_C = 100^oC$.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

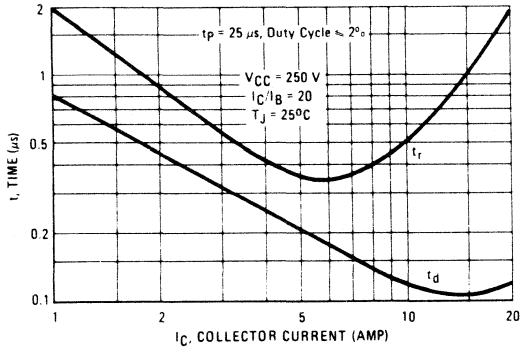


FIGURE 9 – TURN-OFF TIME

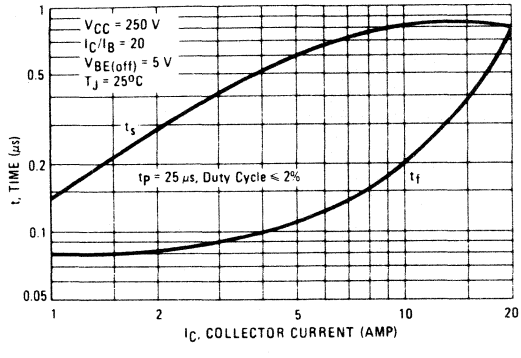
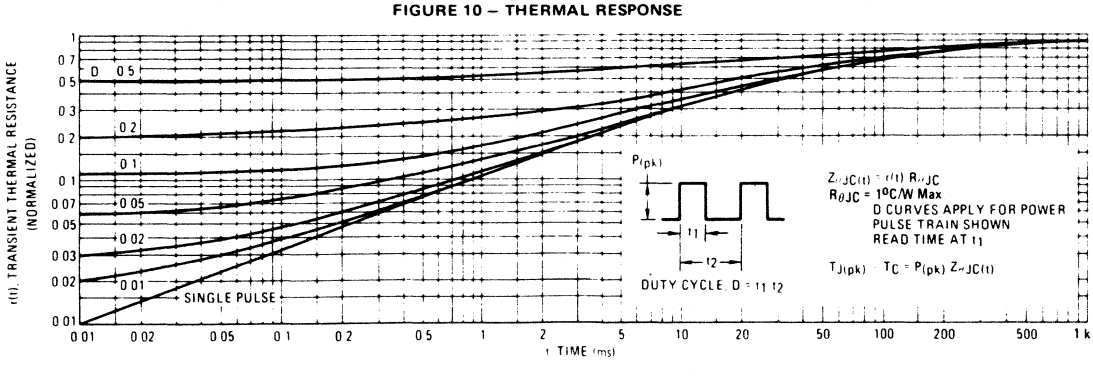


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

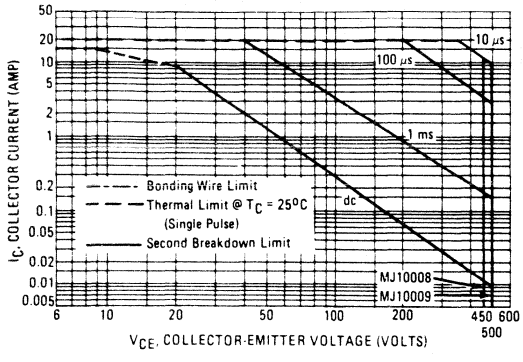
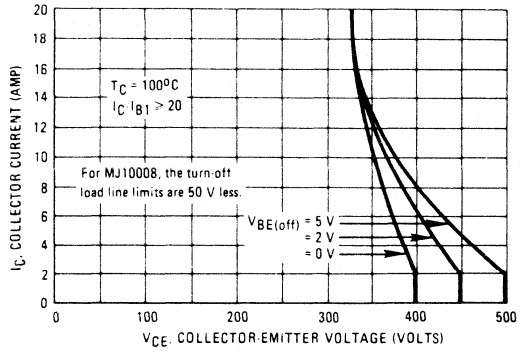


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA (MJ10009)



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics. See Table 1 for circuit conditions.

FIGURE 13 – POWER DERATING

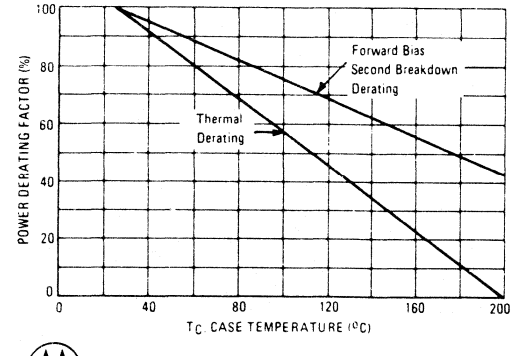
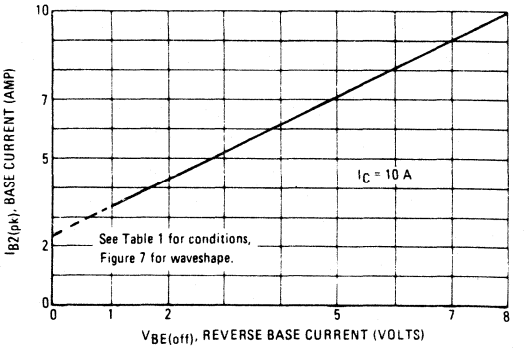


FIGURE 14 – REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



MOTOROLA

SEMICONDUCTORS

Designers Data Sheet

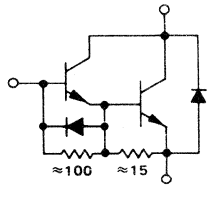
MJ10013
MJ10014

10 AMPERE
NPN SILICON
POWER DARLINGTON TRANSISTORS
550 AND 600 VOLTS
175 WATTS

SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS

The MJ10013 and MJ10014 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

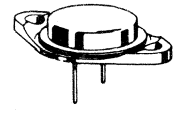
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls
- Deflection Circuits



- Fast Turn-Off Times
  - 500 ns Inductive Crossover Time—25°C (Typ)
  - 1.4 μs Inductive Storage Time—25°C (Typ)
- Operating Temperature Range: -65 to +200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA With Inductive Loads
  - Switching Times With Inductive Loads
  - Saturation Voltages
  - Leakage Currents

Designers Data for "Worst-Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data—representing device characteristic boundaries—are given to facilitate "worst-case" design.



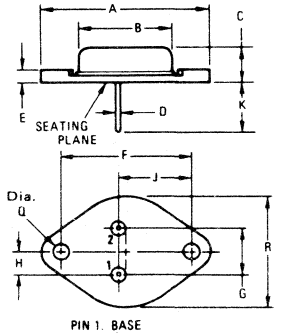
MAXIMUM RATINGS

Rating	Symbol	MJ10013	MJ10014	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	550	600	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	600	650	Vdc
Collector-Emitter Voltage	V_{CEV}	650	700	Vdc
Emitter Base Voltage	V_{EB}	8		Vdc
Collector Current — Continuous — Peak (1)	I_C I_{CM}	10 15		Adc
Base Current — Continuous — Peak (1)	I_B I_{BM}	7 10		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	175 100 1		Watts W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%



PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

Collector connected to case.
CASE 11-01
TO-3

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DS 3349

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (Table 1)		$V_{CEO(sus)}$				Vdc
(I_C = 100 mA, I_B = 0)	MJ10013		550	–	–	
	MJ10014		600	–	–	
Collector-Emitter Sustaining Voltage (Table 1, Figure 12)		$V_{CEX(sus)}$				Vdc
(I_C = 2 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C,	MJ10013		600	–	–	
$V_{BE(off)}$ = 5 V, $I_C/I_B \geq 5$)	MJ10014		650	–	–	
(I_C = 10 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C,	MJ10013		425	–	–	
$V_{BE(off)}$ = 5 V, $I_C/I_B \geq 5$)	MJ10014		475	–	–	
Collector Cutoff Current		I_{CEV}				mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)			–	–	0.3	
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)			–	–	5	
Collector Cutoff Current		I_{CER}	–	–	5	mAdc
(V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)						
Emitter Cutoff Current		I_{EBO}	–	–	175	mAdc
(V_{EB} = 2 Vdc, I_C = 0)						
SECOND BREAKDOWN						
Second Breakdown Collector Current with base forward biased		$I_{S/b}$	See Figure 11			
ON CHARACTERISTICS (2)						
DC Current Gain		h_{FE}				–
(I_C = 5 Adc, V_{CE} = 5 Vdc)			20	–	500	
(I_C = 10 Adc, V_{CE} = 5 Vdc)			10	–	250	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2 Adc)			–	–	2.5	
(I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)			–	–	2.6	
Base-Emitter Saturation Voltage		$V_{BE(sat)}$				Vdc
(I_C = 10 Adc, I_B = 2 Adc)			–	–	3	
(I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)			–	–	3	
Diode Forward Voltage (1)		V_f	–	3	5	Vdc
(I_F = 10 Adc)						
DYNAMIC CHARACTERISTICS						
Small-Signal Current Gain		$\lvert h_{fe} \rvert$	10	–	–	–
(I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)						
Output Capacitance		C_{ob}	100	–	350	pF
(V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)						
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 10 A, I_{B1} = 400 mA, $V_{BE(off)}$ = 5 Vdc, t_p = 50 μs, Duty Cycle ≤ 2%).	t_d	–	0.02	0.2	μs
Rise Time		t_r	–	0.9	2	μs
Storage Time		t_s	–	0.95	4	μs
Fall Time		t_f	–	0.22	1	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 100°C)	t_s	–	2.3	6	μs
Crossover Time		t_c	–	1	3	μs
Storage Time	(I_C = 10 A(pk), V_{clamp} = 250 Vdc, I_{B1} = 1 A, $V_{BE(off)}$ = 5 Vdc, T_C = 25°C)	t_s	–	1.4	–	μs
Crossover Time		t_c	–	0.5	–	μs

(1) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

(2) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

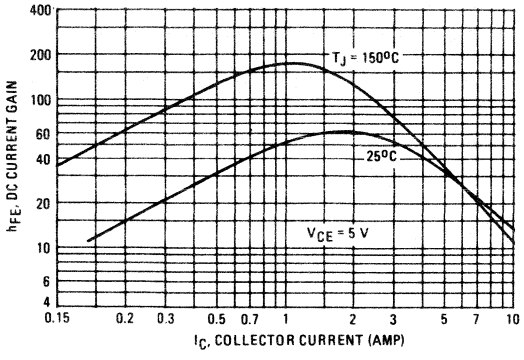


FIGURE 2 – COLLECTOR SATURATION REGION

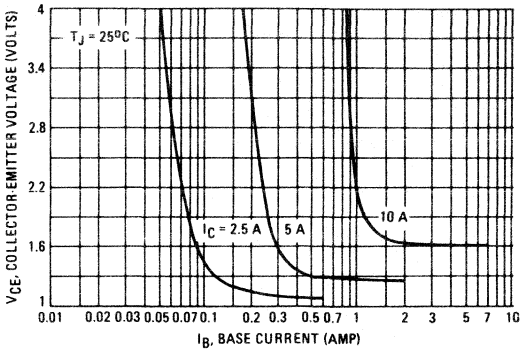


FIGURE 3 – COLLECTOR-EMITTER SATURATION VOLTAGE

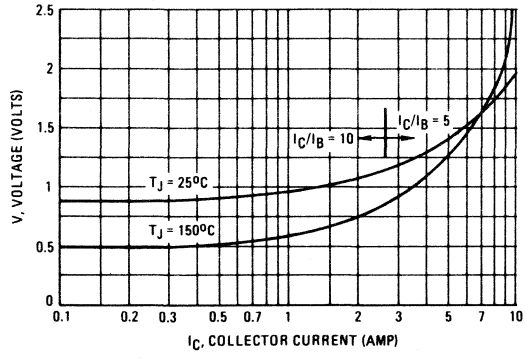


FIGURE 4 – BASE-EMITTER VOLTAGE

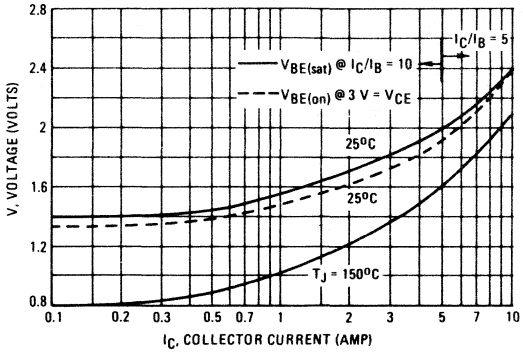


FIGURE 5 – COLLECTOR CUTOFF REGION

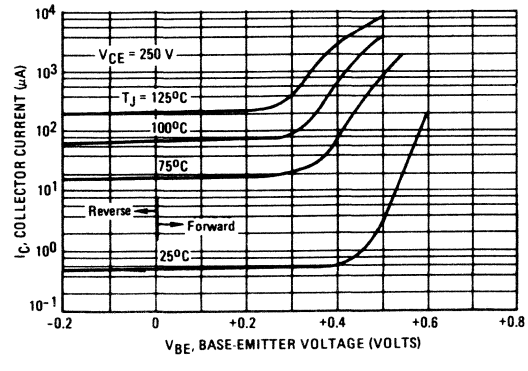


FIGURE 6 – OUTPUT CAPACITANCE

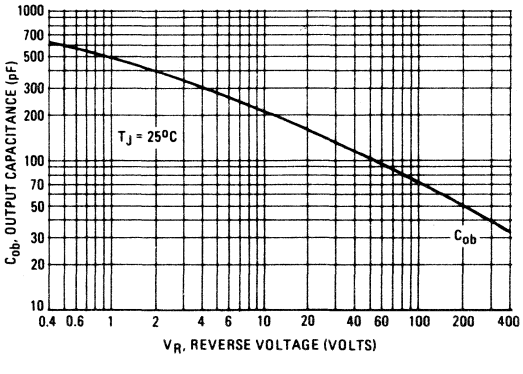
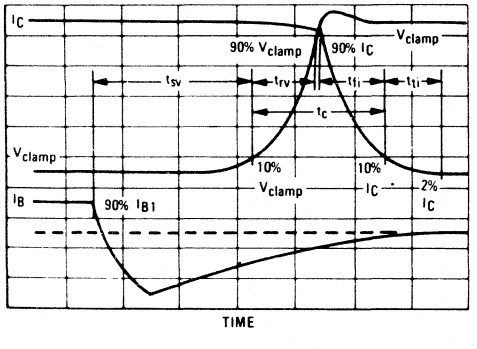


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	$V_{CEX(sus)}$ AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	PW Varied to Attain I_C = 250 mA	Adjust R1 to obtain a forced h_{FE} = 10; Pulse Width; Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 50 μs); Duty Cycle ≤ 3%	Q1 2N2907 Q2 2N2222 Q3 2N3762 Q4 MJE210 Q5 MJE200 D1 1N914 D2 1N914 D3 1N914
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V R_{coil} = 0.7 Ω V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = Rated V_{CEX} Value	V_{CC} = 250 V R_L = 25 Ω Pulse Width = 50 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1N4937 or Equivalent, See Above For Detailed Conditions, 0.1 Ω	OUTPUT WAVEFORMS: t_f Clamped, t_f Unclamped ≈ t_2; t_1 Adjusted to Obtain I_C; $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$; $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$; Test Equipment Scope Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT: TUT, R_L, V_{CC}

FIGURE 7 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIME NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10–90% V_{clamp}
t_{fi} = Current Fall Time, 90–10% I_C
t_{ti} = Current Tail, 10–2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the turn-off waveforms is shown in Figure 7 to aid in the visual identity of these terms.

– continued –

TYPICAL CHARACTERISTICS

SWITCHING TIMES NOTE (continued)

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C(t_c)\ f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

FIGURE 8 – TURN-ON TIME

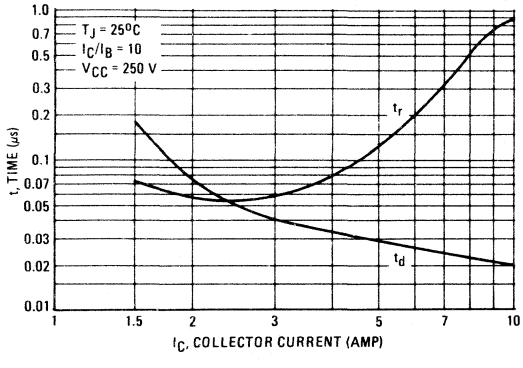


FIGURE 9 – TURN-OFF TIME

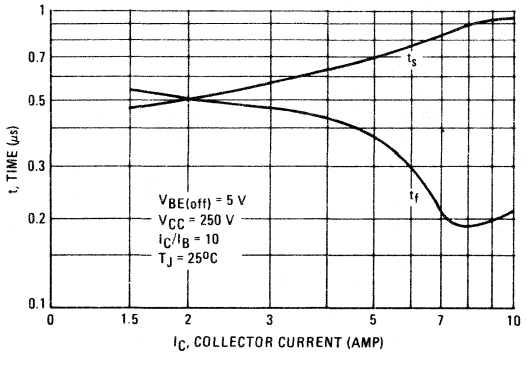
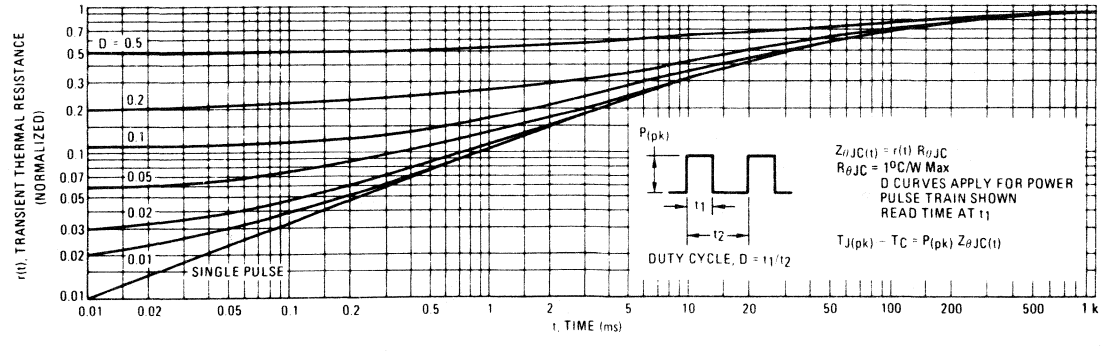


FIGURE 10 – THERMAL RESPONSE



The Safe Operating Area figures shown in Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

FIGURE 11 – FORWARD BIAS SAFE OPERATING AREA

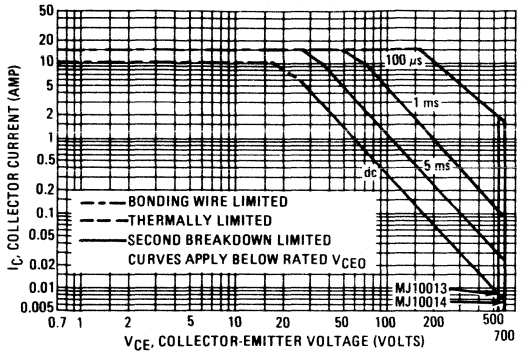
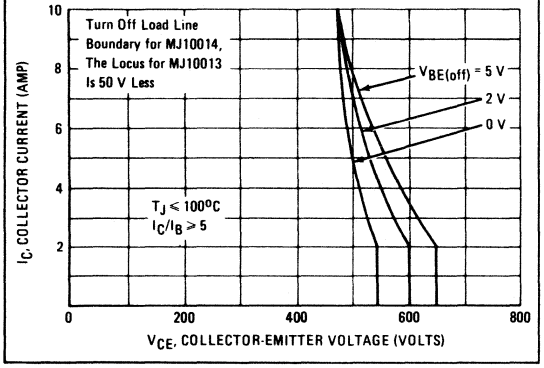


FIGURE 12 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

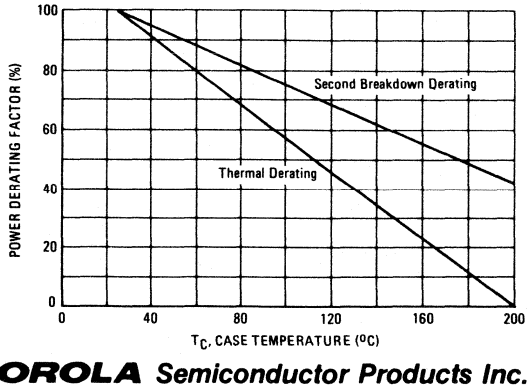
The data of Figure 11 is based on $T_C = 25^oC$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^oC$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as $V_{CEX(sus)}$ at a given collector current and represents a voltage-current condition that can be sustained during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete reverse bias safe operating area characteristics.

FIGURE 13 – POWER DERATING



MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MJ10015
MJ10016

50 AMPERE

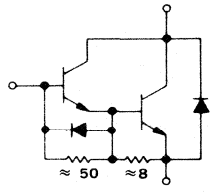
NPN SILICON
POWER DARLINGTON
TRANSISTORS

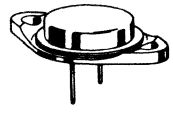
400 and 500 VOLTS
250 WATTS

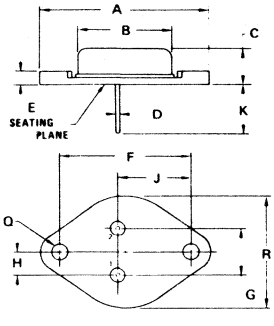
SWITCHMODE SERIES
NPN SILICON POWER DARLINGTON TRANSISTORS WITH BASE-EMITTER SPEEDUP DIODE

The MJ10015 and MJ10016 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications such as:

- Switching Regulators
- Motor Controls
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  - 1.0 μs (max) Inductive Crossover Time – 20 Amps
  - 2.5 μs (max) Inductive Storage Time – 20 Amps
- Operating Temperature Range –65 to +200°C
- Performance Specified for
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents







STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.35	39.37	1.510	1.550
B	19.30	21.08	0.760	0.830
C	6.35	7.62	0.250	0.300
D	1.45	1.60	0.057	0.063
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.21	5.72	0.205	0.225
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	24.89	26.67	0.980	1.050

CASE 197-01
MODIFIED TO-3

MAXIMUM RATINGS

Rating	Symbol	MJ10015	MJ10016	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	500	Vdc
Collector-Emitter Voltage	V_{CEV}	600	700	Vdc
Emitter Base Voltage	V_{EB}	8.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	50 75		Adc
Base Current – Continous – Peak (1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above 25°C	P_D	250 143 1.43		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%

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DS 3360
(Replaces ADI 440)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)						
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0, V_{clamp} = Rated V_{CEO})	MJ10015 MJ10016	$V_{CEO(sus)}$	 400 500	 – –	 – –	Vdc
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	–	0.25	mAdc
Emitter Cutoff Current (V_{EB} = 2.0 Vdc, I_C = 0)		I_{EBO}	–	–	350	mAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 7			
Clamped Inductive SOA with Base Reverse Biased		RBSOA	See Figure 8			
ON CHARACTERISTICS (1)						
DC Current Gain (I_C = 20 Adc, V_{CE} = 5.0 Vdc) (I_C = 40 Adc, V_{CE} = 5.0 Vdc)		h_{FE}	 25 10	 – –	 – –	–
Collector-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc) (I_C = 50 Adc, I_B = 10 Adc)		$V_{CE(sat)}$	 – –	 – –	 2.2 5.0	Vdc
Base-Emitter Saturation Voltage (I_C = 20 Adc, I_B = 1.0 Adc)		$V_{BE(sat)}$	–	–	2.75	Vdc
Diode Forward Voltage (2) (I_F = 20 Adc)		V_f	–	2.5	5.0	Vdc
DYNAMIC CHARACTERISTIC						
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 100 kHz)		C_{ob}	–	–	750	pF
SWITCHING CHARACTERISTICS						
Resistive Load (Table 1)						
Delay Time	(V_{CC} = 250 Vdc, I_C = 20 A, I_{B1} = 1.0 Adc, $V_{BE(off)}$ = 5 Vdc, t_p = 25 μs Duty Cycle ≤ 2%).	t_d	–	0.14	0.3	μs
Rise Time		t_r	–	0.3	1.0	μs
Storage Time		t_s	–	0.8	2.5	μs
Fall Time		t_f	–	0.3	1.0	μs
Inductive Load, Clamped (Table 1)						
Storage Time	(I_C = 20 A(pk), V_{clamp} = 250 V, I_{B1} = 1.0 A, $V_{BE(off)}$ = 5.0 Vdc)	t_{sv}	–	1.0	2.5	μs
Crossover Time		t_c	–	0.36	1.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

(2) The internal Collector-to-Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage (V_f) of this diode is comparable to that of typical fast recovery rectifiers.

TYPICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

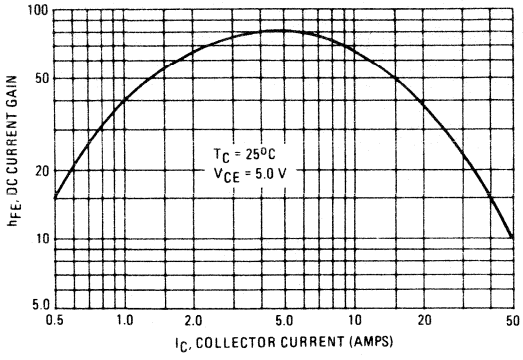


FIGURE 2 – COLLECTOR-EMITTER SATURATION VOLTAGE

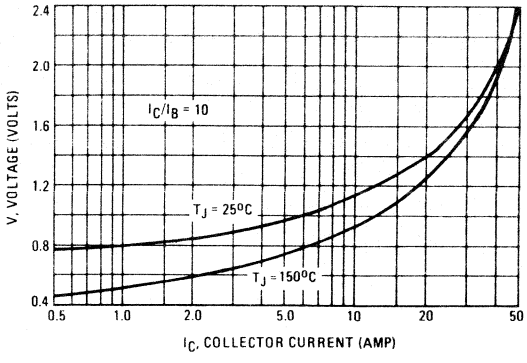


FIGURE 3 – BASE-EMITTER SATURATION VOLTAGE

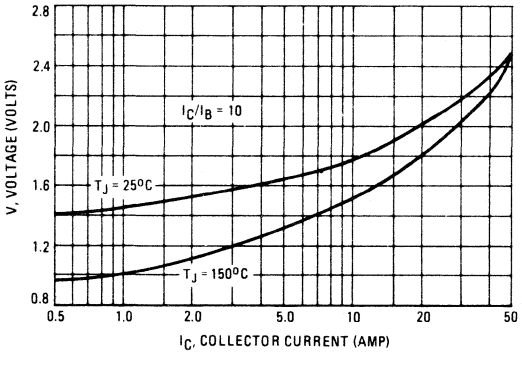


FIGURE 4 – COLLECTOR CUTOFF REGION

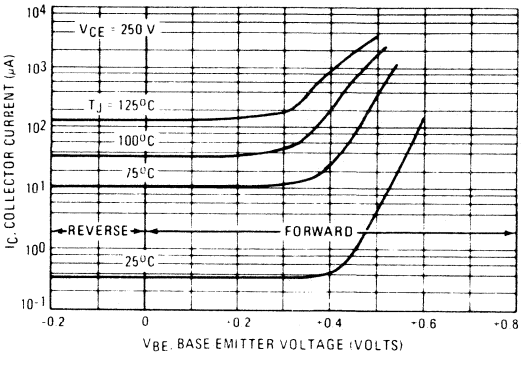


FIGURE 5 – OUTPUT CAPACITANCE

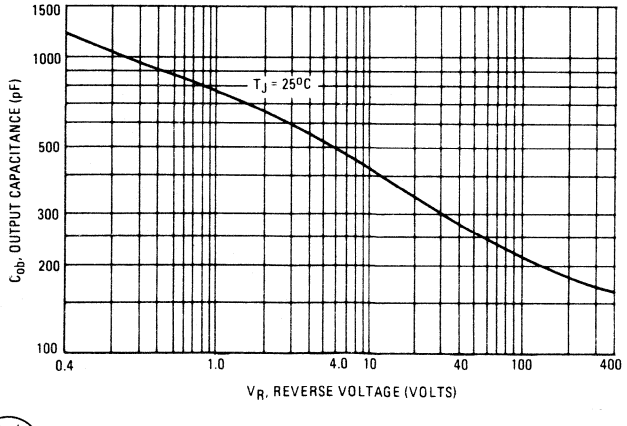
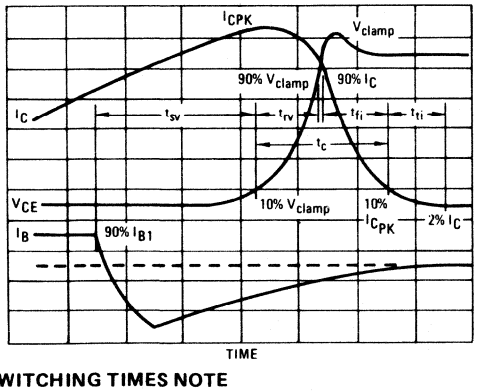


TABLE 1 – TEST CONDITIONS FOR DYNAMIC PERFORMANCE

	$V_{CEO(sus)}$	V_{CEX} AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	20 Ω, 5 V, PW Varied to Attain I_C = 100 mA	Pulse Width adjusted to obtain specified I_C (Resistive Switching, Pulse Width = 25 μs); Adjust R1 to obtain a forced h_{FE} = 20; Duty Cycle ≤ 3%	TURN-ON TIME: I_{B1} adjusted to obtain the forced h_{FE} desired. TURN-OFF TIME: Use inductive switching circuit as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 10 mH V_{CC} = 10 V, R_{coil} = 0.7 Ω, V_{clamp} = $V_{CEO(sus)}$	L_{coil} = 180 μH, R_{coil} = 0.05 Ω, V_{CC} = 20 V; Q1 2N2907, Q2 2N2222, Q3 2N3762, Q4 MJE210, Q5 MJE200, D1 1N914, D2 1N914, D3 1N914	V_{CC} = 250 V, R_L = 12.5 Ω, Pulse Width = 25 μs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT: TUT, 1N4937 or Equivalent, R_{coil}, L_{coil}, V_{clamp}, V_{CC}, R_S = 0.1 Ω, See Above for Detailed Conditions	OUTPUT WAVEFORMS: I_C, $I_{C(pk)}$, t_f Clamped, V_{CE}, V_{CE} or V_{clamp}, Time, t_1, t_2; t_1 Adjusted to Obtain I_C: $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$, $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$; Test Equipment: Scope – Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT: TUT, R_L, V_{CC}

*Adjust –V such that $V_{BE(off)}$ = 5 V except as required for RB SOA (Figure 12).

FIGURE 6 – INDUCTIVE SWITCHING MEASUREMENTS



SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10-90% V_{clamp}
t_{fi} = Current Fall Time, 90-10% I_C
t_{ti} = Current Tail, 10-2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \cong t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed.

The Safe Operating Area figures shown in Figures 7 and 8 are specified ratings for these devices under the test conditions shown.

FIGURE 7 – FORWARD BIAS SAFE OPERATING AREA

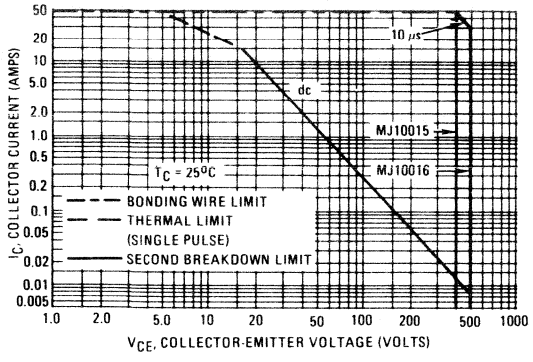
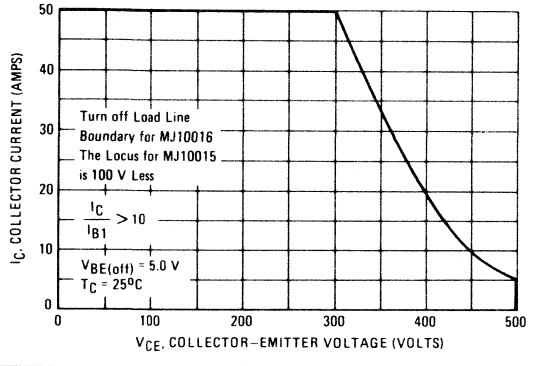


FIGURE 8 – REVERSE BIAS SWITCHING SAFE OPERATING AREA



SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 7 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geqslant 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 8 gives the complete RBSOA characteristics.

FIGURE 9 – POWER DERATING

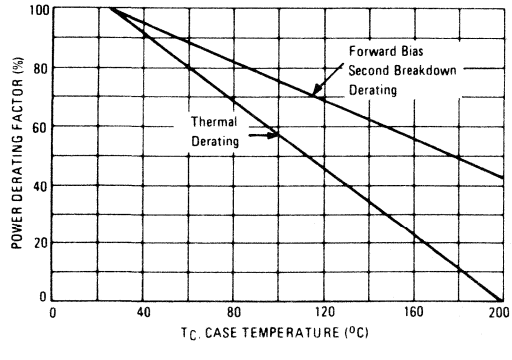
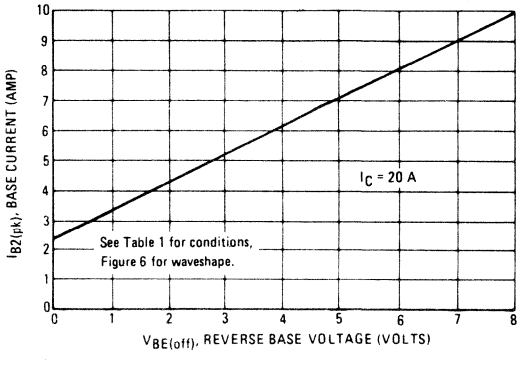


FIGURE 10 – TYPICAL REVERSE BASE CURRENT versus $V_{BE(off)}$ WITH NO EXTERNAL BASE RESISTANCE



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MOTOROLA *Semiconductor Products Inc.*

MOTOROLA Semiconductors

TL494
TL495

Advance Information

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

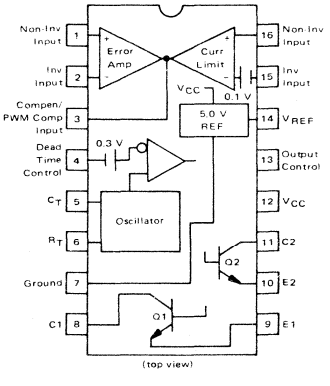
The TL494 and TL495 combine the best features of existing PWM control circuits and add other on-chip functions. These devices provide, on a single monolithic chip, all the control circuitry for PWM push-pull, bridge and series type switchmode power supplies.

The TL494M/495M are specified over the military operating range of -55°C to +125°C. The TL494C/495C are specified from 0°C to +70°C.

- Uncommitted Output Transistors Capable of 250 mA Source or Sink
- On-Chip Error Amplifier and Current Limit Sense Amplifier
- On-Chip 5 V Reference
- Internal Protection from Double Pulsing of Outputs with Narrow Pulse Widths or with Supply Voltages below Specified Limits
- Dead Time Control Comparator
- Pulse-Steering Flip-Flop and Output Control Circuitry
- Easily Synchronized (Slaved) to Other Circuits
- On-Chip 39 V Zener for High Voltage ($V_{IN} > 40$ V) Applications (TL495 only)
- Output Steering Control Pin Overrides Internal Pulse Steering Flip-Flop (TL495 only)

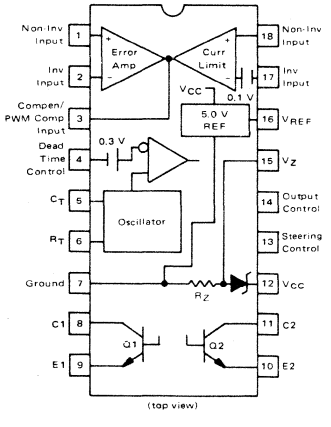
PIN CONNECTIONS

TL494



(top view)

TL495

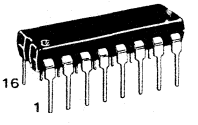


(top view)

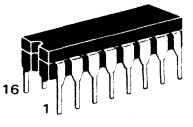
SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS

TL494

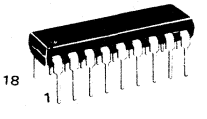


N SUFFIX
PLASTIC PACKAGE
CASE 648
(TL494C only)

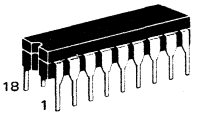


J SUFFIX
CERAMIC PACKAGE
CASE 620

TL495



N SUFFIX
PLASTIC PACKAGE
CASE 701-01
(TL495C only)



J SUFFIX
CERAMIC PACKAGE
CASE 726

ORDERING INFORMATION

Device	Temperature Range	Package
TL494CJ	0 to +70°C	Ceramic DIP
TL494CN	0 to +70°C	Plastic DIP
TL494MJ	-55 to +125°C	Ceramic DIP
TL495CJ	0 to +70°C	Ceramic DIP
TL495CN	0 to +70°C	Plastic DIP
TL495MJ	-55 to +125°C	Ceramic DIP

his is advance information and specifications are subject to change without notice.

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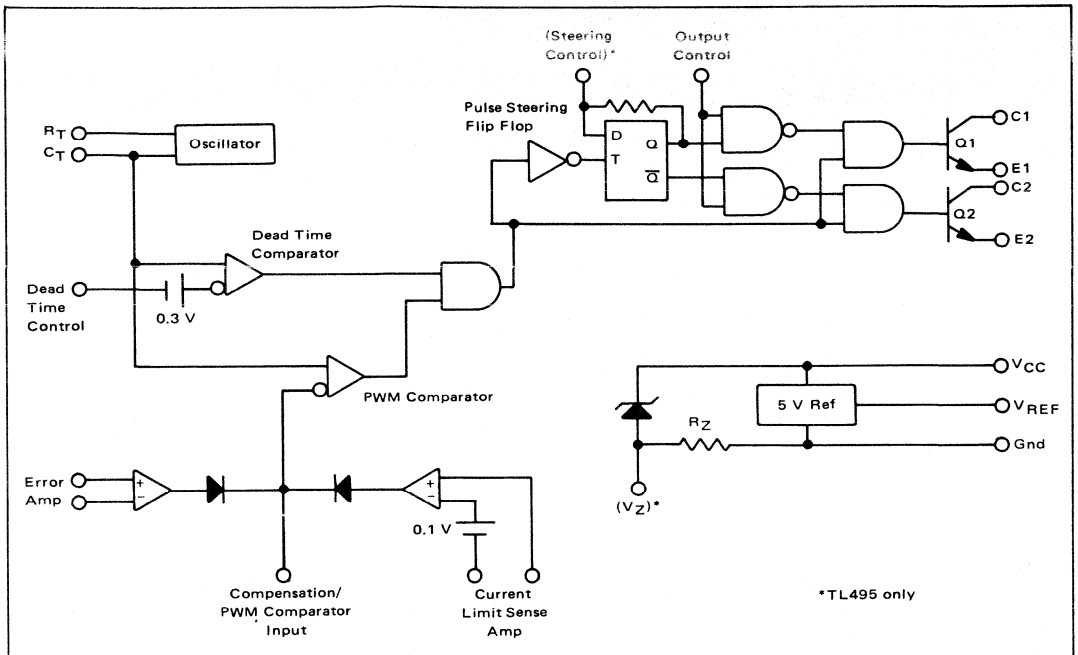
EQUIVALENT CIRCUIT



PIN ASSIGNMENTS

Device	R_T	C_T	Dead Time Cntrl	Error Amp +	Error Amp −	C.L. Sense +	C.L. Sense −	V_Z	Gnd	V_{REF}	V_{CC}	Q1 E1	Q1 C1	Q2 E2	Q2 C2	Output Cntrl	Steering Cntrl	Compen/ PWM Comp Input
TL494	6	5	4	1	2	16	15	N.A.	7	14	12	9	8	10	11	13	N.A.	3
TL495	6	5	4	1	2	18	17	15	7	16	12	9	8	10	11	14	13	3

MAXIMUM RATINGS (Operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	TL494M/495M	TL494C/495C	Unit
Power Supply Voltage	V_{CC}	42		V
Any Pin to Gnd except C1 and C2	V_{IN}	V_{CC} + 0.3		V
Output Voltage	V_{C1}, V_{C2}	42		V
Output Collector Current	I_{C1}, I_{C2}	250		mA
Power Dissipation ($T_A \leq 25^oC$)	P_D	1000 See Thermal Information		mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 – 150	 125 150	^oC
Operating Ambient Temperature Range	T_A	-55 to +125	0 to +70	^oC
Storage Temperature Range Ceramic Package Plastic Package	T_{stg}	 -65 to +150 –	 -65 to +150 -55 to +125	^oC

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL494C/TL495C Min	TL494C/TL495C Max	Unit
Power Supply Voltage	V_{CC}	7.0	40	V
Voltage on Any Pin Except C1 or C2 (Referenced to Ground)	V_{IN}	−0.3	V_{CC} + 0.3	V
Output Voltage	V_{C1}, V_{C2}	−0.3	40	V
Output Collector Current	I_{C1}, I_{C2}	–	200	mA
Timing Capacitor	C_T	470 –	– 10	pF μF
Timing Resistor	R_T	1.8	500	kΩ
Oscillator Frequency	f_{osc}	1.0	300	kHz
Operating Ambient Temperautre Range TL494C and TL495C	T_A	0	+70	°C

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions per above except V_{CC} = 15 V, f_{osc} = 10 kHz unless otherwise noted)

Characteristic	Symbol	TL494C/TL495C Min	TL494C/TL495C Typ	TL494C/TL495C Max	Unit
REFERENCE SECTION					
Reference Voltage (I_{REF} = 1.0 mA)	V_{REF}	4.75	5.0	5.25	V
Line Regulation of Reference Voltage (7.0 V ≤ V_{CC} ≤ 40 V)	Reg_{line}	–	2.0	25	mV
Temperature Coefficient of Reference Voltage (0°C ≤ T_A ≤ 70°C)	TCV_{REF}	–	0.01	0.03	%/°C
Load Regulation of Reference Voltage (0 ≤ I_{REF} ≤ 10 mA)	Reg_{load}	–	1.0	15	mV
OSCILLATOR SECTION					
Oscillator Frequency (C_T = 0.01 μF, R_T = 12 kΩ)	f_{osc}	–	10	–	kHz
Oscillator Frequency Change with Temperature 0°C ≤ T_A ≤ +70°C (C_T = 0.01 μF, R_T = 12 kΩ)	Δf_{osc}	–	–	2	%
DEAD-TIME CONTROL SECTION					
Input Bias Current (Pin 4) (V_{CC} = 15 V, 0 V ≤ V_{IN} ≤ 5.25 V)	$I_{IB(DT)}$	−10	−2.0	0	μA
Maximum Duty Cycle, Each Output (V_{CC} = 15 V, Pin 4 = 0 V, "Output Control" Pin = V_{REF})	DC_{max}	45	–	–	%
Input Threshold Voltage Zero Duty Cycle Maximum Duty Cycle	$V_{TH(in)}$	 – 0	 3.0 –	 3.3 –	V

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	TL494C/TL495C Min	Typ	Max	Unit
ERROR AND CURRENT LIMIT AMPLIFIER SECTIONS					
Error Amplifier Input Offset Voltage (V_{O3} = 2.5 V)	$V_{IO(EA)}$	–	2.0	10	mV
Current Limit Amplifier Input Offset Voltage (V_{ICM} = 0 V)	$V_{IO(CL)}$	88	110	132	mV
Input Offset Current (V_{O3} = 2.5 V)	I_{IO}	–	25	250	nA
Input Bias Current (V_{O3} = 2.5 V)	I_{IB}	–	0.2	1.0	μA
Input Common Mode Voltage Range (7 V ≤ V_{CC} ≤ 40 V)	V_{ICR}	-0.3	–	V_{CC} - 2.0	V
Large Signal Open Loop Voltage Gain (ΔV_{O3} = 3 V, 0.5 V ≤ V_{O3} ≤ 3.5 V)	A_{VOL}	60	74	–	db
Unity Gain Crossover Frequency	f_c	–	650	–	kHz
Output Sink Current (0.5 V ≤ V_{O3} ≤ 3.5 V)	I_{O-}	-0.3	-0.6	–	mA
Output Source Current (0.5 V ≤ V_{O3} ≤ 3.5 V)	I_{O+}	2.0	–	–	mA
PWM COMPARATOR SECTION (Pin 3)					
Inhibit Threshold Voltage (Zero Duty Cycle)	V_{THI}	–	4.0	4.5	V
Input Sink Current	I_{I-}	-0.3	-0.6	–	mA
OUTPUT SECTION					
Output Saturation Voltage	$V_{CE(sat)}$				V
Common-Emitter Configuration (V_E = 0 V, I_C = 200 mA)		–	1.1	1.3	
Emitter-Follower Configuration (V_C = 15 V, I_E = 200 mA)		–	1.5	2.5	
Output Collector Leakage Current (V_{CC} = 40 V, V_{CE} = 40 V)	I_{CEO}	–	2.0	200	μA
Output Short-Circuit Current, Each Output (T_A = 25°C)	I_{OS}	–	450	–	mA

OUTPUT CONTROL PIN FUNCTIONAL TABLE

Output Control Pin		Output Control Pin Condition	Output Function
TL494	TL495		
13	14	$0 V \leq V_{OC} \leq 0.4 V$	Single-Ended or Parallel Output
		$2.4 V \leq V_{OC} \leq V_{REF}$	Push-Pull Output

OUTPUT CONTROL PIN

Characteristic	Symbol	TL494C/TL495C			Unit
		Min	Typ	Max	
Low-Level Input Current (V_{OC} = 0.4 V)	I_{OCL}	–	–	-1600	μA
High-Level Input Current (V_{OC} = 2.4 V)	I_{OCH}	–	–	+200	μA

STEERING CONTROL PIN FUNCTIONAL TABLE (Pin 13 on TL495 only)

Pin 13 Condition	Pin 14 Condition	Output Function
Open	$2.4 V \leq V_{OC} \leq V_{REF}$	Normal Push-Pull Operation
$0V \leq V_{ST} \leq 0.4 V$		PWM Output at Q1
$2.4 V \leq V_{ST} \leq V_{REF}$		PWM Output at Q2

STEERING CONTROL PIN (TL495 only)

Characteristic	Symbol	TL495C			Unit
		Min	Typ	Max	
Low-Level Input Current (V_{ST} = 0.4 V)	I_{STL}	–	–	-200	μA
High-Level Input Current (V_{ST} = 2.4 V)	I_{STH}	–	–	+200	μA

ZENER CHARACTERISTICS (TL495 only)

Characteristic	Symbol	TL495C			Unit
		Min	Typ	Max	
Zener Voltage (V_{CC} = 42 V, I_{15} = −2.0 mA)	V_Z	–	39	–	V
Sink Current, Pin 15 (V_{CC} = 15 V, V_{15} = 1.0 V)	I_{RZ}	–	0.3	–	mA

TOTAL DEVICE

Characteristic	Symbol	TL494C/TL495C			Unit
		Min	Typ	Max	
Standby Power Supply Current	I_{CC}	–	6.0	10	mA

OUTPUT AC CHARACTERISTICS

(Use Recommended Operating Conditions except T_A = 25°C unless otherwise noted)

Characteristic	Symbol	TL494C/ TL495C			Unit
		Min	Typ	Max	
Rise Time of Output Voltage	t_r				ns
Common-Emitter Configuration		–	100	200	
Emitter-Follower Configuration		–	100	200	
Fall Time of Output Voltage	t_f				ns
Common-Emitter Configuration		–	25	100	
Emitter-Follower Configuration		–	40	100	

FIGURE 1 – ERROR AMPLIFIER TEST CIRCUIT

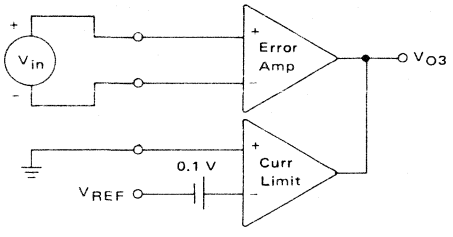


FIGURE 2 – CURRENT LIMIT SENSE AMPLIFIER TEST CIRCUIT

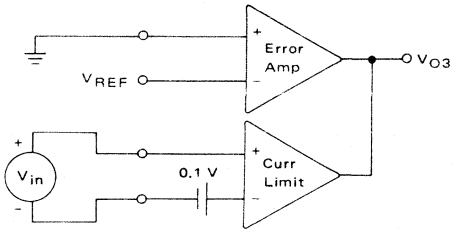


FIGURE 3 – COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

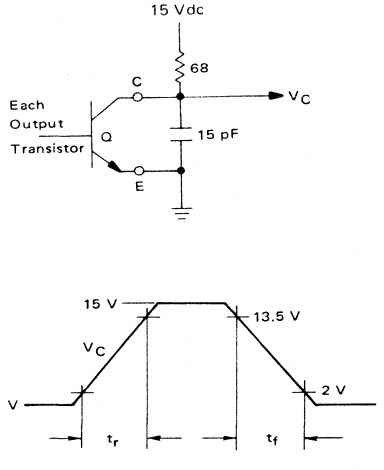


FIGURE 4 – EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

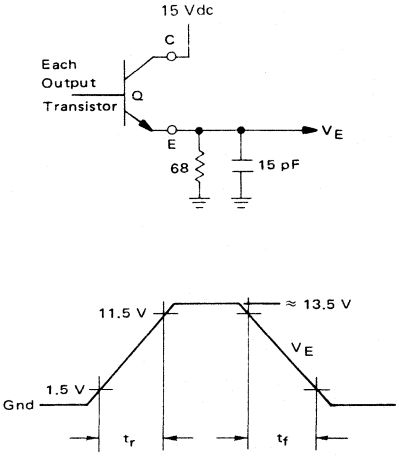


FIGURE 5 – ERROR AMPLIFIER AND CURRENT LIMIT SENSE AMPLIFIER OUTPUT CIRCUITS

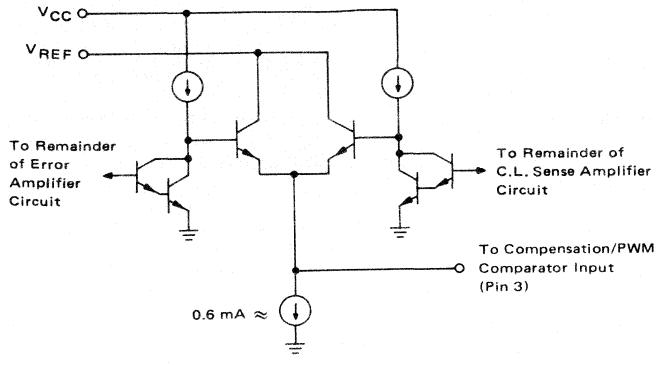


FIGURE 6 – OUTPUT CONNECTIONS FOR SINGLE-ENDED AND PUSH-PULL CONFIGURATIONS

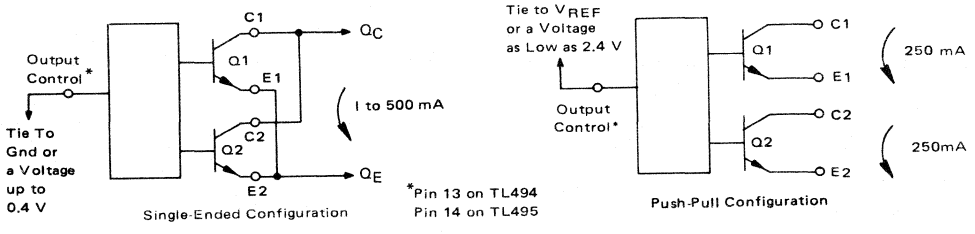


FIGURE 7 – SLAVING TWO OR MORE CONTROL CIRCUITS

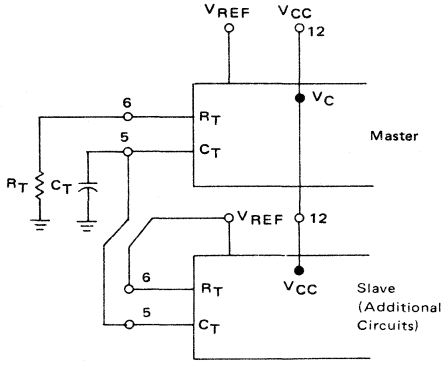


FIGURE 8 – OPERATION WITH $V_{IN} > 40$ V USING INTERNAL ZENER (TL495 ONLY)

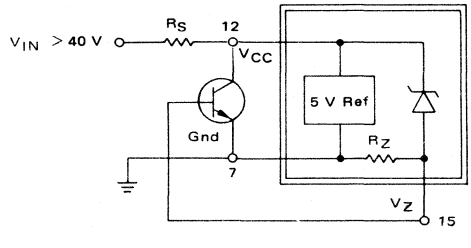
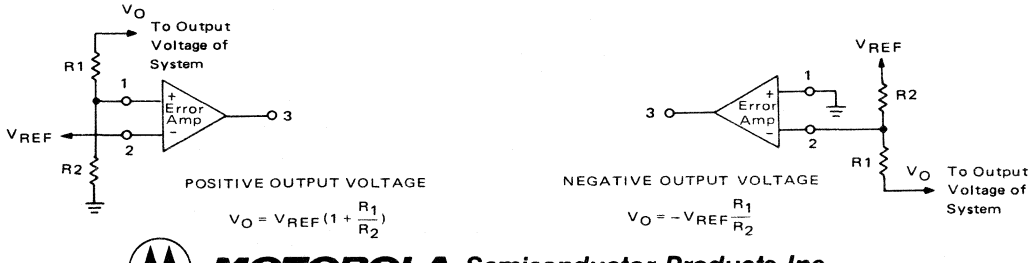


FIGURE 9 – ERROR AMPLIFIER SENSING TECHNIQUES



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geq I_C V_{CC}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

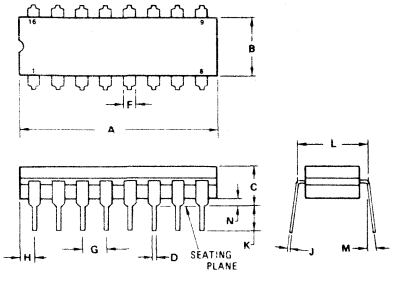
T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

I_C = Total Sink Current

V_{CC} = Supply Voltage

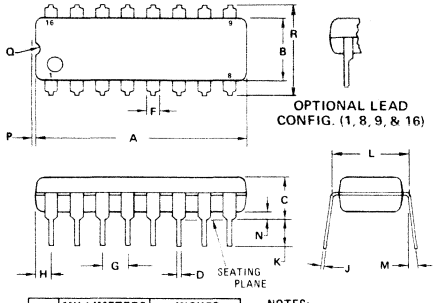
TL494 OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	3.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

J SUFFIX
CERAMIC PACKAGE
CASE 620
$R_{\theta JA}$ = 100°C/W

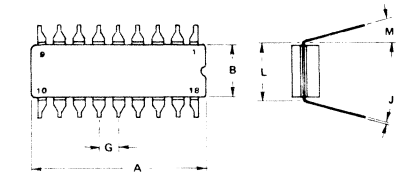


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	22.10	–	0.870
B	6.10	6.60	0.240	0.260
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	–	1.78	–	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	–	0.115	–
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	–	0.020	–
R	–	8.26	–	0.325

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS).

N SUFFIX
PLASTIC PACKAGE
CASE 648
(TL494C ONLY)
$R_{\theta JA}$ = 100°C/W

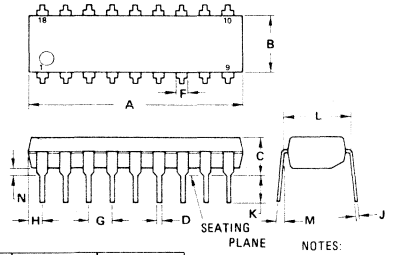
TL495 OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.35	23.11	0.880	0.910
B	6.63	7.24	0.261	0.285
C	–	5.08	–	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.76	1.02	0.030	0.040
J	0.13	0.38	0.005	0.015
K	–	4.44	–	0.175
L	7.37	8.00	0.290	0.315
M	0°	15°	0°	15°
N	0.51	0.76	0.020	0.030

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.

J SUFFIX
CERAMIC PACKAGE
CASE 726
$R_{\theta JA}$ = 100°C/W (Typ)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	23.11	23.88	0.910	0.940
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUM OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G").
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

N SUFFIX
PLASTIC PACKAGE
CASE 701-01
(TL495C ONLY)
$R_{\theta JA}$ = 100°C/W (Typ)

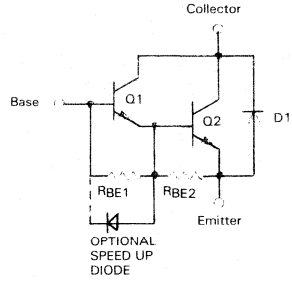
SECTION 6

APPLICATIONS NOTES

ENGINEERING BULLETIN

by: Carl Dockendorf and R. J. Haver

POWER DARLINGTON DESIGN TIPS



WHY DESIGN WITH POWER DARLINGTONS?

Monolithic power Darlington devices have found wide design usage in a variety of different applications. This power technology promises an even brighter future in advancing the state-of-the-art in high-voltage and very high current devices.

Darlingtons offer the designer significant advantages which include:

- High current gain
- Integrated circuit compatibility
- Lower overall cost
- Reduced component count
- Space savings
- Low system driver power requirements
- Internal base-emitter resistors

Since Darlingtons do possess unique advantages they have been designed into many applications which include:

- Class B audio amplifiers and disk-head positioners
- Class D servo amplifiers and tape (head/motor) drivers
- Switching power supplies
- Series pass (linear) regulators
- Hammer drivers
- Series switching regulators
- Motor controls

GAIN

Due to optimum die designs, monolithic Darlingtons almost always give better overall gain than two equivalent discrete transistors. As with discretes, h_{FE} is usually specified at a collector-emitter voltage near but above saturation, and may range from 10 to 200 for high-voltage, high current devices, to 1000 to 20,000 for low-voltage, general purpose devices.

SWITCHING

Storage Time. The output device is not saturated but is close enough that storage time with a base-emitter speedup diode is not much different than discretes. On devices with a speedup diode, storage time can be reduced by approximately 50% by using a Baker clamp with one diode in series with the base. (To get similar results, a discrete would require two series diodes.) Without the diode, the only way to dissipate stored charge is with R_{BE2} and storage time is generally about twice as high as discrete transistors.

Fall Time. Actual resistive fall times when base-emitter diodes are used are comparable or faster than discretes. Without the diode these times can be an order of magnitude higher (2 to 3 μs).* Such devices would not be useful in ultrasonic (20 kHz) Switchmode applications, but are more economical and useful in lower frequency switching applications such as motor controls and hammer drivers.

Turn-On Time. All types of Darlingtons offer a turn-on advantage over discretes because of their high gain. Turn-on losses as measured by dynamic $V_{CE(sat)}$ tests will almost always be lower.

* N.B. When base-emitter avalanche is used, devices without the speed up diode are generally faster with fall times often below 100ns.

USABLE CURRENT RANGE

Like discrete transistors with external base-emitter resistors for thermal stability, at I_B below the $V_{BE(on)}$ threshold, the gain is zero. At high values of IC, gain falls faster than a discrete (approximately $1/IC^2$ instead of $1/IC$). This is a definite advantage when the transistor must switch capacitive or temporaly short-circuit loads because it tends to self-limit its current-to-save values.

To indicate the high current operational limits, Motorola derates $I_{C(max)}$ usually by a factor of two and specifies a gain at this recommended operating current level.

A gain spec at a low current identifies the lower limit. Outside these limits, the device is operational, but will have something less than the specified gain.

PEAK GAIN

This term refers to the point where gain is at its highest value. Turn-on performance is enhanced at all current levels by high peak gain, but turn-off performance is sacrificed. For this reason, manufacturers deliberately design high-voltage Darlington switching transistors for relatively low peak gain to minimize power dissipation during turn-off.

TEMPERATURE RATINGS

Metal power Darlingtons are rated to $T_J = 200°C$ and plastic power Darlingtons are rated to $T_J = 150°C$.

For highest reliability, designers should avoid temperature excursions near the maximum temperature ratings. Under worst-case conditions a derating factor of 20% minimum should be considered.

Motorola generally provides I_{CEO} or I_{CEV} leakage specs at elevated temperatures to guarantee blocking capability at high temperature.

THERMAL STABILITY

At high temperatures, the Darlington turns on in two steps as evidenced by the low-current transconductance curves. First, the driver which has a higher base-emitter resistor turns on, then the output device turns on. It is poor design practice to operate at high temperatures with the driver partially turned on. The rules for discretes of keeping V_{BE} below the turn-on threshold of only one junction apply here as well, since R_{BE2} is low and could allow Q1 to turn on with a voltage of only one V_{BE} drop applied to the base. Very often, external base-emitter resistors or even reverse bias will have to be used to sink the worst-case leakage currents anticipated.

HIGH FREQUENCY

The high frequency gain performance of a Darlington does not fall off at 6 dB/octave like a discrete and so f_T has been replaced by h_{fe} as a figure of merit. This gain is typically measured at 1.0 MHz where gain is decreasing by approximately 12 dB/octave.

1. Al Pshaenich, "Driving Inductive Loads," *Electronic Design*, Feb. 15, 1977, pp. 86-91.

ADDITIONAL COMPONENTS

Output Collector-Emitter Diode. All Motorola power Darlingtons provide a diode connected between the output collector and its emitter. This diode has blocking voltage capability comparable to the device V_{CB} rating, forward switching, and forward recovery times which compare very favorably with typical load clamp diodes and forward current capability equal to or greater than the device maximum current rating. While ignored by many designers, this diode can be quite useful as a surge suppressor for inductive loads in such multiple transistor drive configurations as complementary push-pull, totem-pole, half-bridge, and full-bridge circuits.[1]

The diode does have a higher forward drop than standard rectifers and has slow reverse recovery. Therefore, if long intervals of high reverse current are expected (such as motor controls), a parallel fast recovery diode is recommended.

Base-Emitter Turn-Off Diode. The base-emitter turnoff diode is used primarily on high-voltage Switchmode Darlingtons to access the output transistor's base. It is connected across the base-emitter junction of the driver (QI) and is generally a hybrid diode mounted on the same header with bond wires connecting it to the Darlington. It has proven quite successful in enhancing turn-off time and is provided on most high-voltage switching Darlingtons. (See schematic on page 1.)

Base-Emitter Resistors. Most devices have two base-emitter resistors for thermal stability. These resistors at one time were made during the base diffusion and doubled with a 100°C temperature rise. New low-voltage parts now use emitter resistors which are much less sensitive to temperature (<10% change) and new high-voltage parts use low resistivity base material at the surface of the die.

THE dv/dt EFFECT

The dv/dt effect present a potential efficiency problem whenever two switching Darlingtons are connected in a totem-pole configuration between a supply line and ground. When one device turns on, it creates a fast-rising voltage pulse across the other and causes displacement currents to flow through the C_{ob} capacitance. Because these devices have high gain, a significant pulse of collector current may flow during this turn-on time interval and cause excessive heating and loss of efficiency. This effect is most noticeable when only resistors are used to terminate the base-emitter junction. It can be minimized or eliminated by using reverse bias on the base or by using soaking inductors in series with the collector to absorb the dv/dt and limit current.

BREAKDOWN VOLTAGES

Because Darlingtons have monolithic base-emitter resistors, a $V_{CEO(sus)}$ test is actually measuring $V_{CER(sus)}$ which may be 20 to 50 V higher than that of this same device without R_{BE}. However, the $V_{CEO(sus)}$ rating is still very useful and is backed up by forward bias SOA curves and reverse bias SOA curves (where appropriate) to indicate the pulsed or switching current capability of these parts near this rated voltage.

To verify $V_{CEO(sus)}$, the classic inductive sweep test can sometimes be used with low-voltage (<300 V) parts. However, high-voltage parts, both discretes and Darlingtons, may be degraded or shorted by such a test. Even the 300 μs curve tracer test is not considered fail-safe because the relatively high voltage at even 50 to 100 mA can cause instantaneous second breakdown. For this reason, clamped inductive tests are recommended to verify all sustaining voltage ratings. (See Motorola Engineering Note 101.)

THERMAL RESISTANCE, $R_{\theta JC}$

Measuring $R_{\theta JC}$ on a Darlington is not straightforward, since the fourth terminal (the output base) is typically not accessible and standard measurement techniques do not apply, since a Darlington has two emitter-base junctions in series. Motorola performs this test by specially bonding the testing Darlingtons with only the output transistor connected. This provides conservative ratings in that the published $R_{\theta JV}$ and power dissipation of the Darlington reflect only that of the output device.

The NBS (National Bureau of Standards) has reported an alternate technique with comparable results in "Darlington Thermal Resistance Measurements," a paper by Mr. S. Rubin published in the PESC (Power Electronic Specialist Conference) record of 1975.

SATURATION VOLTAGES

The Darlington collector-emitter saturation voltage will always be slightly higher than a discrete. This voltage can be shown to be a sum of the base-emitter drop of Q2 and the collector-emitter saturation voltage drop of the driver Q1. This higher saturation volgate does decrease collector efficiency, but is normally offset by improved efficiencies and simpler driver circuits in the base.

COMPARISON CHART

The comparison chart shows the significant difference between discretes and equivalent Darlington transistors. The three types of parts shown include low-voltage plastic (<300 V), low-voltage metal, and high-voltage metal. Gain is the most obvious difference and saturation voltages are about 1.0 V higher. The gain will generally be several thousand for low-voltage devices, but only a couple of hundred for high-voltage parts. Switching times for some of the high-voltage parts are comparable with discretes because a base emitter diode is used. Darlingtons without this diode are slower, as noted earlier they may be improved with base-emitter avalanche.

DARLINGTON versus DISCRETE COMPARISON

Devices		Plastic (Low Voltage)		Metal (Low Voltage)		Metal (High Voltage)	
		Discrete MJE3055	Darlington MJE6045	Discrete 2N5886	Darlington MJ11014	Discrete 2N6547	Darlington MJ10005
	$I_{C(max)}$	10 A	8 A	25 A	30 A	15 A	20 A
	$V_{CEO(sus)}$	60 V	100 V	80 V	90 V	400 V	400 V
	$T_{J(max)}$	150°C	150°C	200°C	200°C	200°C	200°C
	Die Size (mils)	100 x 130	108[2]	200[2]	200[2]	230[2]	200[2]
	At I_C of	4 A	4 A	10 A	10 A	10 A	10 A
Typ	h_{FE}	35	3000	40	8000	10	100
Typ	$V_{CE(sat)}/I_B$	0.4/10	1.4/ 1 K	0.4/20	1.0/1 K	0.4/4	1.4/40
Typ	t_s Resistive	600 ns	1,5 μs	700 ns	3.5 μs	2.0 μs	600 ns
Typ	t_f Resistive	400 ns	2.5 μs	250 ns	2.5μs	200 ns	150 ns

Note: High Voltage Metal is NPN only. Others have PNP complements available. The MJ 10005 has a base-emitter speedup diode, others do not.

INDUSTRIAL CONTROLS

Engineering Bulletin

By: Henry Wurzburg,
Industrial Applications Engineer

Control Your Switching Regulator with the MC3380 Astable Multivibrator

An emitter-coupled astable multivibrator with programmable pulse width and current-controlled pulse-repetition-rate capabilities can be used not only as a free-running oscillator, but as the control element in switching regulator applications. This bulletin describes the operation and characteristics of the MC3380 astable multivibrator and details the design of a 200-volt switching regulator circuit for gas discharge displays, which uses this device as the control element.

Device Operation

Figure 1 is a schematic of the MC3380 in an oscillator circuit. Q1 and Q2 form an astable multivibrator whose pulse width and repetition rate are determined by R_{EXT}, C_{EXT} and the magnitude of I_4, which is proportional to the current into pin 6, I_{FB}. To understand the operation of the circuit, begin by assuming that a voltage exists on C_{EXT} sufficient to turn Q1 off. Under this condition,

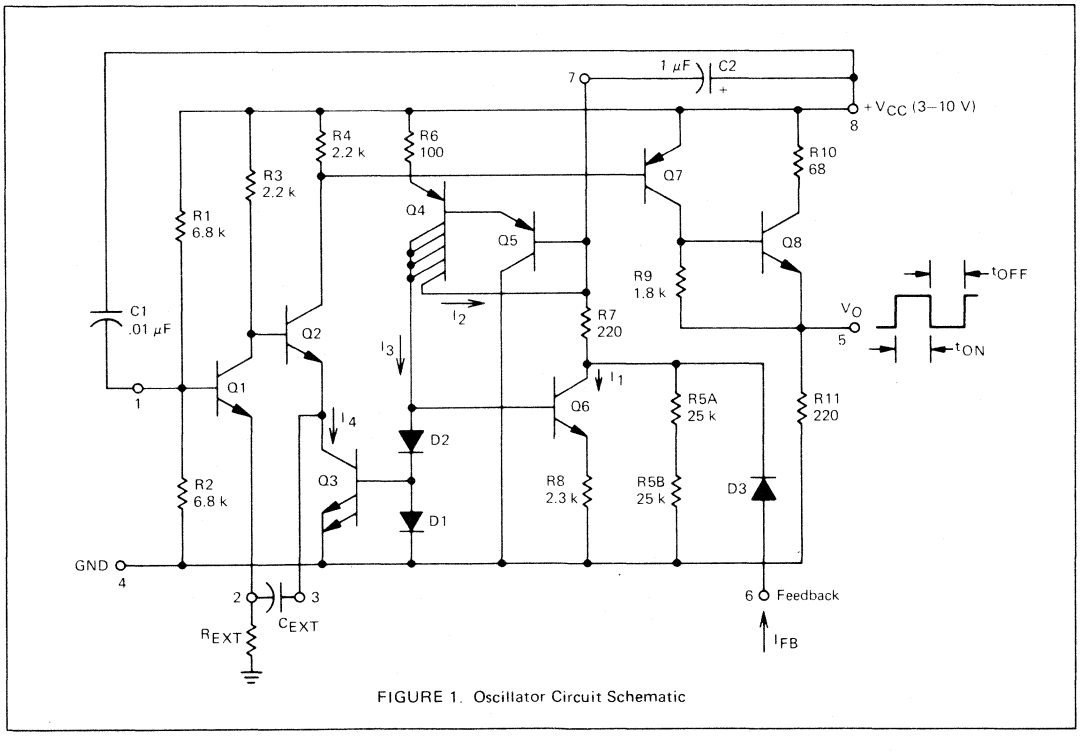


FIGURE 1. Oscillator Circuit Schematic

Q2 is on and the oscillator output, V_O, is high. The charge in C_{EXT} flows to ground at a rate determined by R_{EXT} until the voltage across C_{EXT} is low enough to allow Q1 to turn on. This period is t_{ON}. When Q1 turns on, Q2 turns off, the output goes low, and C_{EXT} is now charged at a rate determined by C_{EXT} and I_4 until the voltage across C_{EXT} is sufficient to turn off Q1 again. This period is t_{OFF}.

Transistor Q6, in conjunction with D1, D2 and R8, forms a constant current source whose output is I_1 (nominally 400 μA). The value of I_2 is approximately $I_1 - I_{FB}$. Q4 sources a current, I_3, whose value is $4I_2$, or 4 ($I_1 - I_{FB}$). Since the emitter area of Q3 is twice that of D1, the combination of Q3, D1, and D2 forms a current mirror which sinks a current, I_4, equal to $2I_3$ or 8 ($I_1 - I_{FB}$). By increasing I_{FB}, the magnitude of I_4 is decreased, the charging time of C_{EXT} is increased and t_{OFF} becomes longer. As I_{FB} approaches I_1, I_4 approaches zero and oscillation ceases. The value of I_{FB} at which this occurs is specified to be between 250 μA and 600 μA.

Two additional external capacitors are required for proper operation of the oscillator circuit. C1 assures initial startup, while C2 serves as a noise filter for the current summing node of Q6.

Device Characteristics

The output characteristics of MC3380 are shown in Figure 2 and in Figure 3, a plot of t_{OFF} versus C_{EXT} shows the minimum t_{OFF} that can be obtained with a given value of C_{EXT} which occurs when I_{FB} is equal to zero. A plot of t_{OFF} versus I_{FB} is not shown since this characteristic varies widely between individual devices and is not normally necessary for proper circuit design if the MC3380 is used in a closed-loop control system. The following design example will show that knowledge of t_{OFF} versus C_{EXT} is necessary only for an I_{FB} equal to zero. A graph of t_{ON} versus R_{EXT} and C_{EXT} is shown in Figure 4. Note that t_{ON} is not dependent upon the value of I_{FB}, but only on the value of R_{EXT} and C_{EXT}.

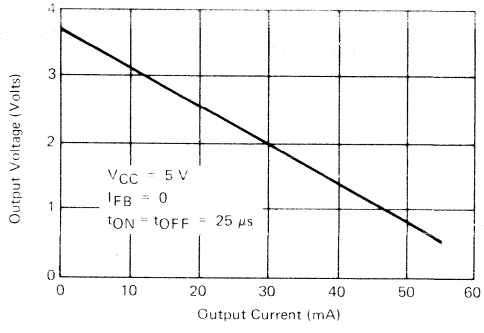


FIGURE 2. Typical MC3380 Output Characteristics

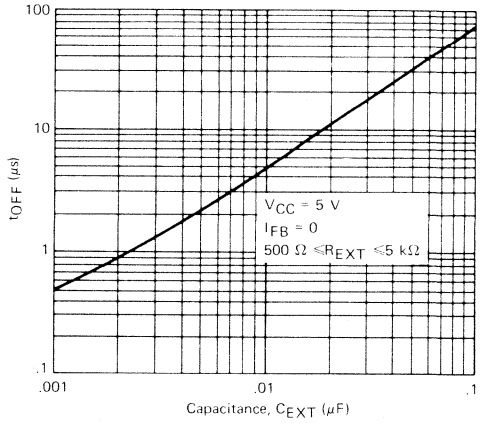


FIGURE 3. Typical C_{EXT} versus t_{OFF}

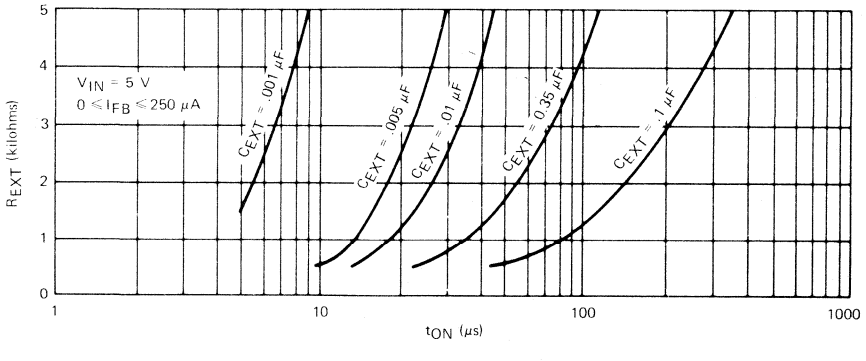


FIGURE 4. Typical t_{ON} versus R_{EXT}

Circuit operation is as follows: during t_{ON}, Q1 and Q2 are saturated and the primary current of T1 increases, fast recovery diode, D1, preventing secondary current flow during this period. Q1 and Q2 are then switched off, and the energy stored in the primary of T1 ($1/2LI^2$) is transferred to the secondary during t_{OFF}. Feedback to the MC3380 is accomplished by a zener diode, Z1. If the output voltage tends to increase, the zener current, I_{FB}, increases and lengthens t_{OFF}. The rate of energy transfer is decreased, and the output voltage tends to decrease.

The general design procedure for the circuit of Figure 8 is as follows:

1. Design specifications

Input Voltage, V_{IN}	5 V
Output Voltage, V_{OUT}	200 V ±10%
Output Current, I_O	15 mA
Conversion Efficiency, η	≥70%
Full Load Operating Frequency, f	≥20 kHz

2. Determine input power, P_{IN}

$$P_{IN} = \frac{P_{OUT}}{\eta} = \frac{V_O I_O}{\eta} = \frac{2 \times 10^2 (15 \times 10^{-3})}{0.7} W = 4.3 \text{ W}$$

3. Arbitrarily choose t_{ON} = 30 μs, t_{OFF} = 10 μs, for a full-load frequency of 25 kHz.

4. Determine R_{EXT} and C_{EXT}.
   a. Choose C_{EXT} such that $t_{OFF} \leq 10$ μs when I_{FB} = 0. This guarantees that $I_{FB} \geq 0$ at full load, assuring proper regulation. From Figure 3, $C_{EXT} \leq 0.02$ μF; 0.01 μF is a convenient value.
   b. R_{EXT} is found from Figure 4. If C_{EXT} = 0.01 μF, then R_{EXT} = 2.5 kΩ for t_{ON} = 30 μs. 2.7 kΩ is the nearest standard value, giving t_{ON} = 31 μs.

5. Determine I_{PK} through T1 primary

$$P_{IN} = \frac{V_{IN} I_{PK} (t_{ON})}{2 (t_{ON} + t_{OFF})}$$

$$I_{PK} = \frac{2 P_{IN} (t_{ON} + t_{OFF})}{V_{IN} t_{ON}}$$

$$= \frac{2 (4.3) 41 \times 10^{-6}}{5 (31 \times 10^{-6})} \text{ A} = 2.3 \text{ A} .$$

Note that a 500-μF capacitor is used to decouple the power supply from the 2.3A peak current.

6. Determine primary inductance, neglecting the transistor saturation voltage.

$$L_P = \frac{V_{IN} t_{ON}}{I_{PK}} = \frac{5 (31 \times 10^{-6})}{2.3} \text{ H} = 65 \text{ μH} .$$

7. Using manufacturers' design equations, determine inductor specifications. A Ferroxcube pot core (No. 2213-L00387) with the following primary winding specification was used:

   Np = 8 turns of No. 22 AWG magnet wire

   Gap = 0.006 inch.

8. Determine maximum number of secondary turns allowable for complete decay of secondary current during the minimum t_{OFF} at rated output.

$$L_{S\,(MAX)} = \frac{V_{OUT} t_{OFF}}{I_{S\,(PK)}} \text{ where}$$

$$I_{S\,(PK)} = \frac{2 I_O (t_{OFF} + t_{ON})}{t_{OFF}}$$

$$I_{S\,(PK)} = \frac{2 (15 \times 10^{-3}) 41 \times 10^{-6}}{10 \times 10^{-6}} \text{ A} = 123 \text{ mA}$$

therefore

$$L_{S\,(MAX)} = \frac{200 (10 \times 10^{-6})}{123 \times 10^{-3}} \text{ H} = 16.26 \text{ mH}$$

$$N_{S\,(MAX)} = \frac{N_P}{\sqrt{\frac{L_P}{L_{S\,(MAX)}}}}$$

$$= \frac{8}{\sqrt{\frac{65 \times 10^{-6}}{16.26 \times 10^{-3}}}} = 125 \text{ turns} .$$

9. Determine turns ratio of T1.
   From the standpoint of secondary current decay, the number of secondary turns could be from 1 to 125. However, winding space limits the number of turns, while the breakdown rating necessary for Q2 increases as the turns ratio decreases. Also, the peak diode current increases with decreasing secondary turns. A good compromise between space limitations and Q2 breakdown rating is 80 turns. The necessary BV_{CER} is:

$$BV_{CER} \geq V_R + V_{IN} \text{ where } V_R = V_{OUT} \frac{N_P}{N_S}$$

$$= \frac{2 \times 10^2 \times 8}{80} \text{ V} = 20 \text{ V} .$$

Therefore, a minimum BV_{CER} of 25 V is required.

10. Power Switch.
Q2 must have the following characteristics: Low $V_{CE\ (SAT)}$ at I_C = 2.3 A and $\frac{I_C}{I_B}$ = 10, high switching speed and a $BV_{CER} \geq 25$ V. Q1 was chosen on a similar basis. R2 was chosen to be as low as possible to aid turn-off of Q2. R1 and C1 form a snubber network to damp any high voltage spikes generated by the leakage inductance of T1 and were chosen empirically.

11. Feedback.
The type of feedback scheme depends upon the polarity of the input and output voltages with respect to system ground. A positive 200-volt output is desired, and a negative input voltage is available. Therefore, the system ground reference must be pin 8 and a zener diode can be used as a feedback element. The output voltage is given by:

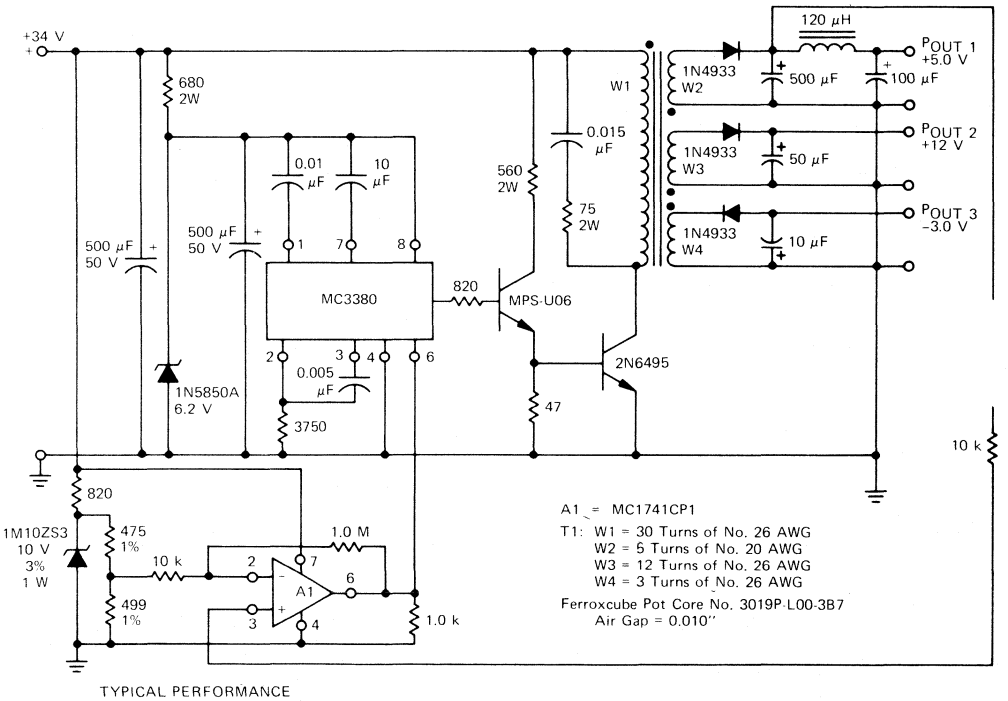
$V_{OUT} \approx V_Z$ = 200 ±10% volts (for a 10% tolerance zener).

Multiple Output Regulator

Multiple output voltages can be obtained by using additional secondary windings. Figure 9 illustrates the use of this technique. The regulation provided by these additional outputs depends upon the degree of their coupling to the regulated 5-volt winding.

The system ground reference for this circuit is pin 4. Feedback is accomplished by amplifying the output error with op amp A1, and applying this voltage to pin 6 of the MC3380. Referring back to Figure 1, it can be seen that if the voltage at pin 6 increases to within one-diode drop of the voltage at pin 8, Q4 and Q5 will begin to turn off, decreasing I_4 and increasing t_{OFF}.

Design of the transformer, T1, and the power circuit consisting of Q1 and Q2 was accomplished using the same methods discussed in the previous section.



TYPICAL PERFORMANCE

$P_{OUT\ 1}$ = 4 Watts (V_O = 5 V ±5%)
5-V Ripple Component = 50 mV (120 Hz + 20 kHz)

$P_{OUT\ 2}$ = 600 mW (V_O = 12 V ±10%)
$P_{OUT\ 3}$ = 3 mW (V_O = 3 V ±10%)

Load Regulation, $P_{OUT\ 1}$ = 0.6% ($0 \leq I_L \leq 800$ mA)

FIGURE 9. Typical Application as Multiple Output Switching Regulator

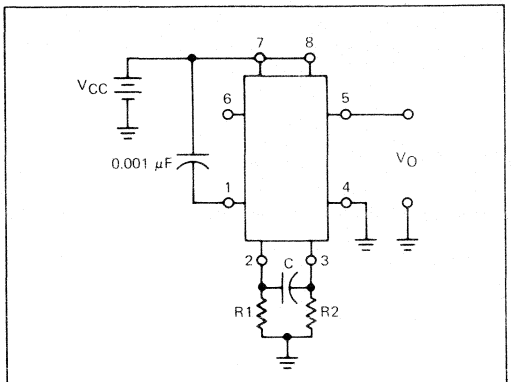


FIGURE 5. Astable Multivibrator Circuit

Free-Running Oscillator

If a fixed-frequency, free-running oscillator is required, the circuit of Figure 5 can be used. In this circuit, the current sink, Q3, has been disabled by connecting pin 7 to pin 8. Q4 and Q5 are therefore off and $I_4 = 0$. R2 provides a charging path for C during t_{OFF}. The frequency range of this oscillator is from approximately 1 kHz to greater than 300 kHz. Plots of frequency and duty cycle versus R1, R2 and C are shown in Figures 6 and 7.

A 200-V Switching Regulator for Gas Discharge Displays

The use of gaseous discharge displays in electronic equipment is becoming increasingly common. A convenient method of converting a low-voltage supply to high voltage to power this type of display is shown in Figure 8. In this circuit, the MC3380 is used as the control element in a switching regulator. The regulator converts 5 V into 200 V and provides up to 15 mA of output current, sufficient to drive 10 to 15 digits of most gas discharge displays.

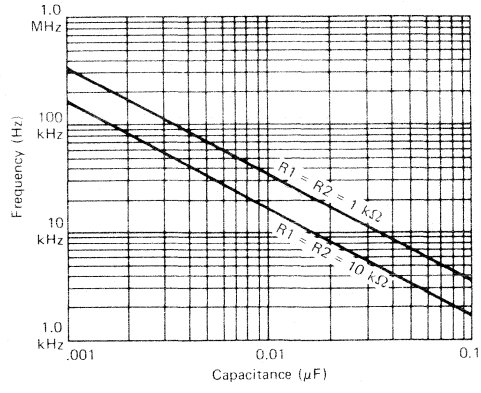


FIGURE 6. Typical Capacitance versus Frequency

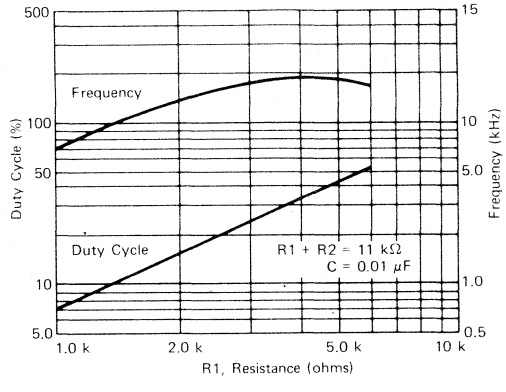


FIGURE 7. Typical Duty Cycle and Frequency Characteristics

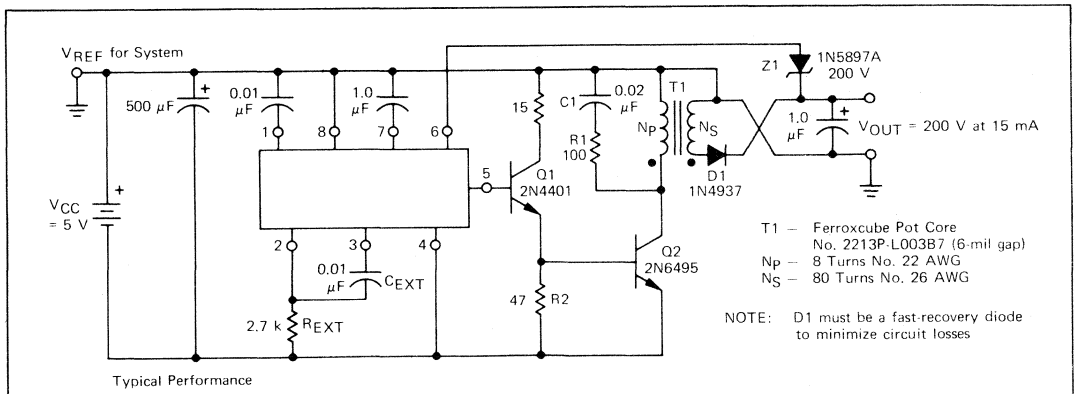


FIGURE 8. 200-V Switching Regulator Circuit

Engineering Bulletin

Prepared by
R. Suva and R. J. Haver

NEW ICs PERFORM CONTROL AND ANCILLARY FUNCTIONS IN HIGH PERFORMANCE SWITCHING SUPPLIES

A newly introduced IC, the MC3420, performs a great number of functions required for the control of inverter type Switchmode power supplies. It contains the obvious functions of oscillator, pulse-width modulation and pulse routing to two internal medium power buffers, as well as unique features like independent dead-time selection, remote shutdown and symmetry correction between the outputs.

Instead of including all functions into a single IC, the more flexible multi-circuit approach was preferred which guarantees a more effective cost-performance ratio in a great number of simple systems and gives better performances in sophisticated designs. Following this approach Motorola has also developed a separate IC for the overvoltage protection of power supplies. This circuit, the MC3423, allows the detection of an overvoltage across two lines from which it also takes its supply. It delivers at its output a suitable signal to effectively fire a crowbar SCR. This technique achieves the best and fastest protection of the load. A unique feature of the MC3423 allows its triggering action to be delayed so that short overvoltages are not taken into account. The present note shows as an example a complete 5 V/50 A, 20 kHz off-line supply designed around an MC3420 and MC3423. It features a regulated output voltage, a limited output current, soft start, inrush current limitation and over and under voltage output protection.

A brief description of the system and of its different sections and their performance follows.

The design uses the preferred inverter configuration for European mains voltages and medium output power, i.e., the half-bridge which does require only moderately high V_{CEX} power devices.

Figure 1 is the basic block diagram of the supply that shows the different sections and their interconnections. Greater details are given in Figure 3 to which reference will be made in the following.

Input Rectifier and Filter

The 220 Vac line voltage is rectified by an MDA970-5 bridge (see input section Figure 3) and filtered by a 600 μF capacitor which also provides energy storage for maintaining the output during a missing mains cycle. Bridge inrush current limitation at switch-on is performed by R1 while triac Q1 is off. After about 100 ms timer C6, R6 (see control section) enables the output pulses of the MC3420 control circuit which, through Q7 and transformer T2, continuously fire Q1 thus bypassing R1 and limiting power waste.

Power Inverter

The inverter consists of capacitors C1 and C2, transistor TR1, TR2 and transformer T1. By the alternate switching ON and OFF of TR1 and TR2 a stepped waveform of approximately 155 V is applied to transformer T1 which provides isolation between mains and output as well as stepping down to the desired output voltage. Regulation of the output is obtained by varying the duty ratio of this stepped waveform. Overlapping of the conduction phases of the power transistors is avoided by a correct setting of R3 at the MC3420 control circuit and by maintaining high transistor switching speed by use of the anti-saturation diodes D4 to D9.

The 20 kHz low amplitude output of T1 is efficiently rectified by Schottky rectifiers D1 and D2 (see rectifier and filter section) and filtered by two LC filter sections. The output current is measured across shunt RSC and limited to 50 A by the control electronic. A crowbar thyristor, fired by the overvoltage detector circuit, is actuated in the event of an abnormally high or low output voltage.

Control Section

The control is centered around the MC3420 IC whose internal oscillator is set at 40 kHz, twice the working frequency, by means of R2 and of the capacitor on pin 2. The triangular wave generated by the oscillator, available on pin 8, is compared by the internal comparator to the external control voltage applied on pin 6, the result is a PWM wave where pulses appear alternately at output 11 and 13. As previously stated R3 sets the minimum dead time to insure non-overlapping between the output power devices. At pin 9 the MC3420 delivers a stable reference voltage that can be used externally. The control voltage

at pin 6 is given by the error amplifiers U1A, U1B for current and voltage, respectively, or by the soft-start timing capacitor C6, the three outputs are diode-ORed so that the one requiring the lowest supply output is active.

Base Drivers

Base drive of TR1 and TR2 is provided by Q5 and Q6 through transformers T3, T4 that transmit pulses of both polarities for the efficient drive and recovery of the power devices.

Voltage Sensors

The additional function of overvoltage sensing is given by the MC3423 IC. This circuit compares the voltage at pin 2, here the scaled down supply output voltage, with an internal reference. The result of the comparison, if active, is delayed 0.1 ms by the capacitor on pin 3, 4 and if lasting, triggers the crowbar SCR and inhibits the MC3420 at pin 15. The trip-point is set here at around 5.5 V.

The use of a single quad amplifier for the error amplifiers leaves a third amplifier U1C with which a low voltage sensor can be implemented for detecting output voltages of 4.5 V or lower. U1C actuates the remote activation input of the MC3423. Here, too, a delayed action is obtained by use of an RC network.

Low-voltage sensing may be desirable to detect an overload or an excessively low input mains that would, for example, not guarantee the reliable switch-off of the power devices and thus possibly cause catastrophic failures.

Reset

Starting of the supply and resetting it after a crowbarring is obtained by the reset button R which, when depressed, disables the over and under voltage sensors.

Ancillary Indicator Functions

The addition of a D-flip-flop (Figure 2 of LED + drivers and use of the fourth linear amplifier U1D allows the permanent indication of the tripping cause, a very useful information especially in the development stage of a new electronic system. Minor additions of the devices indicated by an asterisk in Figure 2 are also necessary to grant proper performance of this circuit. Clocking of the D-flip-flop is provided by transistor Q2 and data inputs to it by comparators U1C and U1D.

Supply Performances

The performances of the present power supply are as follows:

Line Regulation	0.4%
Load Regulation	0.25%
Output Ripple	60 mVp-p
Efficiency	75%

FIGURE 1 – Power Supply Basic Block Diagram

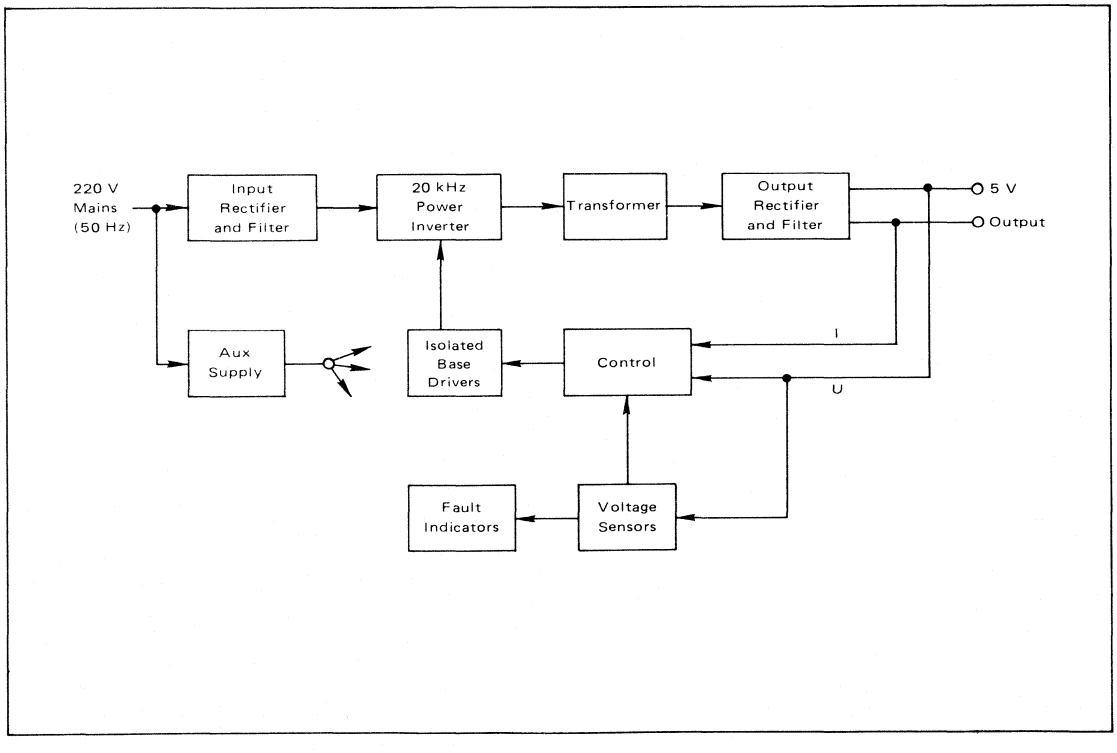
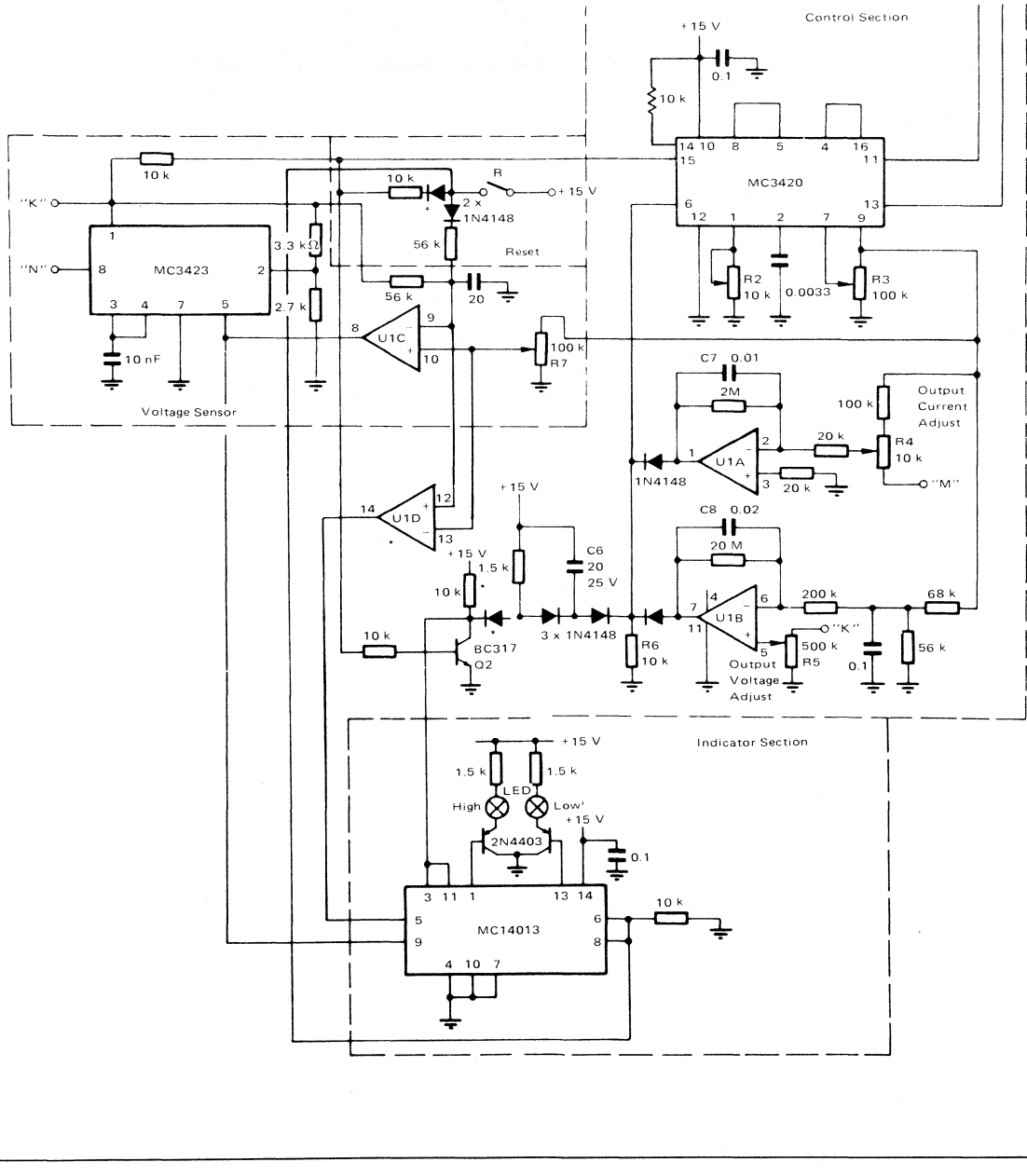
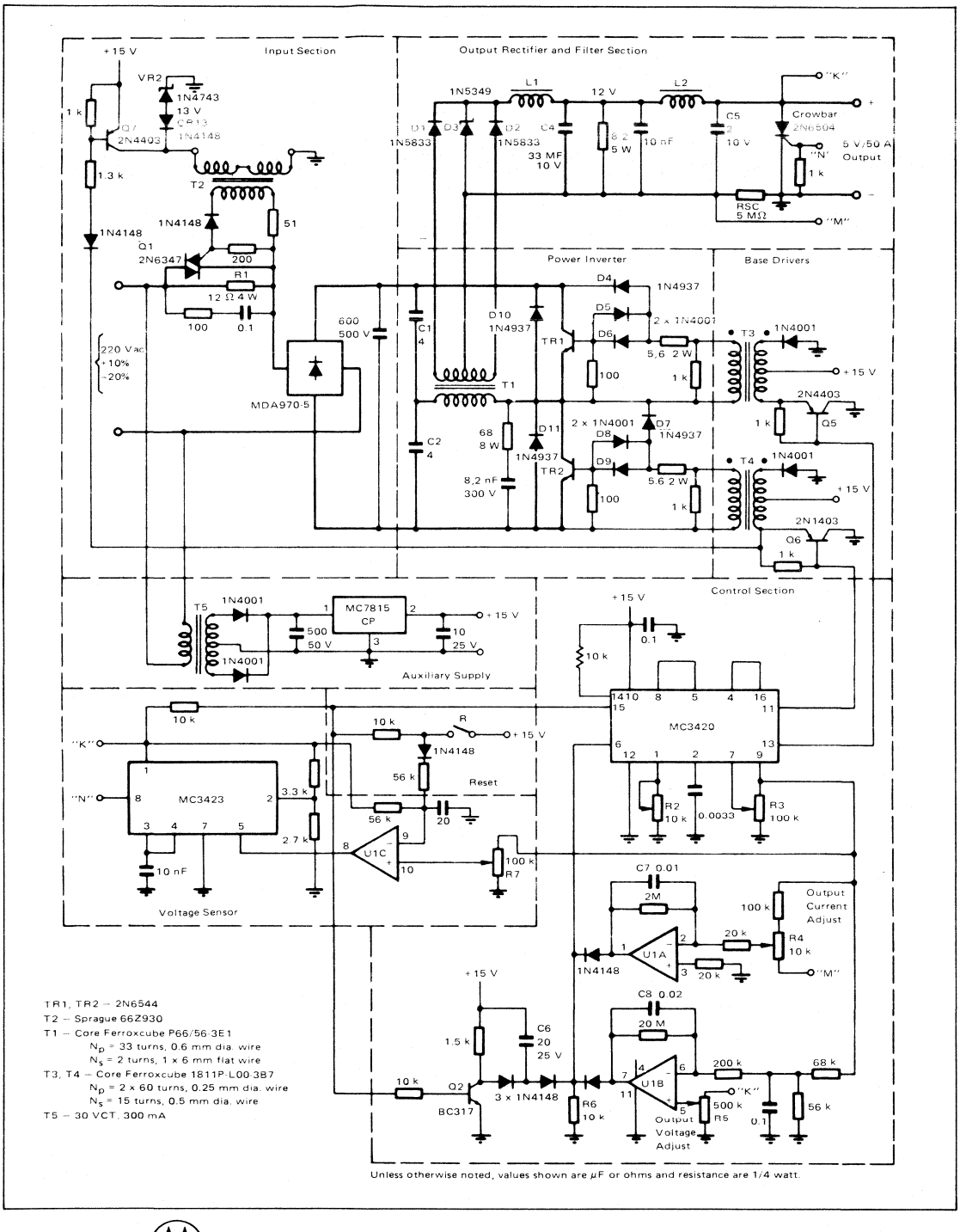


FIGURE 2 – Ancillary Indicator Functions



Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

FIGURE 3 – Complete Schematic of Half-Bridge 5 V/50 A Switching Supply



TR1, TR2 – 2N6544
T2 – Sprague 66Z930
T1 – Core Ferroxcube P66/56-3E1
N_p = 33 turns, 0.6 mm dia. wire
N_s = 2 turns, 1 x 6 mm flat wire
T3, T4 – Core Ferroxcube 1811P-L00-3B7
N_p = 2 x 60 turns, 0.25 mm dia. wire
N_s = 15 turns, 0.5 mm dia. wire
T5 – 30 VCT, 300 mA

Unless otherwise noted, values shown are μF or ohms and resistance are 1/4 watt.

AN-314

THERMAL STABILITY CONSIDERATIONS FOR HIGH CURRENT SCHOTTKY BARRIER RECTIFIERS

The power dissipation of schottky barrier diodes in different single phase full wave rectifier circuits is calculated and the thermal stability of the corresponding circuits is discussed.

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INTRODUCTION

The schottky barrier diode, also called surface barrier and hot carrier diode, consists of a rectifying metal-semiconductor junction. Due to this structure these diodes exhibit a very low forward voltage drop and, because the forward current is due to majority carrier flow, the diodes have practically no storage time, thus allowing a highly efficient rectification up to quite high frequencies.

However, this feature has to be paid for and the price is relatively high reverse current.

The reverse current follows an exponential temperature characteristic of the form

$$I_R = RT^2 e^{-q\Phi(V_R) / kT}$$

The potential barrier height $\Phi(V_R)$ is a function of the reverse voltage V_R and decreases with increasing V_R. Consequently the reverse current of hot carrier diodes is considerably more dependent on the voltage than normal silicon p-n junction diodes.

This dependence of the reverse current on temperature and voltage can cause thermal runaway of the devices.

The purpose of this note is to discuss some commonly used single phase rectifier circuits and to analyse their thermal stability.

The results of this analysis can be used to calculate heatsink specifications and safe operating temperature ranges.

THE ELECTRICAL CHARACTERISTICS OF HOT CARRIER DIODES

The discussion is based on the typical values given in the data sheet for the 1N5834. Figures 1 and 2 represent the forward and the reverse current-voltage characteristics of this device.

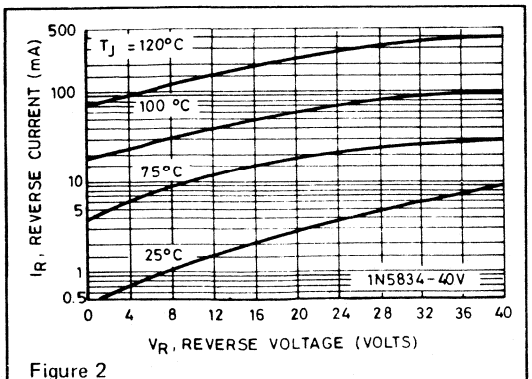


Figure 2
Reverse characteristics

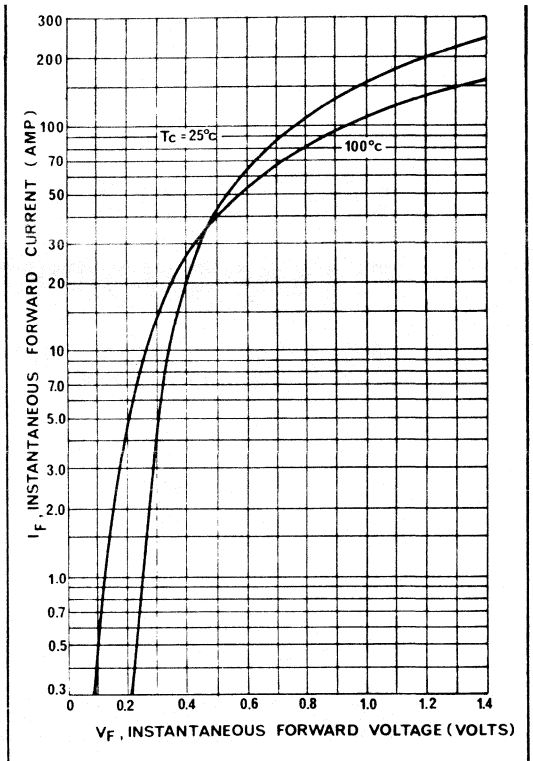


Figure 1
Forward characteristics

For the further calculations made here, it is more convenient to use a linear plot of the forward current-voltage characteristic, because this permits a very practical piece-wise linear approximation. Such a representation is shown in Figure 3.

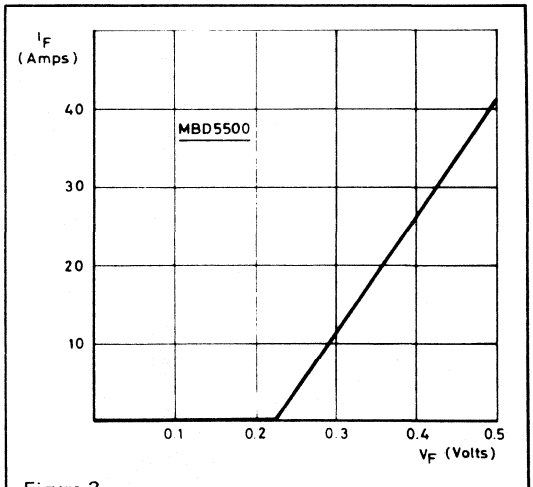


Figure 3.
Piece-wise linear approximation of the forward characteristics
$V_F = 6.5 \cdot 10^{-3} \cdot I_F + 0.23$

THERMAL STABILITY

Before discussing the conditions for thermally stable operation of hot carrier diodes, it is useful to recall briefly the conditions for thermal stability in a general way:

The junction temperature of a dissipating semiconductor device can be described by the equation:

$$T_j = P_o \cdot R_{th} + P(T_j) \cdot R_{th} + T_a \qquad (1)$$

T_j = junction temperature
T_a = ambient temperature
P_o = temperature independent power dissipation
$P(T_j)$ = temperature dependent power dissipation
R_{th} = total thermal resistance from the junction to the ambient meduim

Equation (1) is found by considering the energy balance

$$\frac{T_j - T_a}{R_{th}} = P_o + P(T_j) \qquad (2)$$

at thermal equilibrium. The term on the left of (2) represents the power flow to the ambient medium (P_{out}) whereas the right hand term represents the power produced within the device (P_{in}).

The condition for thermal stability is

$$\frac{dP_{out}}{dT} \geqq \frac{dP_{in}}{dT} \qquad (3)$$

Figure 4 shows the variations of both the terms of equation (2) as a function of T_j. The intersection points A and B satisfy equation (2) but only point A represents a thermally stable state, because equation (3) is only satisfied for point A but not for point B.

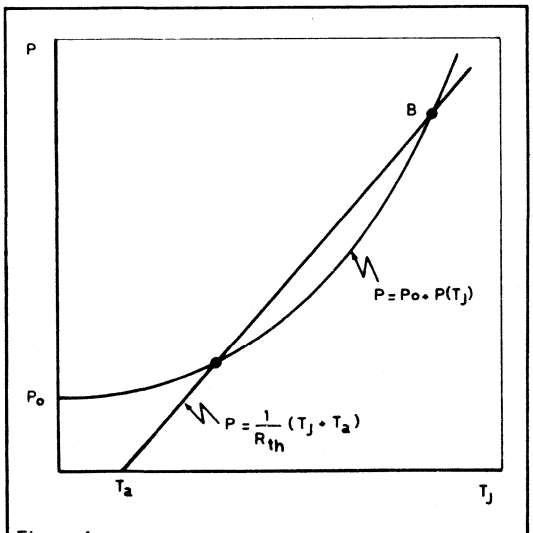


Figure 4
Graphical representation of equation (2)

THE POWER DISSIPATION OF HOT CARRIER DIODES IN RECTIFIER CIRCUITS

Compared to conventional rectifiers the hot carrier diodes present a much closer approach to an ideal rectifier, owing to the smaller losses of the latter.

Power is dissipated during the conduction period of the rectifier due to the forward voltage drop and the load current. Because the forward voltage drop of schottky barrier diodes is only slightly dependent on temperature, the forward power dissipation may be considered as independent of the temperature.

During the period of reverse bias, power is dissipated due to the leakage current. The leakage current is strongly temperature dependent and has therefore to be considered in the analysis of thermal stability.

The operating conditions of rectifiers are essentially defined by the load conditions. The most frequently encountered load conditions are the following:
- Resistive load
- Inductive filter input load
- Capacitive filter input load

In the following three sections the power dissipated in the rectifiers used under the above mentioned load conditions will be calculated.

The input voltage is assumed to be a sinusoidal wave of angular frequency ω. Also, only single phase full wave rectifier circuits with a center tap transformer will be considered. The results may easily be applied to the bridge rectifier circuits by modifying only a few details, without changing the general results.

In the appendices A and B the electrical characteristics of rectifier circuits with inductive and capacitive loads are analysed. These results are used in the following three sections to calculate the power dissipation in the rectifiers. In addition, though, the results given in appendices A and B are of general interest, because they contain useful information for the design of rectifier circuits.

Resistive Load

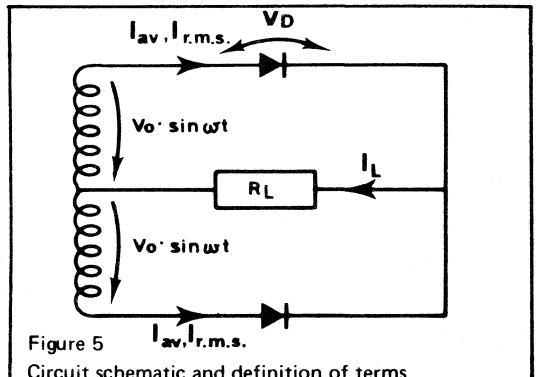


Figure 5
Circuit schematic and definition of terms

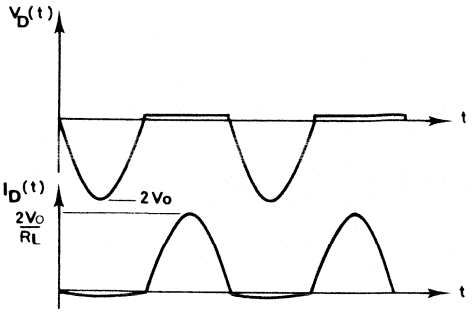


Figure 6
Current and voltage waveforms of one diode leg.

Neglecting the forward voltage drop of the rectifiers, the mean currents flowing through one leg of the rectifier circuit are:

$$I_{av} = \frac{V_o}{R_L} \cdot \frac{1}{\pi} = \frac{I_L}{2} \quad I_{r.m.s} = \frac{1}{2}\frac{V_o}{R_L} = \frac{\pi}{4} \cdot I_L, \qquad (4)$$

where I_L is the average value of the total load current.

The average forward power dissipation of one diode is then

$$P_F = V_{DD} \cdot \frac{I_L}{2} + \frac{\pi^2 I_L^2}{16} \cdot r_D \qquad (5)$$

This function is represented in Figure 7.

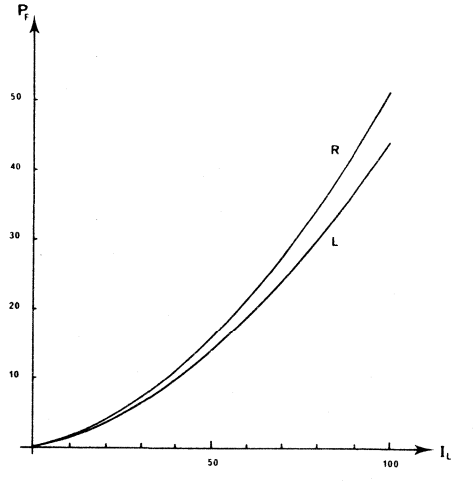


Figure 7
Forward power dissipation per diode as a function of the total load current.

Because neither V_{DD} nor r_D depend noticeably on the temperature, P_F is assumed constant against temperature variations.

The average power dissipation P_R in the reverse direction is given by:

$$P_R = \frac{1}{T} \int_0^{T/2} V_R(t) \cdot I_R(V_R, T_j)\, dt \qquad (6)$$

Where $V_R(t) = 2\,V_o \sin \omega t$ and $T = \frac{2\pi}{\omega}$

This integral can be calculated numerically or graphically from the reverse current data given before.

Numerical integration yields the temperature dependence of P_R given in Figure 8.

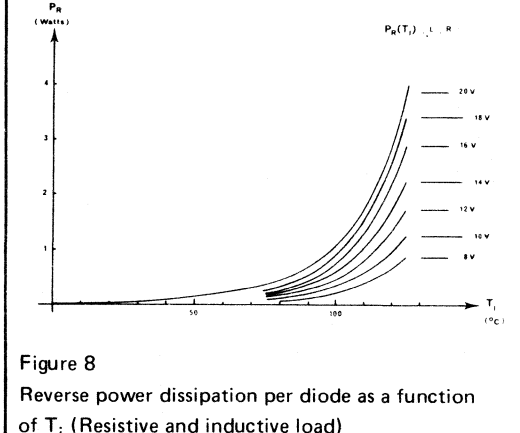


Figure 8
Reverse power dissipation per diode as a function of T_j (Resistive and inductive load)

Inductive filter load

The electrical characteristics of this circuit are determined in Appendix A.

Because thermal problems arise only at fairly large load currents, it is safe to assume that

$$I_L \gg \frac{4\,V_o}{3\,\pi} \cdot \frac{1}{2\omega L}$$

The assumption states essentially that the current flowing through the inductor has a constant value.

Furthemore, the filter capacitor is assumed to be sufficiently large such that the voltage across it can also be considered constant.

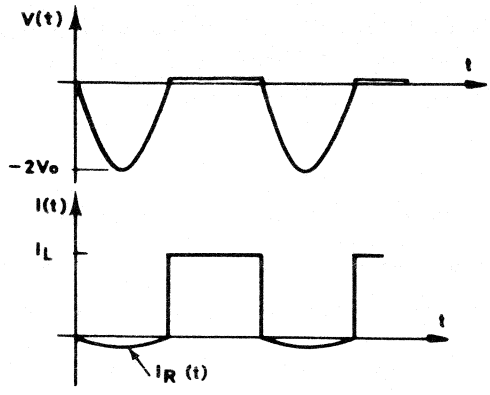


Figure 9
Current and voltage waveforms for one diode leg

The average forward power dissipation per diode – again considered as independent of temperature – becomes

$$P_F = \frac{I_L}{2} \cdot V_{DD} + \frac{I_L^2}{2} \cdot r_D \qquad (7)$$

P_F is shown also in Figure 7 as a function of the total load current I_L. The power dissipation in the reverse direction is found to be the same as calculated for the resistive load. For this reason thermal stability may be evaluated in the same ways as for the resistive load, referring to Figure 8.

Capacitive filter load

It is necessary to refer to appendix B, where the electrical characteristics of this rectifier circuit are treated in detail. The definitions of the terms used are also found there.

The conduction period τ is assumed to be

$$\tau = 0.15\ T, \text{ where } T = \frac{2\pi}{\omega}$$

Figure 10 shows the corresponding current and voltage waveforms.

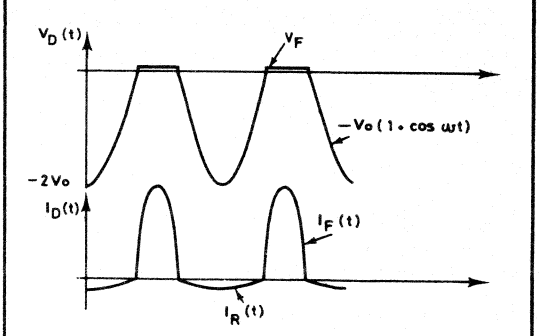


Figure 10
Current and voltage waveforms through one rectifer leg

From the results of appendix B, using formula (B7), and the rectifier data given above, the average forward power dissipation per diode can be calculated:

$$P_F = I_{av} \cdot V_{DD} + I_{r.m.s} \cdot r_D = \frac{I_L}{2} \cdot V_{DD} + 2I_L^2 \cdot r_D \qquad (8)$$

P_F is plotted as a function of the total load current in Figure 11.

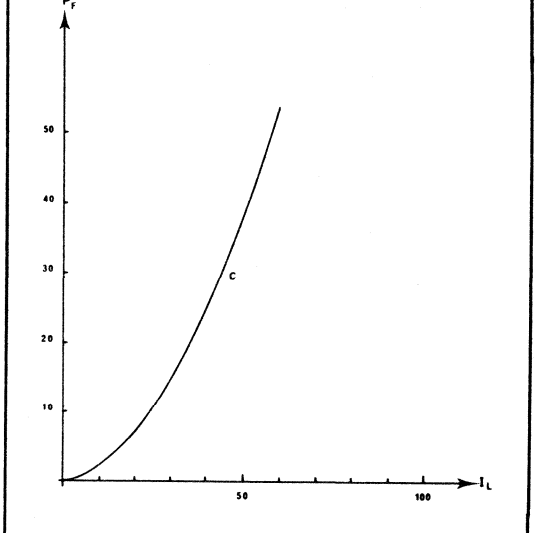


Figure 11
Forward power dissipation per diode as a function of the total load current

To calculate the reverse power, the reverse voltage waveform has to be determined first. This waveform is essentially

$$V_R = -(V_c + V_o \cos \omega t) \quad (9)$$

Where V_c is the dc voltage across the capacitor C. However, as a first approximation, V_c may be considered to be only slightly different from V_o, so putting V_c equal V_o, the equation becomes

$$V_R = -V_o (1+\cos \omega t) \quad (10)$$

The average reverse power dissipation is then given by the integral.

$$P_R = \frac{2}{T} \int_0^{T/2} I_R(t) \cdot V_o (1+\cos \omega t)\, dt \quad (11)$$

This integral can again be evaluated numerically, using the same data as in the preceding two paragraphs for I_R and V_o. The resulting power dissipation is plotted in Figure 12 as a function of the junction temperature T_j.

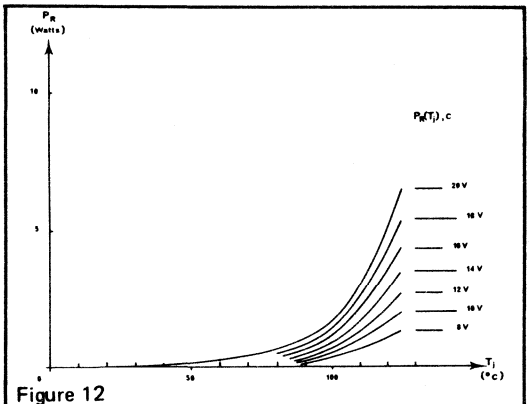


Figure 12
Reverse power dissipation per diode as a function of T_j.

APPLICATION EXAMPLES

The following examples have been chosen to show how the results obtained in the former chapter can be used to calculate the heat sink specifications.

Inductor Filter Input

Assumptions

- Voltage amplitude $V_o = 18$ V
- Total load current $I_L = 28$ A
- Rectifier circuit with center tap transformer
- Maximum ambient temperature $T_{amb} = 35^oC$
- Ambient temperature safety margin $\Delta T_{amb} = +5^oC$.

Problem

Determination of the maximum thermal resistance from junction to ambient allowed for stable operation under the above stated conditions.

Solution

- Calculating the forward power dissipation from equation (7) or taking the value from Figure 7 gives: $P_F = 5.8$ Watts
- The point ($P_F = 5.8$ W, $T_j = 40^oC$) is marked on to Figure 13 (point x')
- The tangent t is drawn from the point x to the 18 V – P_R curve.
- A parallel s to the tangent t is drawn through point x, ($P_F = 5.8$ W, $T_j = 35^oC$)
- The intersection of s with the 18 V – P_R curve is the operating point of the diode:

  $P_F = 5.80$ W
  $P_R = 0.80$ W
  $T_j = 98^oC$

- The reciprocal slope of s or t yields to the total thermal resistance from junction to ambient:

  $R_{th} = 10^oC/W$

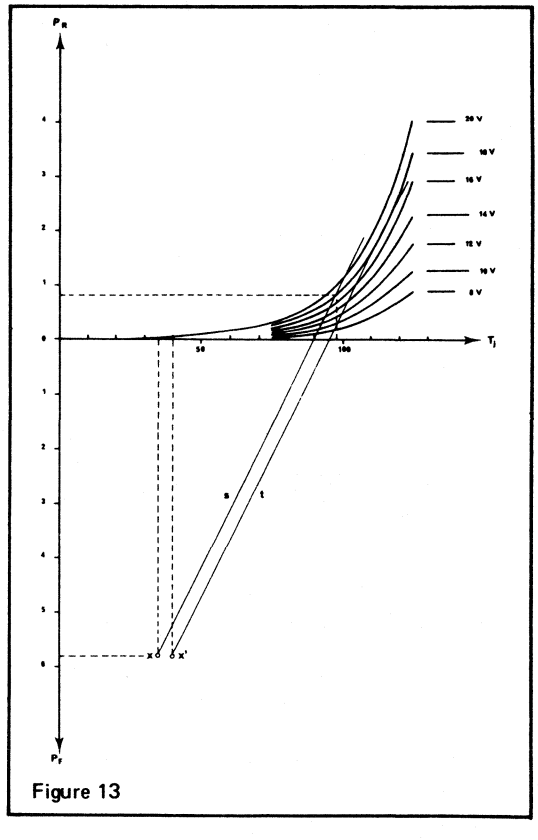


Figure 13

Capacitor Filter Input

Assumptions

- Voltage amplitude $V_o = 32$ V
- Total load current $I_L = 28$ A
- Full wave bridge rectifier circuit
- Maximum ambient temperature $T_{amb} = 35^oC$
- Ambient temperature safety margin $\Delta T_{amb} = +5^oC$

Problem

Determination of the maximum thermal resistance from junction to ambient allowed for stable operation under the above stated conditions.

Solution

- The forward power dissipation is determined from equation (8) or from Figure 11:

  $P_F = 13.45$ W

- The point y', ($P_F = 13.45$ W, $T_j = 40^oC$) is marked on to figure 14.

- The tangent t is drawn from the point y' to the 16 V – P_R curve, because 32 V in a bridge rectifier circuit corresponds to 16 V in a center tap circuit.

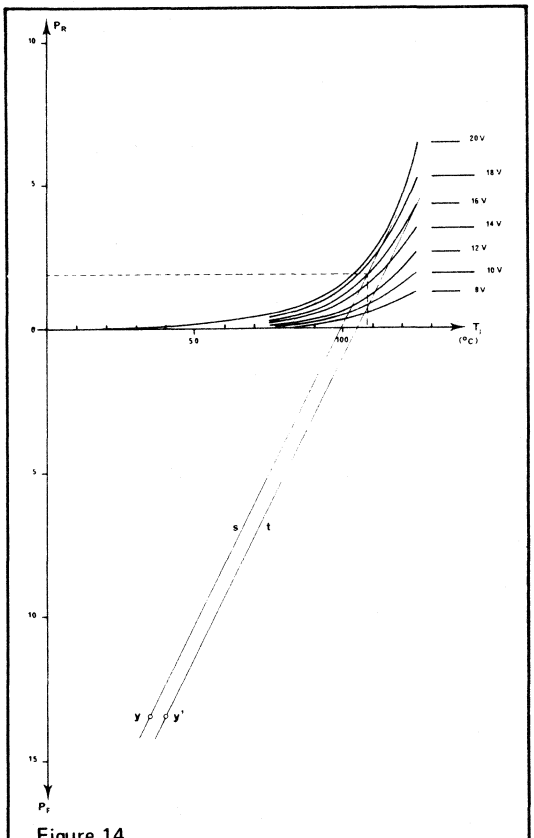


Figure 14

- The parallel s to the tangent t is drawn through the point y, ($P_F = 13.45$ W, $T_j = 35^oC$)

- The intersection of s with the 16 V – P_R curve is the operating point of the diode:

  $P_F = 13.45$ W
  $P_R = 1.9$ W
  $T_j = 108^oC$

- The reciprocal slope of s or t is equal to the total thermal resistance from junction to ambient:

  $R_{th} = 4.85^oC/W$

- If two diodes of the bridge are mounted on the same heat sink, the power dissipation is doubled. Therefore, the total thermal resistance form junction to ambient has, to a first approximation, to be half of the above calculated value, i.e. about $2.4^oC/W$, if thermally stable operation has to be guaranteed.

APPENDIX A

SINGLE PHASE FULL WAVE RECTIFIER CIRCUIT WITH INDUCTOR FILTER INPUT

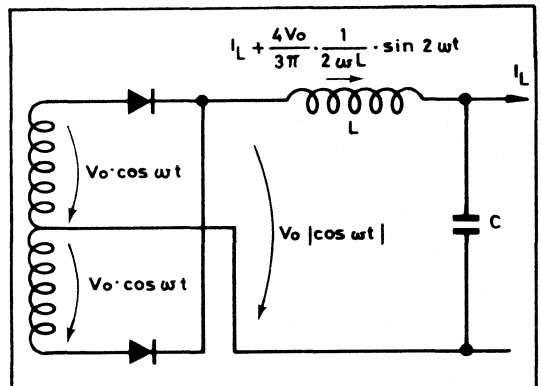


Figure 15
Circuit schematic and definition of terms

The voltage at the input of the filter is of the form

$$V(t) = V_o \cdot |\cos \omega t| \qquad \text{(A 1)}$$

It is assumed that the capacitor C is very large, i. e. the voltage across it can be considered constant

The voltage V(t) can be developed in a Fourier-series with the coefficients:

$$\frac{A_0}{2} = \frac{2V_0}{\pi} \qquad A_n = \frac{-4V_0\,(-1)}{(4n^2-1)\,\pi} \qquad \text{(A 2)}$$

All harmonics with $n > 1$ can be neglected because the second harmonic is already five times smaller than the first one. If the capacitor is very large, the current flowing through the inductor is

$$I_L + \frac{4V_0}{3\pi} \cdot \frac{1}{2\omega L} \cdot \sin(2\omega t) \qquad \text{(A 3)}$$

If the load current I_L is larger than the amplitude of the current due to the first harmonic A_1

$$I_L > \frac{4V_0}{3\pi} \cdot \frac{1}{2\omega L} \qquad \text{(A 4)}$$

the current flow through the inductor will not be interrupted.

This case is the most frequently encountered one in rectifier circuits. The DC voltage across the capacitor is:

$$V_c = \frac{2V_0}{\pi} - I_L \cdot R, \qquad \text{(A 5)}$$

where R represents the total resistance of the rectifier circuit, including the ohmic resistance of the inductor.

The ripple voltage on the capacitor may be calculated, considering only the first harmonic A_1 of the voltage V(t) at the input of the inductor and assuming that the capacitor is very large.

The amplitude A_1 of the first harmonic is attenuated by the L–C voltage divider represented by the filter inductor and the output capacitor. The peak to peak ripple voltage at the capacitor becomes then:

$$V_R = \frac{2V_0}{3\pi\ \omega^2 LC} \qquad \text{(A 6)}$$

If $I_L \gg \frac{4V_0}{3\pi} \cdot \frac{1}{2\omega L}$, the current through the inductor will be nearly constant. The current through each rectifier will then be a rectangular recurrent waveform having a pulse width of half the period of the input voltage and an amplitude equal to the load current

$$I_{peak} = I_L \qquad \text{(A 7)}$$

$$I_{av} = \frac{I_L}{2} \qquad \text{(A 8)}$$

$$I_{r.m.s} = \frac{I_L}{\sqrt{2}} \qquad \text{(A 9)}$$

APPENDIX B

SINGLE PHASE FULL WAVE RECTIFIER CIRCUIT WITH CAPACITOR FILTER INPUT

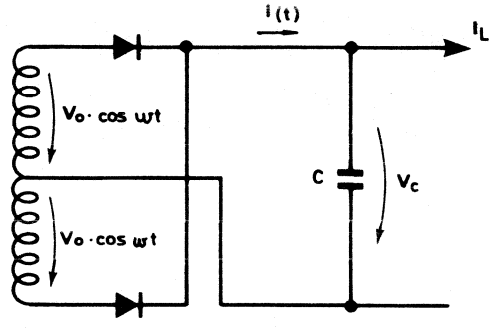


Figure 16
Circuit schematic and definition of terms

The charge being supplied to the capacitor during one period is given, to a good approximation, by the expression

$$Q = \frac{2}{R} \cdot \int_{-T/2}^{+T/2} (V_0 \cos \omega t - V_c)\, dt = I_L \cdot T \qquad \text{(B 1)}$$

Where $T = \frac{2\pi}{\omega}$ (see figure 17)

Developing the cosine and neglecting the higher order terms gives an equation relating the actual dc – voltage V_c across the filter input capacitor to the amplitude of the alternative voltage V_o, the load current I_L and the total rectifying circuit resistance R:

$$(V_o - V_c)^{3/2} = I_L \cdot R \cdot \sqrt{V_o} \cdot \frac{3\pi}{4\sqrt{2}} \qquad \text{(B 2)}$$

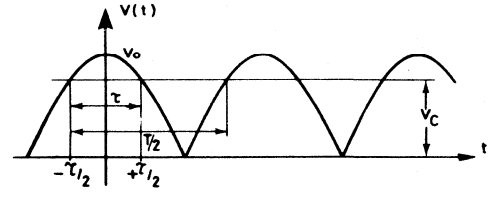


Figure 17
Calculation of the dc output voltage

from the voltage change during the discharge time of the capacitor:

$$\Delta V_c = \frac{1}{C} \cdot I_L \left(\frac{T}{2} - \tau\right) = \frac{1}{C} \cdot I_L \cdot \frac{\pi}{\omega}\left(1 - \frac{2\tau}{T}\right) \qquad \text{(B 3)}$$

ΔV_c is the peak to peak value of the ripple voltage.

At full load τ may be approximatively equal to 0.15 T, a value found in most medium and high current rectifier circuits.

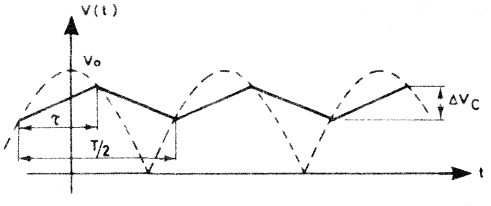


Figure 18
Calculation of the ripple voltage

The capacitor is charged only during the time τ ; this means that, during the time $T - 2\tau$, no current is flowing through the rectifiers. The current through the rectifiers is therefore a recurrent pulse train whose average value equals the load current I_L; the current pulse duration is τ , the duty cycle $\frac{2\tau}{T}$.

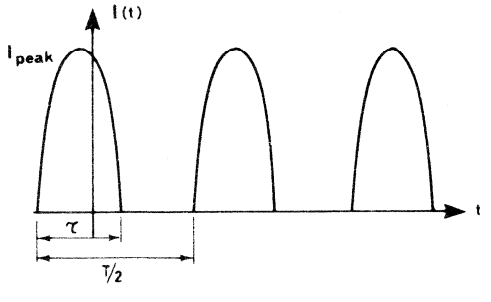


Figure 19
Current through the rectifier circuit

It appears that a parabola is a fairly good approximation fo this pulse waveform. Therefore the following relations between the peak and the mean values hold:

$$I_{av} = I_{peak} \cdot \frac{4\tau}{3T} \qquad I_{r.m.s} = I_{peak} \cdot \sqrt{\frac{8}{15}} \cdot \sqrt{\frac{2}{T}} \qquad \text{(B4)}$$

obtains

$$I_{av} = I_L \qquad I_{r.m.s} = I_L \sqrt{\frac{3T}{5\tau}} \qquad \text{(B 5)}$$

Assuming again $\tau = 0.15\ T$ the following values are found for the total current through the rectifier circuit:

$$I_{av} = I_L \text{ and } I_{r.m.s} = 2\, I_L \qquad \text{(B 6)}$$

$I_{r.m.s}$ is also the current flowing in the secondary winding of the transformer. The mean values of the current per one diode leg are then

$$I_{av} = I_{L/2} \text{ and } I_{r.m.s} = \sqrt{2}\, I_L \qquad \text{(B 7)}$$

AN-316

Application Note

A LINE OPERATED, STABILISED 5 V/50 A SWITCHING POWER SUPPLY

Prepared by
Dr. J.A. Gutmann and R.T. Suvā

This application note describes a regulated 220 V ac to 5 Vdc converter using high voltage switching transistors and schottky barrier rectifiers. The control functions are all performed by integrated circuits.

MOTOROLA Semiconductor Products Inc.

A LINE OPERATED, STABILISED 5 V/50 A SWITCHING POWER SUPPLY

INTRODUCTION

Almost all electronic circuits require a dc voltage supply with some degree of stabilisation. This voltage is normally obtained by rectifying and filtering an ac voltage. The desired stability is produced by the action of certain regulating circuits.

The most widely used regulator is the series linear regulator which is essentially a controlled voltage divider. The ratio of this divider is controlled such that the output voltage remains at a constant level for all specified changes of input voltage and load current. This type of regulator has outstanding properties as far as load and line regulation, noise and regulation response time are concerned. It is particularly suitable for those applications where linear operational amplifiers have to be supplied and noise can be a problem, or where a very high degree of stability is required. On the other hand, a lot of power is dissipated in these regulators because their efficiency is rarely higher than 50 percent. Higher efficiency, however, at the expense of slower regulation response time and higher noise levels, can be achieved by series switching regulators.

In a series switching regulator, the filtered dc input voltage is chopped by a series switching element, in general, a switching transistor. The resulting rectangular pulse train is filtered by a low pass filter, yielding a smooth dc voltage at the output of the filter. The value of this voltage is determined by the duty-cycle of the chopper and can therefore be stabilised electronically by controlling the duty-cycle, with respect to a reference voltage. This type of regulator offers noise and regulation performances that are always inferior by one order of magnitude to the corresponding linear regulators. They are therefore best suited for supplying less critical loads, like digital circuits. The losses in a series switching regulator are caused mainly by the voltage drops of the saturated switching transistor, the forward voltage drop of the freewheeling diode and the power dissipation during the commutation of the switching transistor. Efficiencies up to 85 percent can be obtained with this system.

Both types of series regulator use a transistor as the controlling element which has not only to withstand the full input voltage but also to carry the full load current. Therefore, both systems usually need a mains transformer in order to produce the lowest possible input voltage to the regulator. Transformers operating at 50 or 60 Hz that have to transmit several hundred volt-amperes are heavy and bulky components and frequently prove difficult to place in equipments that have to be compact. The availability of high voltage transistors capable of carrying several amperes collector current have made it possible to design inverter-type switching regulators working directly off the mains voltage without an intermediate 50 Hz transformer.

These inverter switching regulators offer noise and regulation performances similar to the series switching types and can replace them in most applications where price is not the ultimate requirement. They can be built to be more compact and light-weight, at the expense of slightly more complicated electronics, than the equivalent series switching units.

Inverter regulators use either two or four switching transistors for chopping the rectified mains voltage at ultrasonic frequency (usually between 20 and 50 KHz) before applying it to a compact power transformer designed for operation at this frequency. The transformer, generally a step-down, is followed by a rectifier and a smoothing filter to obtain the dc output. The basic inverter configurations of transistors are the full bridge and its derivatives, the push-pull and the half bridge. A discussion of the properties of the last two circuits is presented in AN737 (ref. 1). The choice between these circuits depends on specific conditions such as, magnitude of the mains voltage, available switching devices, desired output power, etc. In brief, the full bridge is mainly used for obtaining very high output powers, above 1 kW. For medium and low output powers the half bridge and push-pull are preferred; they require two high power transistors but only two drivers, as compared to four smaller transistors and four drivers for the full bridge. The disadvantage of requiring transistors of higher power is compensated by a simpler driving circuit.

For high line voltages (typically 220 V) the half bridge is preferred to the push-pull because it requires lower voltage transistors. For low line voltages (typically 115 V) the simplicity of the driving circuit of a push-pull inverter makes it generally preferable to the half bridge, although its potential ability to draw destructive dc current through one leg of the output transformer and also sometimes the necessity of having to isolate electrically the transmission of the output voltage magnitude to the control electronics may require extra efforts to find suitable solutions.

In this note a system is described which uses a half bridge Pulse Width Modulated Inverter to generate a 5V/50A output from 220 volts ac mains. The switching transistors, operated at 20 kHz, are used to produce an ac voltage which is stepped down by a ferrite core transformer to an appropriate value. The secondary voltage of the transformer is rectified and filtered to yield the smoothed 5 Vdc output. Stabilisation of the output voltage is achieved by controlling the duty cycle of the switching waveforms.

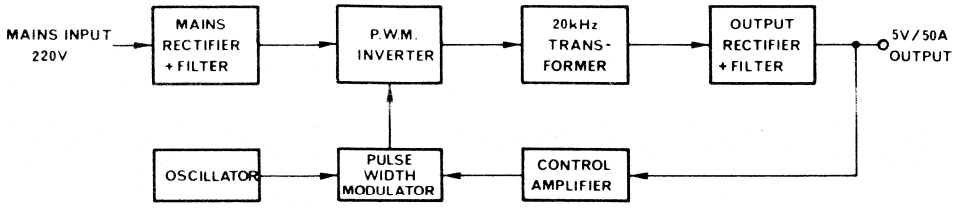


FIGURE 1 – POWER SUPPLY BLOCK DIAGRAM

DESCRIPTION OF THE SYSTEM

General

A block diagram of the complete system is shown in Fig. 1. Rectifying and filtering the mains voltage yields a 310 Vdc voltage which provides the supply voltage for the dc-dc converter generating the 5 volts output.

The control circuitry consists basically of a Pulse Width Modulator, a clock oscillator and a control amplifier. The control pulses generated by the P.W.M. are at clock frequency and have a duration dictated by the control amplifier.

The mains input circuit

The mains input circuit can be seen in detail in figure 2, it consists of a rectifier and a smoothing capacitor. Nominal mains input in 220 volts, 50 Hz. The minimum voltage for a full power output is 190 Vac and the maximum, for the elements selected here, is 260 Vac corresponding to 268 and 367 peak dc volts respectively. The mains is rectified by an MDA 806 bridge and filtered by an electrolytic capacitor of 600 μF. This gives a ripple voltage of 15 volts peak-to-peak at full load and at nominal input voltage. The current flowing from the capacitor to the inverter under these conditions is 1,1 amps dc. The current through the rectifier bridge is 2,4 amps rms.

P.W.M. inverter

The half bridge inverter circuit shown in figure 2 consists of capacitor C_1 and C_2, transistors TR_1 and TR_2 and transformer T_1.

The capacitors C_1 and C_2 divide the dc supply voltage approximately to its mid-value (155 Vdc). These capacitors also prevent any net dc voltage being applied to the primary of T_1. Transistors TR_1 and TR_2 are alternately turned ON and OFF, producing accross the primary of T_1 the stepped ac waveform indicated in the upper half of figure 3, the same waveform that appears across the switching transistors. The current in one transistor is indicated in the lower half of figure 3. At the beginning and at the end of the conduction period the collector-emitter voltage of each transistor changes ideally by half the inverter dc supply voltage (155 volts). The full dc voltage of 310 volts appears at the transistor collector only after the transistors are completely cut-off and draw no more collector current. The peak switching power which the transistors have to handle is therefore, theoretically, the product $1/2\ V_{CC} \times I_C$.

In practice the switch -off portion of the load line tends to extend up to the point V_{CC}, I_C due to stray inductance in the power transformer. Use of an RC snubber network in parallel with TR_2 is therefore recommended to keep the load line within the Safe Operating Area of the switching devices. A practical result obtained with such a technique is illustrated in figure 4.

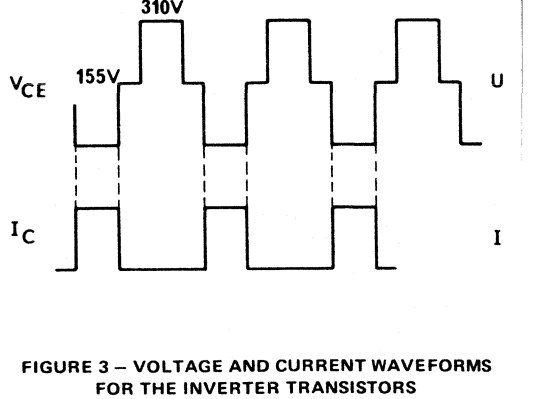


FIGURE 3 – VOLTAGE AND CURRENT WAVEFORMS FOR THE INVERTER TRANSISTORS

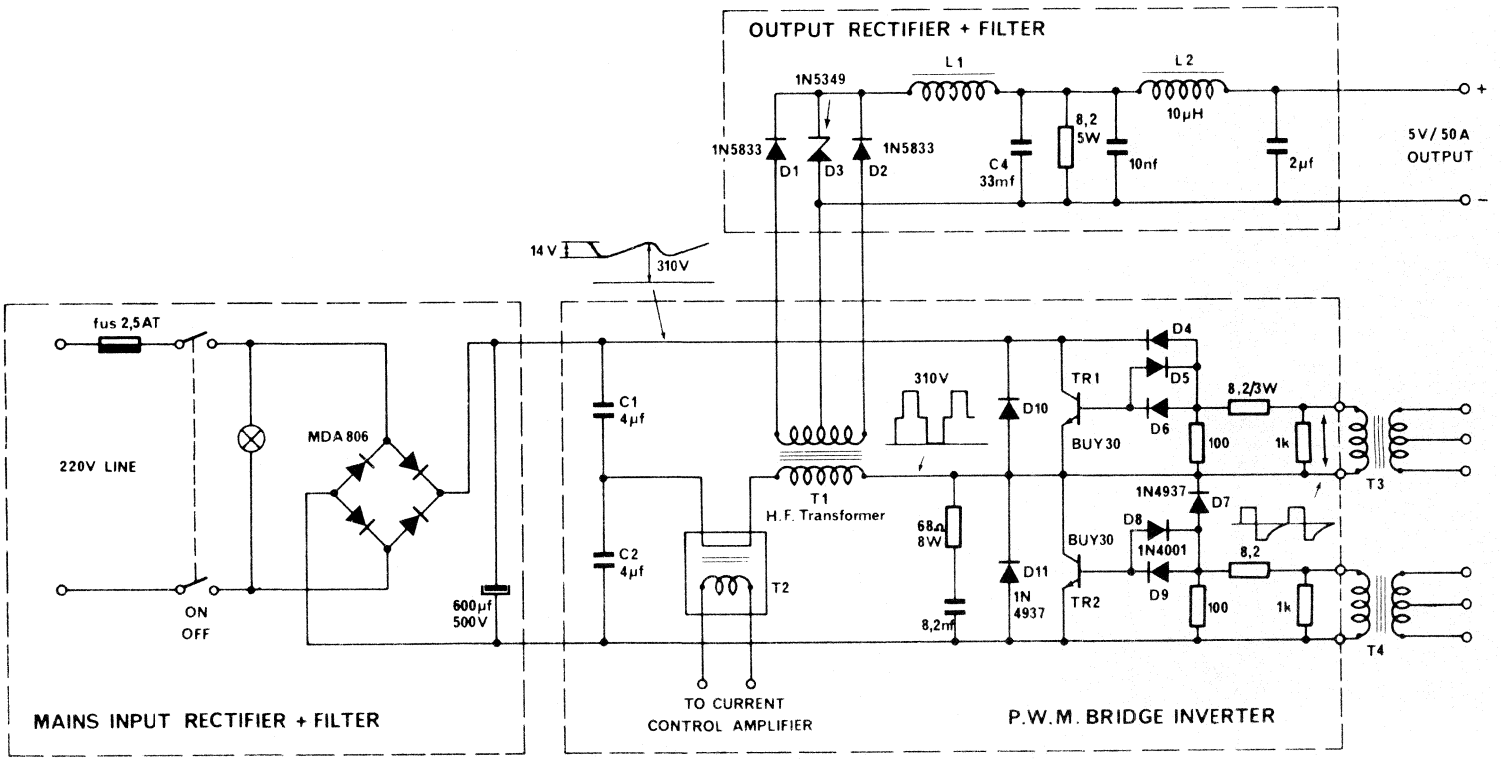
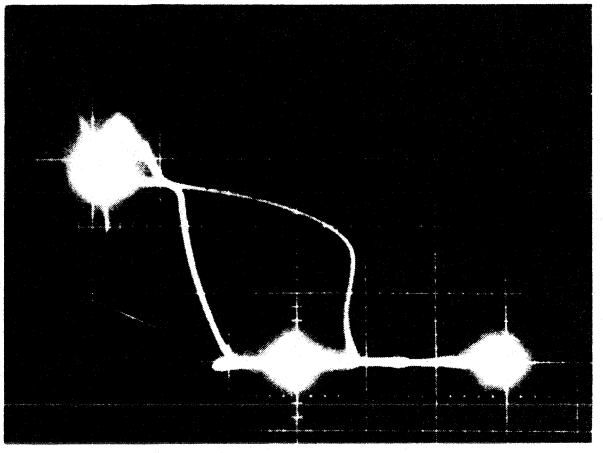


FIGURE 2 – HALF BRIDGE DC-TO-DC CONVERTER



Vertical: 1 A/Div.
Horizontal: 50 V/Div.

FIGURE 4 – LOAD LINE OF THE INVERTER TRANSISTORS AT FULL LOAD

The transistors used in the present design, BUY 30, are fast high voltage triple diffused devices capable of switching currents of 6 A at 250 volts level. In order to keep the devices switching at high speed throughout the complete range from full output load to no-load, great care has to be taken in the design of the base driving circuits. Here, as illustrated in figure 2, use is made of a diode network for avoiding saturation of the transistors. The diodes D_4 up to D_9 very effectively maintain full switching speed for the transistors with any load. A fast recovery type of diode has to be selected for D_4 and D_7.

The transistor dissipation is about 20 watt for both devices together at full load. The required heatsink should have a thermal resistance of about 2,5°C/watt in order to keep the junction temperature below 120°C for a 50°C ambient temperature.

Special care is needed in the design of the ultrasonic frequency power transformer. The winding technique has to be such as to minimize the leakage inductance in order to avoid large voltage overshoots affecting transistor commutation. An interleaved structure was adopted for the transformer windings as shown in figure 5. The primary winding consists of three windings in parallel, the two halves of the secondary winding are sandwiched between the primary ones.

In addition to proper winding techniques, high frequency wiring rules must be observed in order to minimize RF interference and parasitic oscillation.

The following is the specification for transformer T_1:

Core Philips P 66/56 – 3H1
Np = 33 ∅ 0.6 mm
Ns = 8 1 x 6 mm

The current transformer T_2 is used as the detector for the current control loop to limit the output at 50 A. When loaded with 10 KΩ, it provides a signal of about 0,4 V/A.

Construction data for T_2 are as follows:

T_2: Core Telmag HWR 4/5/4, single loop
Np = 1
Ns = 1000

C_1 and C_2 are metallized polyester capacitors with a 20 kHz impedance of approximately 2Ωeach. The ultrasonic frequency ripple across them at full load is about 5 volts pk-pk.

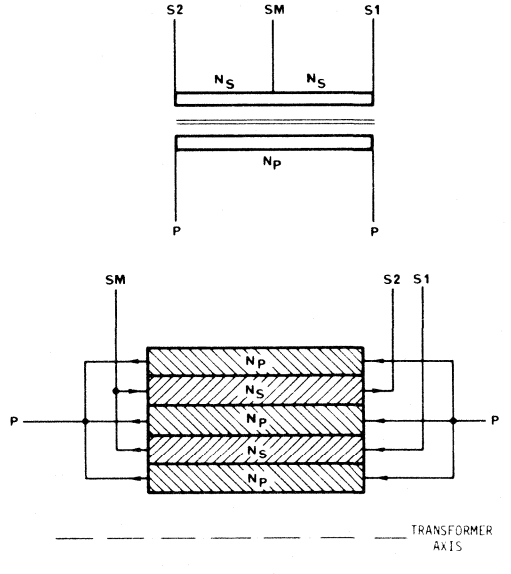


FIGURE 5 – WINDING TECHNIQUES USED FOR THE TRANSFORMER T 1

tput rectifier and filter

e voltage at the secondary of transformer T_1 has an plitude of approximately 9 volts at nominal input volt-. This voltage is rectified by two 40A/30V Schottky tifiers which provide a very efficient high current rec-cation. The thermal power dissipation of these devices full load is approximately 20 watts each and a heat sink at least 1,3°C/w is required to keep their junction tem-ature below 125°C at an ambient temperature of 50°C. ıottky diodes are very sensitive to over-voltages even in form of short spikes; a simple zener diode D_3 protects m against spikes above $2 \times V_Z$ and greatly increases the ability of the system.

e output filter consists of two LC sections with follow-data:

L_1 Core Telmag HWR 40/24/4, double loop with a mm airgap, 23 windings of copper sheet 55 x 0,4 mm

L_2 1 cm^2 iron core with 4 windings of copper flat e 6 x 1 mm.

e first filter section has a series resonance frequency of ıut 400 Hz for greater attenuation of the ripple at the rking frequency and above. The 100 Hz ripple is re-ed by the regulating circuit itself, by as much as 70 dB. e second filter section attenuates the residual commu-ng spikes which can pass the first filter section by ue of the winding capacitance of L_1.

ixed preload of 8.2Ω maintains a minimum of conduc-ı time in the switching transistors and avoids large ts in the dc level at the junction of C_1 and C_2. Such ts would increase the switching power in the switching ices when large loads are suddenly applied.

e control circuitry

e control circuitry is shown in figure 6; it includes all electronic circuits necessary to produce a stabilized dc put voltage with a limited dc output current, by con-ling the duty cycle of the switching power transistors 1, and TR_2 of the inverter. It also contains an overvolt-protection circuit and a reset circuit. Using quad rational amplifiers, the whole circuit needs only 5 IC kages and a few discrete elements, and can easily be lt on a 10 x 16 cm circuit board.

ɔ control amplifiers provide the necessary loop gain to ıilize either the output voltage or the output current ı respect to a given reference. The gain of both feed-k loops can be controlled by adjusting the gain of the ılifiers. No particular frequency compensation of the ɔs was required for their stability.

Pulse-Width-Modulator consists of a linear ramp gen-or and three voltage comparators. The linear ramp gen-or, employing a MC1455 and a small signal transistor, produces the system's clock frequency. The linear p is separately compared to the outputs of the two trol amplifiers and also to a pre-set fixed limiting volt-by three MC3302. The outputs of these three compar-s are connected together in a wired "OR" so that erence is given to the one defining the shorter pulses (i.e. the one defining the lower output voltage). Control of the output voltage is dictated by the voltage loop, up to an output current of approximately 50 A. Above 50 A the current control loop defines the pulse width and causes the output voltage to decrease. The fixed voltage provided by the Limiter defines the maximum length of the pulses and consequently guarantees that in all circumstances (particularly if the input voltage is too low) the switching transistors are both disabled for a few μs at each half cycle. This time, set by potentiometer P_1, is required for the conducting transistor to recover completely before the other transistor is driven ON.

The inverter has to be started with a low duty cycle in order to prevent a large starting pulse (in terms of volt-seconds) from driving the transformer core into saturation and possibly causing high inrush current into the switching transistors. A low duty-cycle start-up network has there-fore been foreseen in combination with the Limiter. When the Reset push-button is pressed, capacitor C_5, initially discharged, causes the Limiter comparator to assume control of the duty cycle and to keep it to a very low value. C_5 is then slowly charged-up through R_5 and the duty cycle is progressively increased until control is taken up by the voltage or the current loop.

The phase splitter provides the correct routing of the pulses from the P.W.M. to the power transistors'drivers. It uses one D-flip-flop MC14013 and two gates MC14023. The pulse train can be stopped by the reset circuit; the drivers and the output power transistors are then auto-matically disabled.

The power transistors' drivers are self-commutating push-pull drivers providing electrically isolated signals to the power transistors by means of the transformers T_3 and T_4. Data for these transformers are as follows:

Core 3H1 18/11
Np 2 x 60
Ns 15

While a positive driving pulse is being transmitted to the bases of the power transistors, energy is stored in the core of these transformers. At the end of each pulse this energy is liberated at the secondary of T_3 and T_4 in the form of a negative 5V pulse applied across the emitter-base junction of the power transistors, resulting in fast recovery of the transistor. During development, it was found useful to include a small fuse in series with the transistors' bases to protect the driving circuits in case of accidental transistor failure.

The overvoltage detector compares the output voltage to a reference by means of a programmable unijunction transis-tor (PUT). If the output voltage exceeds that reference (typically 6 volts) the PUT is triggered and generates a pulse, which, amplified by an MC3302, clocks the reset circuit. An optional thyristor crowbar could easily be added to short the output of the supply so as to avoid damaging the load.

The purpose of the reset circuit, a D-flip-flop MC14013, is to stop the system's clock and disable the output drivers. It is set upon command of the overvoltage detector as well as each time the power supply is switched on, so that it

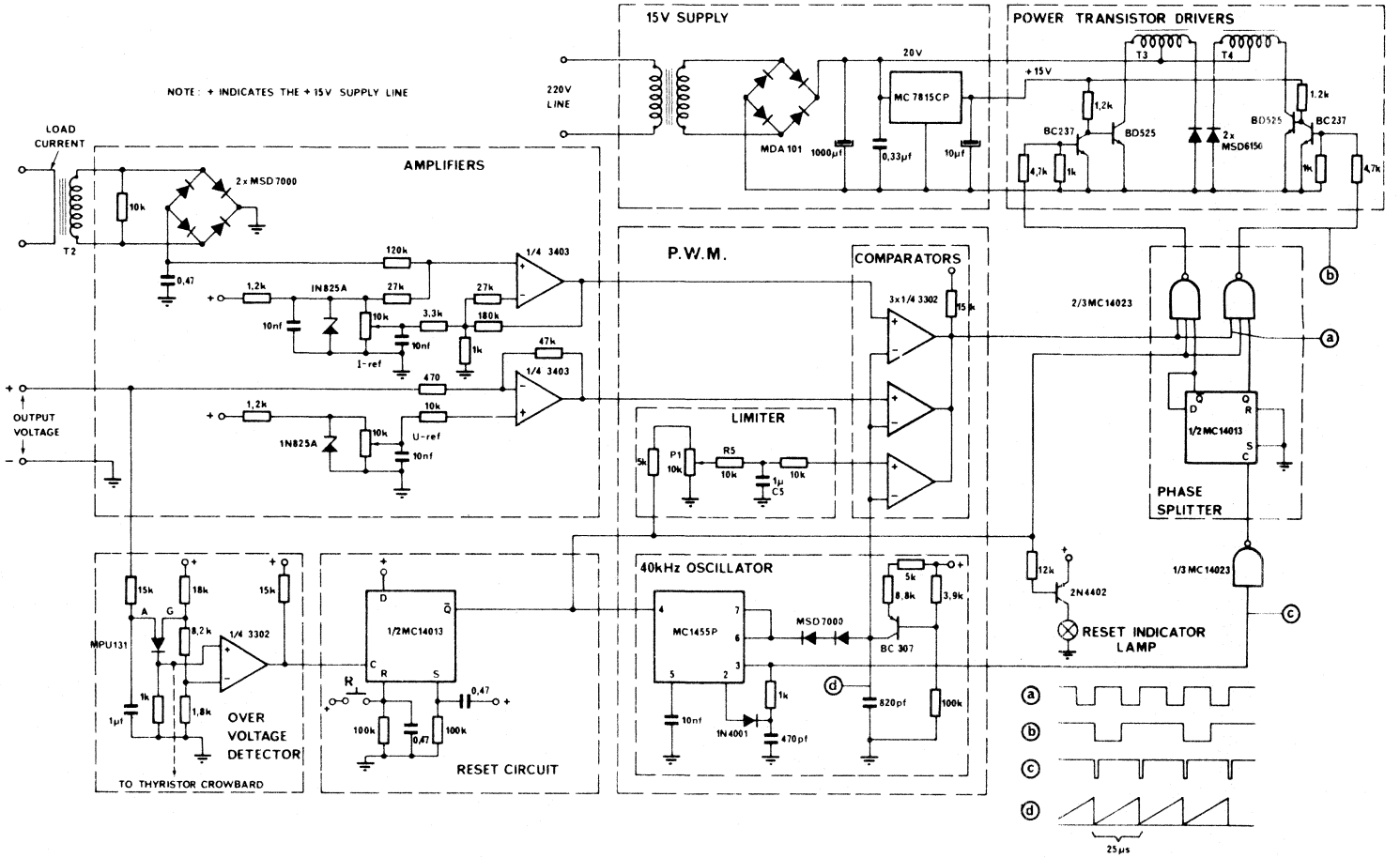


FIGURE 6 – CONTROL CIRCUITRY

insures that the correct supply voltages are present when the clock is enabled. A push button on the front panel allows the circuit to be reset for starting operation.

Performance of the power supply

The output voltage is stable to within +0,2%/o and −0,3%/o, for a line voltage variation between 190 and 260 volts and currents up to 50 A.

Output ripple has a maximum of 25 m volts rms measured with a bandwidth from 10 Hz to 10 MHz. Ripple amplitude is 60 mV peak-to-peak.

Overall efficiency of the power supply at full load is approximately 75%/o.

CONCLUSIONS

The design of a 5V/50A switching power supply working directly off the mains has been illustrated. It has been shown how modern power transistors and high frequency rectifiers can be used in a high performance and yet simple design. Notable simplification of the control circuits was achieved by the use of quad operational amplifiers and quad comparators operated from the same single supply used for the CMOS logic circuits.

The magnitude of the output voltage of a power supply such as the one described here, depends on the choice of the turns ratio of the output transformer and on the suitability of the output rectifier and filter. Only these parts and the gain of the voltage control amplifier would have to be adapted to obtain a 250 watt supply having almost any output voltage.

Ref. 1. Haver, R.J. – Switched Mode Power Supplies – Highlighting a 5V, 40A Inverter Design, AN–737 Motorola Semiconductors Products Inc.

APPENDIX

Estimation of the critical value of the bridge capacitors C1, C2

C1 and C2 should be selected large enough to ensure good efficiency of the power supply, an upper critical value exists however which may lead to saturation of the power transformer T_1 if the switching transistors are not perfectly matched. A quick method for estimating this critical value is given here, it is based on a number of simplifying assumptions leading to an approximate, but worst-case result.

It is supposed that the supply is unloaded, that the resistive components in T_1 are negligible and that a difference exists between the on-time of TR1 and the on-time of TR2. This difference initially gives rise to a net dc voltage ΔV across the primary of T1. ΔV causes a current I_1 in T_1 having the form: $I_1 = \Delta V \sqrt{\frac{2C}{L}} \cdot \sin\left(\frac{t}{\sqrt{2LC}}\right)$

where C is the common value of C1 and C2 and L is the value of the primary inductance of T1.

In the worst case I_1 has to be added to the current in T_1 due to the switching square wave: $I_2 = \frac{Vdc}{4L} \cdot t_{on}$

where Vdc is the rectified mains voltage and t_{on} the equivalent on-time of the power transistors.

If saturation of transformer T_1 is to be avoided, then its total magnetizing current has to be lower than its saturation current I_{sat}:

$$\Delta V \sqrt{\frac{2C}{L}} + \frac{Vdc}{4L} \cdot t_{on} < I_{sat}$$

This condition allows the determination of C for a given set of the other parameters.

As an example, if $I_{sat} = 0{,}3A, L = 15mH, Vdc = 310$ Volt, $t_{on} = 20\mu$ and $\Delta V = 6$ Volts due to a difference of 2 μs between the on-time of TR1 and TR2, then the value of C is 8,5μF

AN-512
Application Note

APPLICATIONS OF FAST-RECOVERY RECTIFIERS

Prepared by
Dave Perkins
Applications Engineering

Many applications that use silicon rectifiers at high frequencies or repetition rates can be improved with fast-recovery diodes. This note discusses the characteristics of these diodes and describes typical applications in which they excel.

MOTOROLA *Semiconductor Products Inc.*

APPLICATIONS OF FAST-RECOVERY RECTIFIERS

NTRODUCTION

Applications of fast-recovery rectifiers are expanding ıpidly. The devices are now available at reasonable cost, ıd many new circuits demand such units. The fast-:overy rectifier is another step toward the ideal diode, ıd while many circuits do not require its excellent charac-:ristics, many applications require or are improved by its sage. Typical applications which require fast-recovery :ctifiers are free-wheeling diodes, circuit isolation, high-'equency rectification, charging diodes (L–C ringing), c-ac high-frequency inverters, series connection of a diode ıd SCR, protection for other semiconductor devices, elim-ıation of commutation voltage transients and reduction f RF noise.

EVERSE-RECOVERY CHARACTERISTICS

Reverse recovery time is the vital characteristic in fast-:overy rectifiers. It is the time that elapses while the ırrent through a previously forward-biased rectifier diode, asses through zero going negatively, until the reverse cur-:nt recovers to a point that is equal to or less than 25% of ıe peak reverse current.

The reverse recovery time (t_{rr}) consists of two distinct parts, t_a and t_b. The first portion is often referred to as the junction recovery time. This term is applied because the junction cannot support the applied reverse voltage because of the stored charge at the junction. The second portion of time is often referred to as the bulk recovery time because the junction has been swept of active carriers, but the bulk material still has some finite action. If the voltage does not reverse across the rectifier, but only drops to zero, then the stored charge (Q) will decay at an exponential rate. The four basic reverse-recovery waveforms are shown in Figure 1. These result when a rectifier is tested in the standard test circuit of the JEDEC JS-1 Committee on Rectifiers, which is shown in Figure 2. Figure 1 (a) and (b) depicts the two common soft-recovery modes while (c) and (d) represents those known as the abrupt-recovery modes.

Since most diodes will display one of these wave shapes, it is necessary to compare the magnitudes of each term to show each diode's true capability. The terms associated with reverse-recovery time are defined as follows:

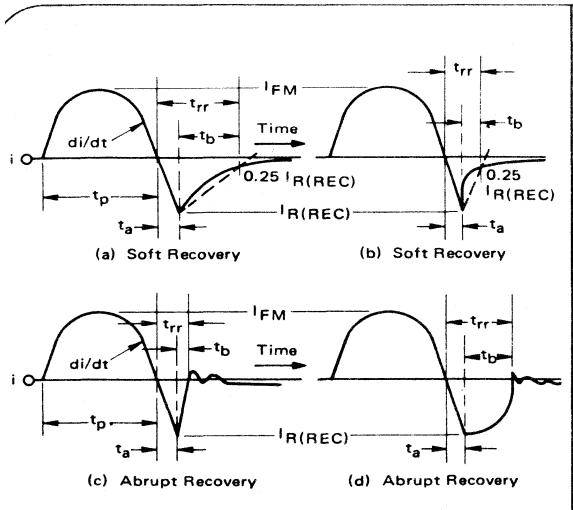
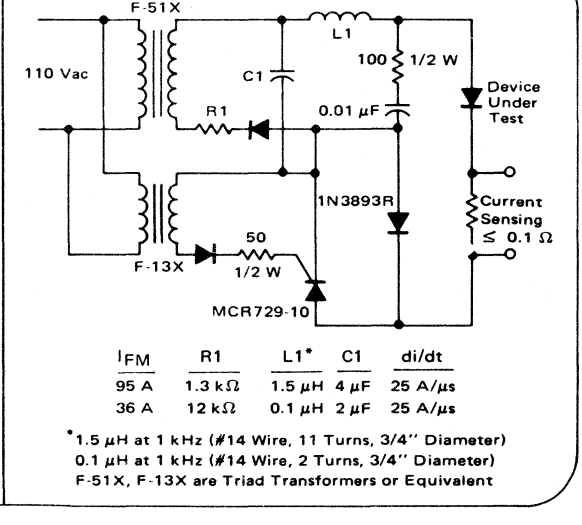


FIGURE 1 – Test Current Waveforms for Various Types of Rectifier Diodes Under Test in the Circuit for Measuring Reverse-Recovery Characteristics



I_{FM}	R1	L1*	C1	di/dt
95 A	1.3 kΩ	1.5 μH	4 μF	25 A/μs
36 A	12 kΩ	0.1 μH	2 μF	25 A/μs

*1.5 μH at 1 kHz (#14 Wire, 11 Turns, 3/4" Diameter)
0.1 μH at 1 kHz (#14 Wire, 2 Turns, 3/4" Diameter)
F-51X, F-13X are Triad Transformers or Equivalent

FIGURE 2 – Standard Test Circuit of JEDEC Committee on Rectifiers

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

t_a = time from zero to peak reverse current

t_b = time from peak reverse current to 0.25 peak reverse current

t_{rr} = total reverse recovery time which is $t_a + t_b$

t_p = forward-current pulse duration ($> 5 \times t_{rr}$)

I_{FM} = peak forward current ($3 \times I_O$)

$I_{R(REC)}$ = peak reverse-recovery current

di/dt = negative slope of forward current (25 A/μs)

Q = total charge stored in the device

$$\int_{t_o}^{t_{rr}} -i\,dt$$

When the various types of diode construction are compared under the same test conditions, distinctly different characteristics are noted. Generally, the conventional diffused diode switches three times faster than the alloyed type, and the gold-diffused diode switches three times faster than the regular diffused diode. Accompanying the faster switching speed of the gold-diffused device is a significant reduction in peak reverse-recovery current and stored charge.

On the other hand, gold doping has some undesirable side effects. Probably the most noticeable change is the reverse blocking-voltage characteristic. Rectifiers are tested for voltage breakdown by measuring leakage current at given voltages, hence it is easy to see that high-voltage, gold-diffused devices are difficult to manufacture compared to conventional rectifiers. Figure 3 shows the effects of gold doping on the reverse blocking voltage.

In addition to its effect on reverse voltage, gold doping may increase forward voltage drop. This parameter is readily

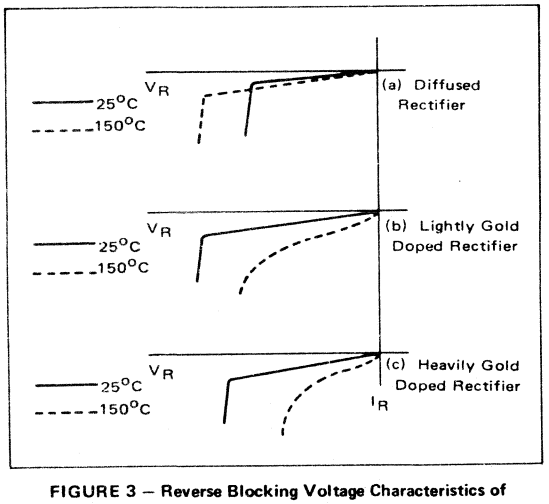


FIGURE 3 – Reverse Blocking Voltage Characteristics of (a) Diffused, (b) Lightly Gold-Diffused and (c) Heavily Gold-Diffused Rectifier

reduced by such techniques as varying the area, thickness and resistivity of the rectifier die.

STORED-CHARGE LOSSES

It has been established that a gold-diffused device has a significantly lower value of stored charge (Q) than standard diffused devices. It is important to understand the advantages of this lower Q. When the peak reverse-recovery current is reached, it is known that at that instant the commutation inductance has a stored energy of $1/2\ L\ I_{R(REC)}$. This stored energy, W, is also equal to one-half the total stored charge times the applied voltage:

$$W = 1/2\ QV = 1/2\ L\ I_{R(REC)}^2$$

Therefore, the energy stored in the circuit inductance is directly proportional to the stored charge of the rectifier. This means that any transient generated by the stored

TABLE I – Typical Values of Total Stored Charge (Q) for Popular Rectifier Lines

Fast Recovery Devices		Diffused Devices	
Type	Typical Charge	Type	Typical Charg
1N4933 Series	0.08 μC*	1N4001 Series	2 μC
MR830 Series	0.12 μC	1N4719 Series	4 μC
1N3889 Series	0.16 μC	MR1120 Series	15 μC
1N3899 Series	0.19 μC	1N1183 Series	20 μC

These values are for a junction temperature of 25°C. The stored charge Q has a positive temperature coefficient of approximately 0.25% per degree centigrade.

*μC = microcoulomb

energy in the inductance is directly proportional to the stored charge. Of course in actual practice the transient never reaches its full potential because of circuit losses.

The potential losses in each rectifier, which cause a corresponding rise in junction temperature, can be estimated with the equation,

$$P_{LOSS} = Wf,$$

where f is the frequency in hertz.

Table I provides typical values of total stored charge Q, for popular rectifier lines.

As an example of the differences in losses, we can compare the potential losses in a 1-ampere, gold-diffused device (1N4935) with a 1-ampere conventional diffused device (1N4003) in a 150-volt 10-kHz converter. From Table

1N4935, $Q = 0.08\ \mu C$

1N4003, $Q = 2\ \mu C$

For the 1N4935, $W = 1/2\ QV$

$= 1/2\ (0.08 \times 10^{-6})(150)$

$= 6 \times 10^{-6}$ joules

$P_{LOSS} = Wf$

$= (6 \times 10^{-6})\ (10^4)$

= 60 milliwatts

Using the 1N4003, $W = 1/2\ QV$

$= 1/2\ (2 \times 10^{-6})(150)$

$= 150 \times 10^{-6}$ joules

$P_{LOSS} = Wf$

$= (150 \times 10^{-6})(10^4)$

$= 1.5$ watts

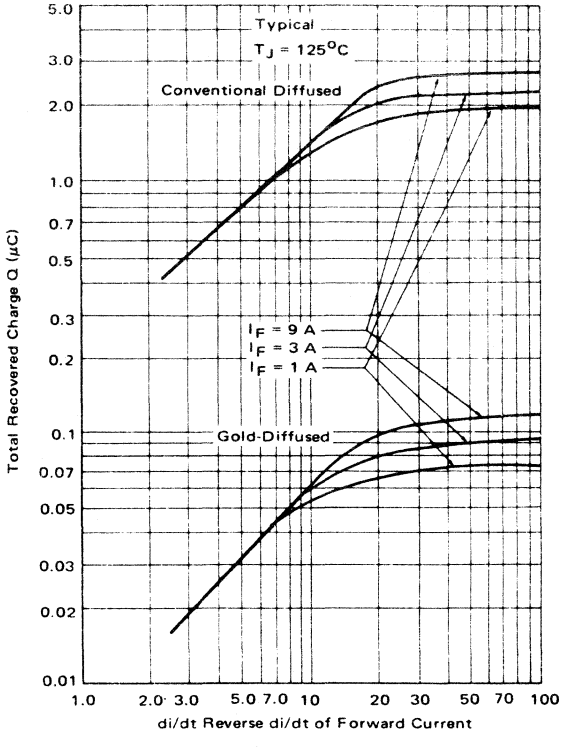


FIGURE 4 – di/dt versus Total Shared Charge Typical Data

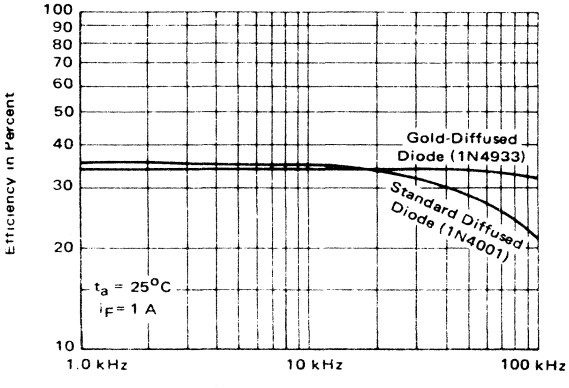


FIGURE 5 – Comparison of Sine-Wave Rectification Efficiency of Gold-Diffused and Conventional Diffused Rectifiers

The actual losses in the rectifier depend on its recovery characteristic. If the recovery characteristic is abrupt, as in all Motorola rectifiers, part of the total potential loss may be absorbed by the rectifier, with the remainder absorbed in the other circuit elements. A device with a soft characteristic will absorb a greater amount of the potential loss. Conservative engineering practices for worse-case designs demand that these losses be considered with the other diode losses to determine the peak junction temperature.

The values for all of the terms discussed, such as t_{rr} and $I_{R(REC)}$, are valid and repeatable in the JEDEC test circuit, and can be readily used for device correlation. These recovery characteristics are very dependent on the circuit used, and can differ in the actual working circuit. For example, Figure 4 shows how Q changes with the rate of fall of current (di/dt) and the forward current.

HIGH-FREQUENCY SINE-WAVE RECTIFICATION

An excellent example of an application where fast-recovery rectifiers are necessary is high-frequency sine-wave rectification. A comparison of the sine-wave rectification efficiency of the standard diffused 1N4001-series of rectifiers and the gold-diffused 1N4933-series is shown in Figure 5. Notice how the efficiency of the standard rectifiers begins to drop slowly even at 1 kHz, and begins to fall rapidly at 20 kHz. The gold-diffused diode is flat to 50 kHz, and even at 100 kHz is only slightly less efficient.

Observing the waveforms as shown in Figures 6 and 7, it is possible to see the drastic difference in rectification of the two devices with a 50-kHz sine wave. The top waveforms show the rectified current, with a large reverse recovery time for the 1N4001 series compared to little or none for the 1N4933-series.

HIGH-FREQUENCY CONVERTERS

Another application in which fast-recovery rectifiers are a necessity is the high-frequency converter with its square-wave output. Figure 8 shows the test circuit used to demonstrate the need for the fast-recovery devices. A full-wave bridge utilizing fast recovery rectifiers and a resistive load was connected to a 50-kHz inverter. After observing and photographing several key parameters, a bridge utilizing standard diffused devices was substituted for the bridge using fast-recovery rectifiers, and the same key parameters were observed and photographed. The supply voltage for the inverter was the same in both cases.

The operation of the rectifiers is best illustrated by observing the voltage and current waveforms for one leg of the bridge. These waveforms are shown for the diffused diode and for the fast-recovery diode in Figures 9 and 10. The peak forward current through the diffused rectifier is several times the peak forward current through the fast-recovery rectifier. A drastic difference between the two devices is apparent from the reverse recovery characteristics While the fast-recovery rectifier has a small reverse current spike of short duration, the standard diffused rectifier has a large reverse current for a much longer period. This large reverse current accounts for power dissipation in the reverse-

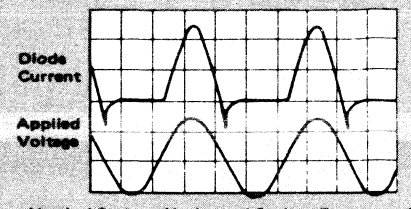


FIGURE 6 – The 1N4001-Series of Diffused Diodes Rectifying a 50-kHz Sine Wave

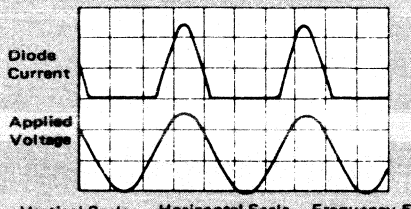
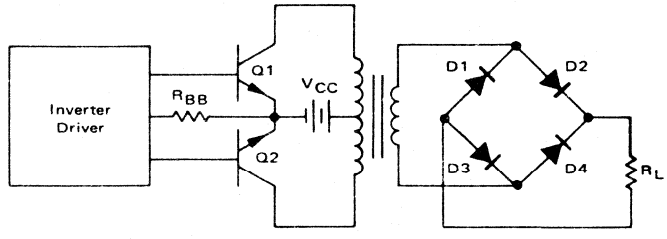


FIGURE 7 – The 1N4933-Series of Gold-Diffused Diodes Rectifying a 50-kHz Sine Wave

FIGURE 8 – High-Frequency Converter



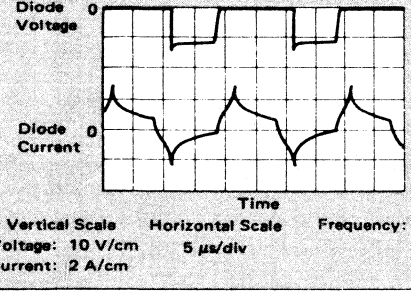


FIGURE 9 – Waveforms for a 1N4719 Diffused Diode Operating in a Bridge Rectifier in a 50-kHz Converter

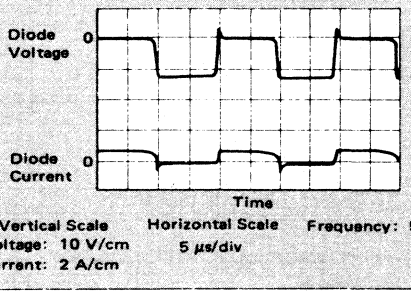


FIGURE 10 – Waveforms for a MR831 Fast-Recovery Rectifier Operating in a Bridge Rectifier in a 50-kHz Converter

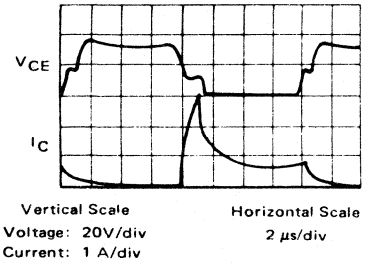


FIGURE 11 – Transistor Collector Voltage and Current for Converter Using Standard Diffused Diodes for Rectification

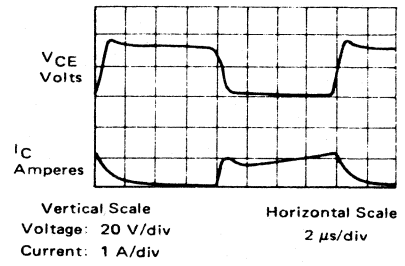


FIGURE 12 – Transistor Collector Voltage and Current for Converter Using Fast-Recovery Diodes for Rectification

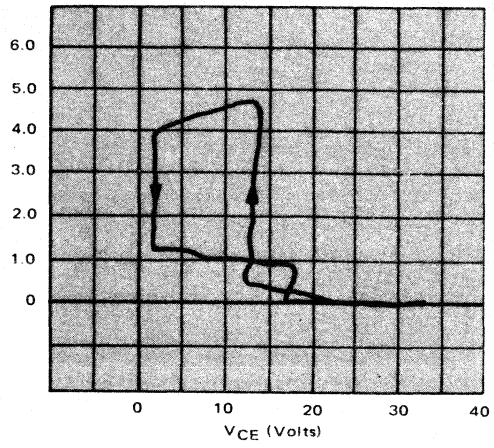


FIGURE 13 – Converter Transistor Load Line with Standard Diffused Diodes Used for Rectification

ased rectifier, and because of the bridge configuration so accounts for part of the forward current of another ctifier in the bridge.

In addition to the increased losses in the bridge, the ffused rectifiers also place a greater demand on the other miconductor devices in the circuit. Figures 11 and 12 ow collector voltage and current for the inverter transtors using the conventional diffused rectifiers and fast-covery rectifiers. Figures 13 and 14 show the load line r these waveforms.

Not only is a higher peak current observed with the ffused rectifiers, but the transistor is also out of saturaon during the switching interval, which greatly increases e switching losses. By combining the information shown the waveforms with the information shown on the load es, one can see the need for better transistor safe opering area in this application when standard diffused rectirs are used instead of fast-recovery rectifiers.

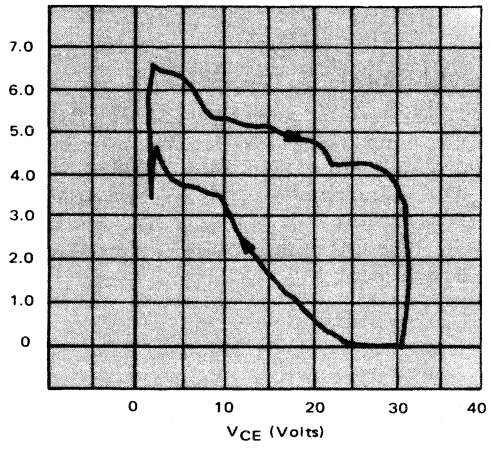


FIGURE 14 – Converter Transistor Load Line with Fast-Recovery Diodes Used for Rectification

In summary, the advantages of using fast-recovery rectifiers for high frequency converters are lower peak forward current and lower losses for the bridge rectifiers, and lower peak current, and lower current gain, safe operating area, and base drive required for the inverter transistors.

In addition, less heat sinking would be required, and the circuit would be more reliable because of lower stress of the semiconductor devices.

INDUCTIVE SWITCHING

Another application which requires a fast-switching rectifier is protection of a transistor switching current at a relatively high repetition rate with an inductive load. Figure 15 is a test circuit that would represent many actual transistor switching circuits such as current regulators. In this application, the base drive was set at a level required to switch the load current to insure saturation of the transistor. The repetition rate of the base drive current was set at 50 kHz. Then as expected, the transistor would fail unless the diode were placed across the inductive load. The discussion is, of

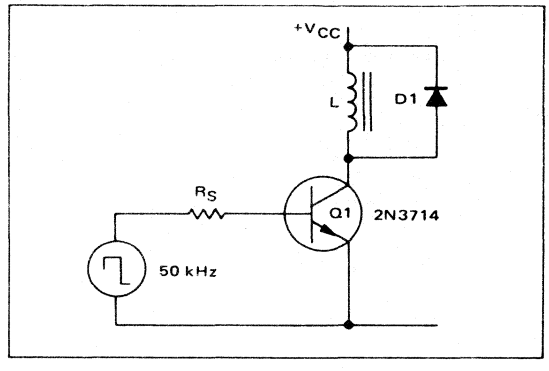


FIGURE 15 – Transistor Switching Circuit with a Clamped Inductive Load

course, based on the difference in operation between the standard and fast-recovery rectifiers and relative to this, the transistor was operated with each type of rectifier in parallel with the inductive load. Figures 16 and 17 show the current waveform through the transistor with a diffused and fast-recovery rectifier respectively. Notice that the peak current with a diffused rectifier is much higher then for the same operating conditions with a fast-recovery rectifier.

Figures 18 and 19 show the load lines encountered for the current waveforms in Figures 16 and 17. They indicated the requirements placed on the transistor for these two types of diodes. If a diffused diode were chosen, the transistor would require higher peak current capability, high current gain, better safe operating area capability, and higher base drive. The fast-switching rectifier would, of course, provide better reliability because of lower stresses placed on the transistor.

All of this discussion is based on an L/R ratio much greater than 10. A lower L/R ratio will reduce the problem,

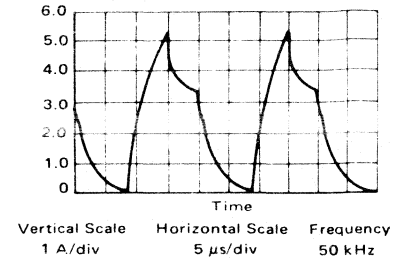


FIGURE 16 – Collector Current Waveform for 50-kHz Repetition Rate with Inductive Load Clamped by a Conventional Diffused Rectifier (1N4719)

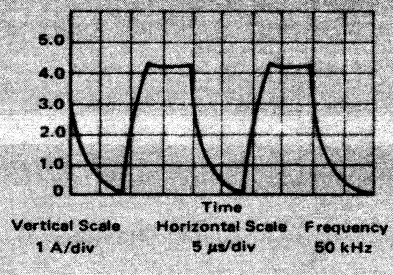


FIGURE 17 – Collector Current Waveform for a 50-kHz Repetition Rate with Inductive Load Clamped by a Fast-Recovery Rectifier (MR831)

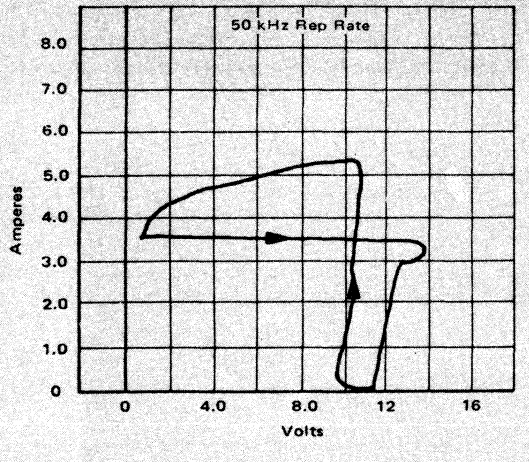


FIGURE 18 – Switching Transistor Load Line for a Standard Diffused Rectifier Operating in Parallel with an Inductive Load (1N4719)

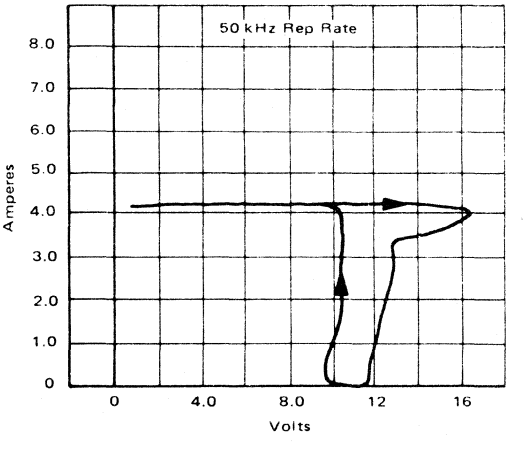


FIGURE 19 – Switching Transistor Load Line for a Fast-Recovery Rectifier Operating in Parallel with an Inductive Load (MR831)

and an analysis of the switching requirements would be needed to adequately define the transistor requirements.

The free-wheeling diode is another example of an application where a gold-diffused diode is needed. In a dc-motor speed-control circuit in a 110-volt line, peak transient voltages of 500 volts were observed with a diffused diode, but the gold-diffused diode yielded only 20 volts above the normal line voltage.

CONCLUSION

Finally, when in doubt as to whether a fast-switching diode should be used, simply insert the two different devices into the operational circuit and observe with a good high-frequency (15 MHz) oscilloscope the voltages and currents of the device and also other semiconductors in that circuit. This will readily indicate whether a fast-recovery diode is desirable.

AN-517
Application Note

IMPROVING THE EFFICIENCY OF LOW VOLTAGE, HIGH-CURRENT RECTIFICATION

Prepared by
Bryce C. Shiner

The efficiency of low-voltage, high-current rectification can be improved by using either Schottky rectifier diodes or synchronous rectification. This note discusses both approaches and compares them to the use of conventional silicon rectifiers.

MOTOROLA *Semiconductor Products Inc.*

IMPROVING THE EFFICIENCY OF LOW-VOLTAGE, HIGH-CURRENT RECTIFICATION

INTRODUCTION

With the ever-increasing need for low-voltage, high-current power supplies* for such systems as thermo-electric coolers and digital integrated circuits (MECL, MTTL, MDTL and MRTL) another look needs to be taken to make this type of power supply more efficient. The basic problem is that a significant amount of the power available at the input to the power supply is dissipated by the rectifying element in supplies using conventional silicon rectifiers, thus reducing the efficiency of the supply.

This application note presents two approaches to increasing the efficiency of low-voltage, high-current rectification over that of using conventional p-n junction silicon rectifiers. One approach is the use of the 1N5832 Schottky rectifier developed by Motorola. The 1N5832 has a lower forward voltage drop than conventional silicon rectifiers, thus making it more efficient.

*A low-voltage, high-current power supply is defined here as being a power supply that has an output voltage of 6 volts or less and a current capability of 5 amperes or more.

The second approach is the use of a germanium transistor with a very low collector-emitter saturation voltage for rectification. This circuit configuration is called synchronous rectification.

SCHOTTKY RECTIFIER

The Schottky rectifier, also known as the hot-carrier or Schottky barrier rectifier contains a semiconductor-metal rather than the n-type to p-type semiconductor junction used in better known rectifiers. This is not a new concept; in fact, this type of device has been used in high-frequency and microwave circuits for several years. The major difference between the microwave Schottky diode and the Schottky rectifier is the much larger contact area between the metal and the semiconductor material in the Schottky rectifier. This results in greatly increased current capability, thus making it suitable for low-voltage, high-current rectification. The Schottky construction also results in excellent high-frequency capability for the Schottky rectifier.

A barrier rectifier can be made using a variety of metals in conjunction with either a p-type or n-type semiconductor. N-type semiconductor material is usually used because it has higher electron mobility.

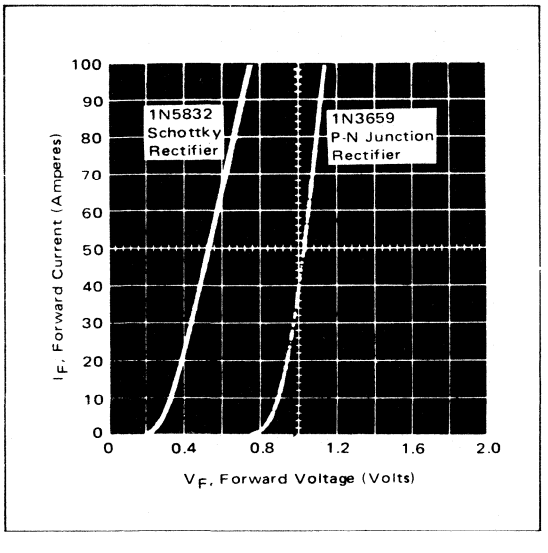


FIGURE 1 – Forward Characteristics of Schottky and p-n Silicon Rectifiers

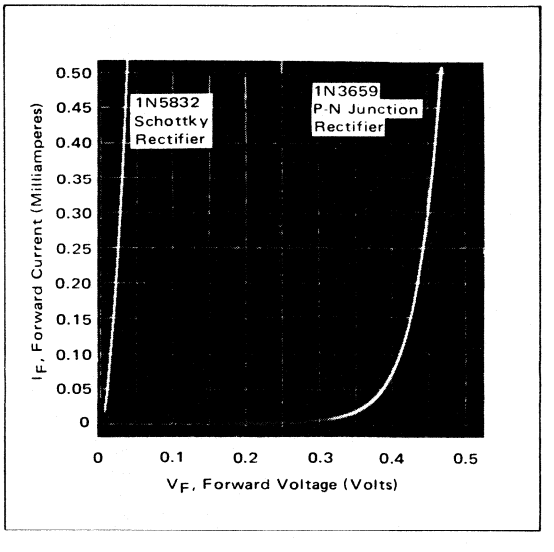


FIGURE 2 – Low-Current Forward Characteristics of Schottky and p-n Silicon Rectifiers

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

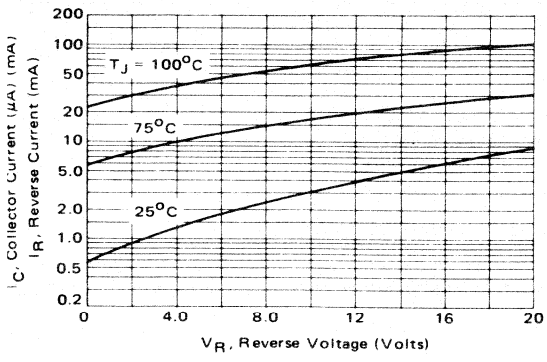


FIGURE 3 – Typical Reverse Leakage

A significant feature of the 1N5832, as shown in Figure 1, is its low forward voltage drop. As the figure indicates, the 1N5832 has a typical forward voltage drop of 0.67 volts at 80 amperes of forward current, considerably lower than the 1.1 volts of the 1N3659 silicon rectifier at the same forward current.

Figure 2 shows the forward characteristics of the 1N5832 and 1N3659 rectifiers at reduced current; the 1N5832 appears to have essentially no offset voltage.

The advantage gained in the forward direction with the Schottky rectifier comes at a slight disadvantage in the reverse direction because of the relatively high leakage current. Figure 3 shows leakage current versus reverse voltage for the 1N5832 Schottky rectifier. However, for a low-voltage power supply, 2 mA or even 10 mA leakage is not significant when compared to 50 amperes forward current, or to the efficiency that results from the low forward drop.

A Schottky rectifier can be used as a direct replacement for diffused rectifiers in low-voltage, high-current power supplies, providing increased efficiency with minimum effort.

SYNCHRONOUS RECTIFICATION

In synchronous rectification a transistor synchronously biased on by the ac input voltage replaces a standard rectifier. Using a germanium transistor with a very low collector-emitter saturation voltage, results in a more efficient low-voltage rectification than possible with conventional rectifiers. The 2N4052 has only 0.3 volts drop at 60 A collector current.

A half-wave synchronous rectification circuit is shown in Figure 4. When points A and C are positive with respect to points B and D, respectively, the base-emitter junction of Q1 is forward biased and collector current flows through the load resistor, R_L. On the negative alternation, when points B and D are positive, the base-emitter junction of Q1 is reverse biased, causing the transistor to block the voltage.

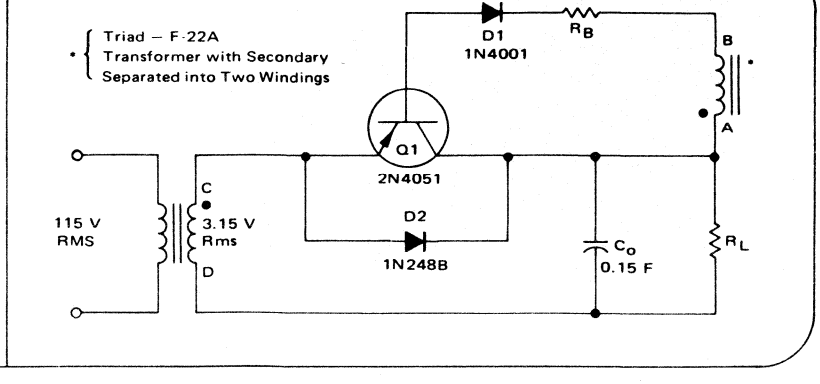
A full-wave rectification circuit is shown in Figure 5. This circuit operates much like the half-wave rectifier, with load current alternately supplied by Q1 and Q2.

CAPACITIVE LOAD

A problem with synchronous rectification occurs when a capacitive load is connected. When the circuit is turned on, because of the large current needed to charge the capacitor, the transistors are pulled out of saturation and can be destroyed because of increased power dissipation, or second breakdown. A solution to this problem is to place a silicon diode (D1 or D2 in Figure 5) across the transistor from collector to emitter (see Figures 4 and 5). Because of the low collector-emitter saturation voltage of the transistor, the diodes do not conduct until the transistors start to pull out of saturation. Then the diodes conduct, supplying part of the increased load current and clamping the collector-emitter voltage of the transistors at a diode drop. As the capacitor charges, the collector current decreases, allowing the transistors to saturate, which turns the diodes off.

A capacitive load results in a slight decrease in efficiency of the synchronous rectification circuit. This is due to the reverse load current that occurs at the turn-on and turn-

FIGURE 4 – Half-Wave Synchronous Rectification Circuit



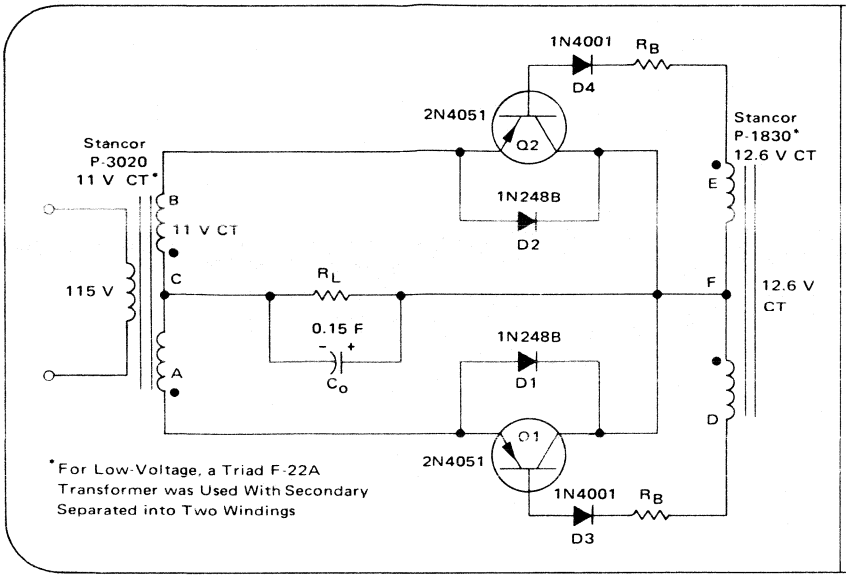


FIGURE 5 – Full-Wave Synchronous Rectification Circuit

off of the transistors. Figure 6 shows the waveform of the load current for the full-wave circuit shown in Figure 5. To understand this phenomenon, assume that Q1 is conducting and Q2 is off. This means that point A is positive with respect to point B. As the voltage at point A decreases below the voltage on capacitor C_O, the voltage at the emitter becomes negative with respect to the collector, and the transistor is driven in the inverted mode. In other words, the collector-base diode is forward biased and the emitter-base diode is reversed biased. Current will then flow through the transistor in the reverse direction causing the capacitor to discharge. The capacitor will discharge until point D becomes sufficiently positive to reverse bias D3, which turns Q1 off. A similar reverse current occurs through Q1 as it is turning on. Point A starts to go positive and at the same time point D starts to go negative. The collector-base junction is now forward biased and capacitor C_O will discharge through Q1. This reverse current flow will continue until the voltage at A becomes more positive tha that of the capacitor, at which time current will begin t flow through the transistor in the normal direction. Sim larly, transistor Q2 has this reverse current during turn o and turn-off.

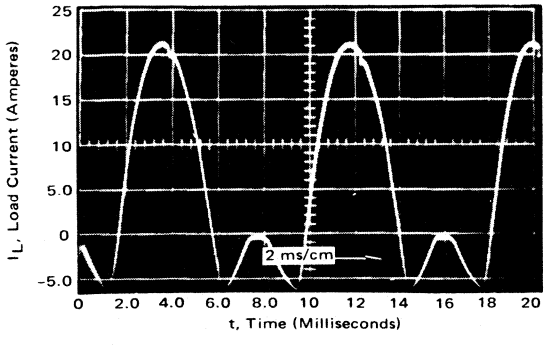


FIGURE 6 – Reverse Load Current for Synchronous Circuit in Figure 5

Although complete elimination of the capacitor dis charge is not practical, two things can be done to keep it t a minimum. Since the base drive is limited, a transisto that has an inverted mode current gain, $h_{FE(inv)}$ of les than one, such as the 2N4052, should be used. A diod should also be placed in the base circuit (D3 and D4 i Figure 5) to cause turn-off of the transistor to begin soone

PERFORMANCE

To provide a means of determining how the Schottk rectifier and the synchronous rectifier circuit compare t a diffused silicon rectifier, curves of efficiency and averag output voltage versus average load current were plotted fo four conditions. The four conditions were high and low voltage (about 6.3 and 3.2 volts) for both half-wave an full-wave rectification. Figures 7 through 10 are plots o efficiency versus average load current for each of the fou conditions and for both resistive and capacitive loads Efficiency as used herein is defined as P_{in}/P_{out} x 10(where P_{in} is the rms power applied to the primary of th transformer and P_{out} is the rms power at the load. Th figures indicate that the Schottky rectifier is the mos efficient.

The efficiency curves all tend to decrease as the loa current increases except for low-voltage, full-wave rectif cation. This decrease in efficiency is attributed mainly t increased transformer losses. For half-wave rectification the transformer is being used on only half of the sine wave This is similar to putting dc through a transformer, whic causes the transformer to saturate, resulting in highe

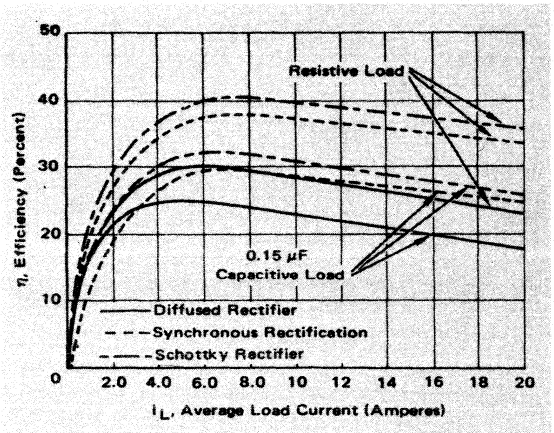


FIGURE 7 – Efficiency versus Load Current for Low-Voltage (3.2 V) Half-Wave Rectification

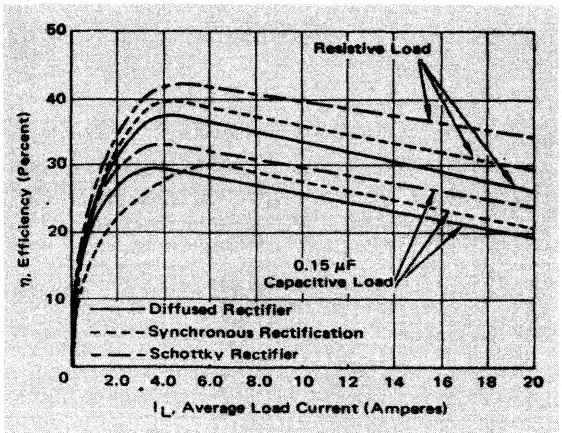


FIGURE 8 – Efficiency versus Load Current for High-Voltage (6.3 V) Half-Wave Rectification

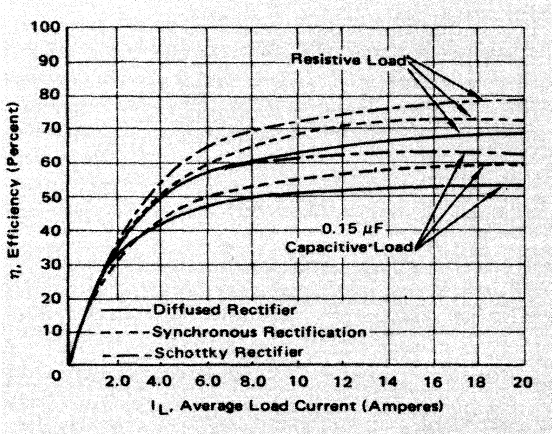


FIGURE 9 – Efficiency versus Load Current for Low-Voltage (3.2 V) Full-Wave Rectification

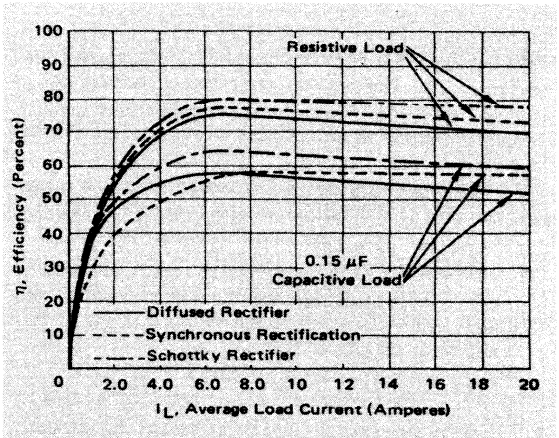


FIGURE 10 – Efficiency versus Load Current for High-Voltage (6.3 V) Full-Wave Rectification

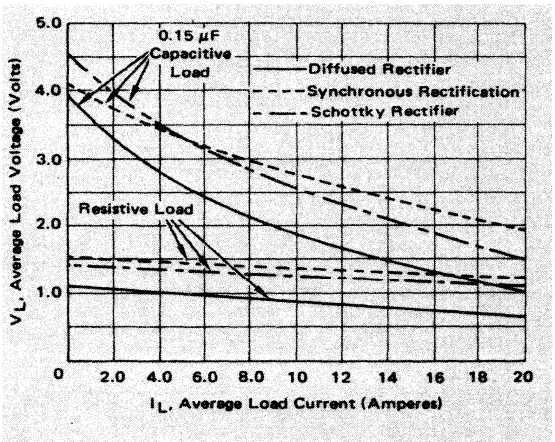


FIGURE 11 – Load Voltage versus Load Current for Low-Voltage (3.2 V) Half-Wave Rectification

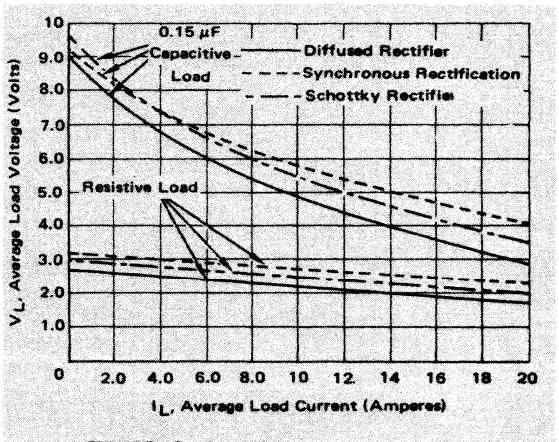


FIGURE 12 – Load Voltage versus Load Current for High-Voltage (6.3 V) Half-Wave Rectification

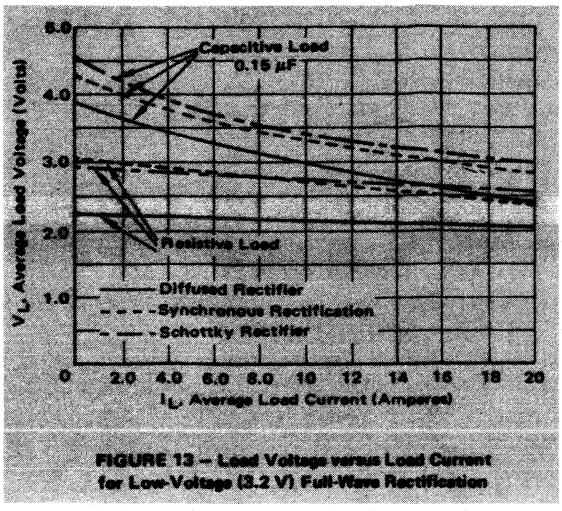


FIGURE 13 – Load Voltage versus Load Current for Low-Voltage (3.2 V) Full-Wave Rectification

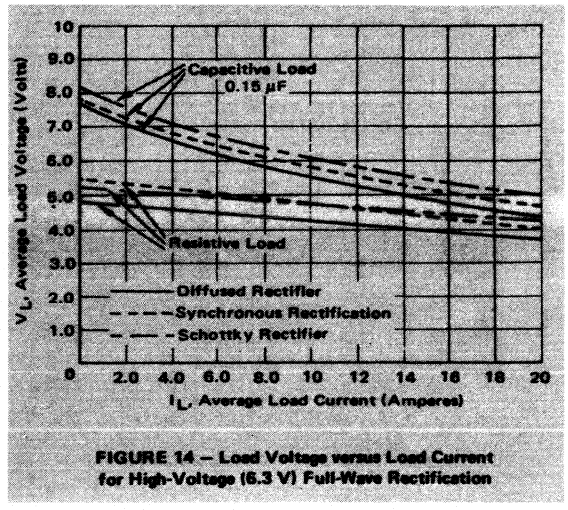


FIGURE 14 – Load Voltage versus Load Current for High-Voltage (6.3 V) Full-Wave Rectification

losses. For full-wave rectification, a 20-ampere transformer was used for the low-voltage tests, and a 10-ampere transformer for the high-voltage test. As a result, the I^2R losses of the 10-ampere transformer were significant enough to cause a decrease in efficiency.

The efficiency curves show that the synchronous circuit is less efficient at low output currents than the Schottky rectifier, and for a capacitive load it is even less efficient than a regular diffused rectifier. This results from the high base current, 2 amperes peak, that is provided at all times to insure that the transistor is saturated at the maximum load current. (The base current is adjusted by changing resistor R_B in the base circuit.)

The average output voltage versus average load current for the four conditions are shown in Figures 11 through 14. In general, synchronous rectification results in the highest output voltage except for full-wave rectification with a capacitive load where the Schottky rectifier provides the highest output voltage.

A square-wave power source was applied to the three rectifying systems to compare the efficiencies. Figure 1 shows a block diagram of the system, in which a 60-hertz 100-watt inverter was used to provide the square wave power. The efficiency versus load current is shown in Figure 16 and the output voltage versus load current is shown in Figure 17. Figure 16 indicates that the synchronous rectification is more efficient that the Schottky diode circuit for the square-wave input.

The efficiency of the synchronous rectification circuit and the Schottky rectifiers were measured at an elevated temperature of 80°C to see whether the efficiency decreased due to the increase in leakage current at high temperature. It was found that for this temperature change the change in efficiency of the two circuits was negligible.

ACKNOWLEDGEMENTS

The author would like to thank Herb Saladin and Nick Freyling for their help in preparing this note.

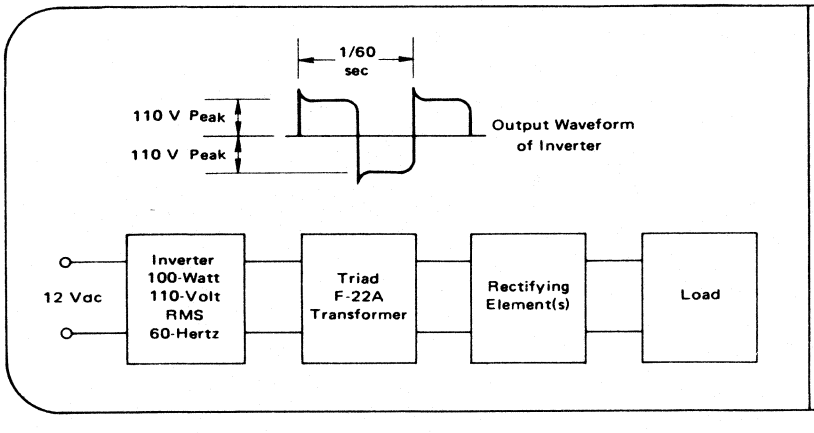


FIGURE 15 – Block Diagram for Rectification With Square-Wave Input

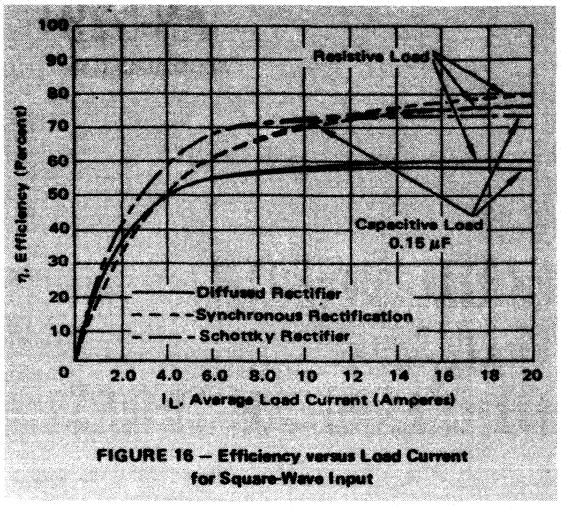


FIGURE 16 – Efficiency versus Load Current for Square-Wave Input

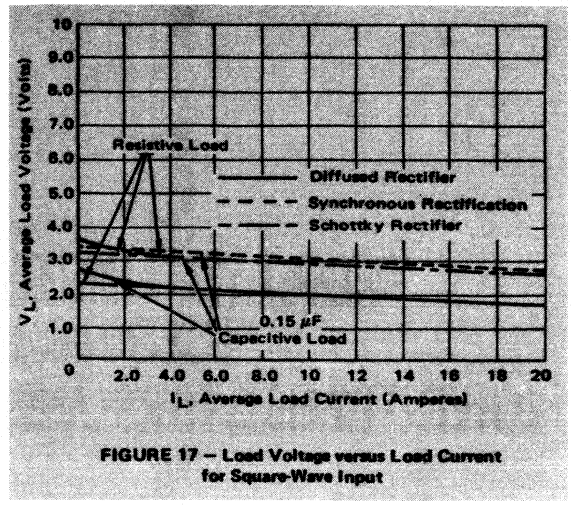


FIGURE 17 – Load Voltage versus Load Current for Square-Wave Input

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AN-529
Application Note

REGULATED LINE OPERATED INVERTER USES HIGH VOLTAGE POWER TRANSISTORS AND HOT CARRIER RECTIFIERS

Edited by
R. J. Haver
Applications Engineering

This report describes a line operated 225 watt preregulated power supply which offers considerable reductions in overall size and weight as compared to more conventional techniques of obtaining low voltages at high currents.

MOTOROLA Semiconductor Products Inc.

LINE OPERATED INVERTER USES HIGH VOLTAGE POWER TRANSISTORS AND HOT CARRIER RECTIFIERS

NTRODUCTION

The circuit shown in Figure 1 is a 15 Volt 225 watt ›ower supply designed for 115V 60 Hz line voltage opera- ion. This circuit makes use of a frequency changing tech- nique in order to reduce the size of transformers and filter- ng components.

This power supply is composed of four major circuits:

1) Series Pass Regulator
2) Inverter
3) Output Rectifier/Filter
4) Error Feedback Amplifier

)ESCRIPTION OF OPERATION

1) Series Pass Regulator

The input voltage, after being rectified by the bridge ·ectifier circuit (D1) and filtered (C1), is regulated by the series pass regulator composed of transistors Q1, Q2 and Q3 and associated components. This regulator sets the voltage at the center tap of transformer T2 at approximately 120 Vdc. As the voltage at the center tap of the transformer (T2) reaches operating potential, capacitor C2 charges to a level necessary to fire the unijunction transistor (Q7). The resulting pulse into the base of Q6 starts the inverter operating.

2) Inverter

The voltage inverter comprised of transformers T1 and T2 and transistors Q5 and Q6 with associated components is a current feedback inverter using positive voltage feedback to enable the circuit to operate into an open circuit. This inverter operates at approximately 20 kHz (See Figure 2), and holds the output frequency relatively constant with respect to changes in load current or input voltage which greatly simplifies the design of filtering systems in the output.

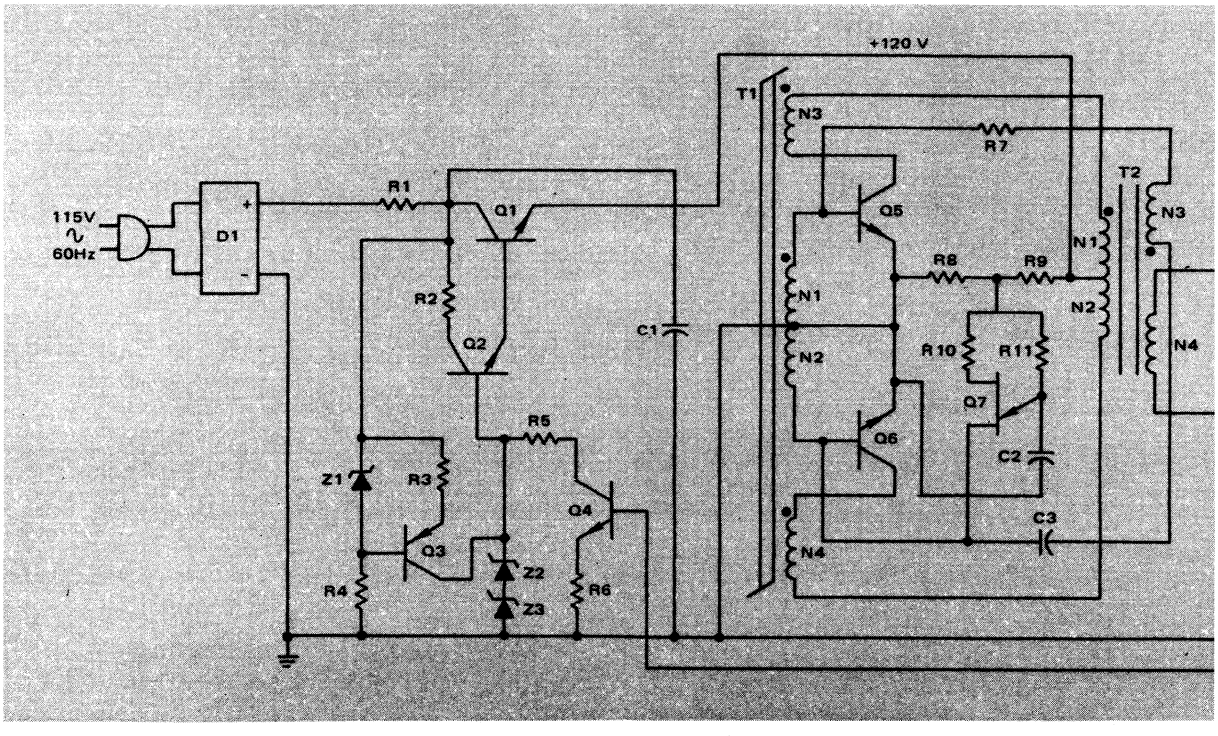


FIGURE 1—Line Operated Inverter With 15 Vdc, 225 Watt Output

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

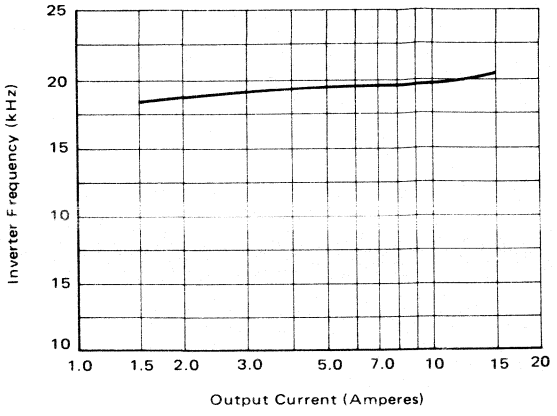


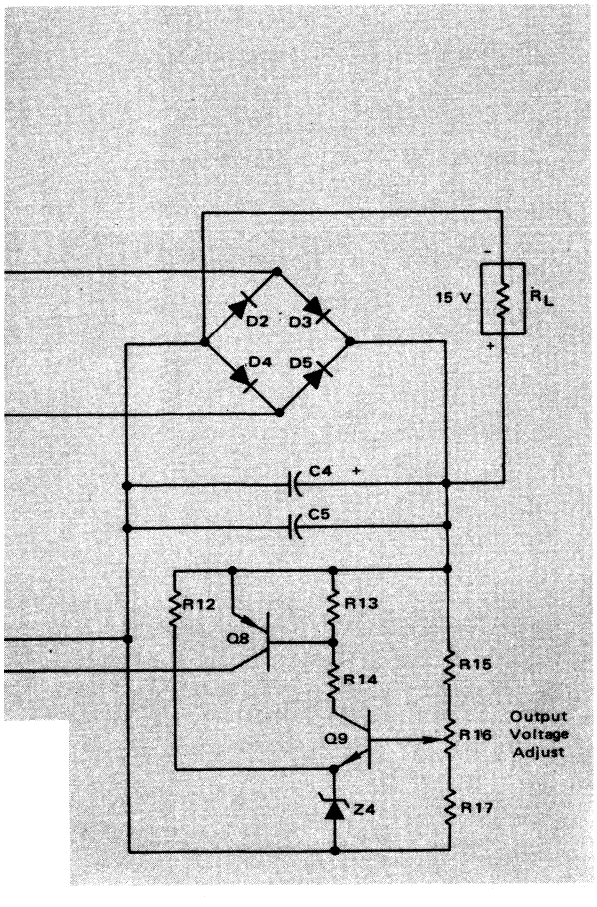
FIGURE 2– Frenquency versus Output Current

When power is first applied between the center taps of transformers Q1 and Q2, capacitor C2 charges and then is discharged by the unijunction transistor (Q7) into the base of Q6. This pulse turns this transistor on and allows current to flow through winding N2 of transformer T2 and N of transformer T1 to ground.

Since transformer T1 is a current transformer, curren flowing in winding N4 will induce a current in winding N The current flowing in N2 drives Q6 into saturation. Sinc the voltage across winding N2 is limited by the emitter-ba diode drop of Q6, this is a clamped winding and will forc the core of T1 to saturate at a predetermined time after Q begins to conduct.

Transistor Q5 cannot conduct during this interval b cause the voltage across N1 is identical to that across N and due to the polarity of the windings, the emitter-ba of Q5 is reverse biased at this time. Once the core of T saturates, N2 loses inductance and ceases to conduct, for ing transistor Q6 to turn off. The collapse of the field winding N2 induces an opposite polarity current into N which turns on transistor Q5. This transistor remains through regeneration from winding N3. When transist Q5 is on, current flows through winding N3 of T1 and N of T2 and continues to flow until transformer T1 aga saturates, this time due to the action of winding N1.

When the field of winding N1 collapses, the resulting i duced current in winding N2 turns off transistor Q5 ar



Parts List

C1 – 2500 μF 350 V electrolytic
C2 – 0.1 μF disc ceramic
C3 – 0.1 μF paper
C4 – 10 μF electrolytic
C5 – 0.25 μF paper

D1 – MDA-980-4 Bridge Rectifier Assy.
D2, D3, D4, D5 – 1N5826, 20 V, 15 A

Q1, Q5, Q6 – 2N6307
Q2, Q4 – 2N5052
Q3 – 2N5345
Q7 – 2N4870
Q8 – 2N3905
Q9 – 2N3903

All Resistors in ohms and ½ W unless otherwise noted

R1 – 1 10 W
R2 – 100
R3 – 82
R4 – 22 k
R5 – 1.5 k 15 W
R6 – 200
R7 – 15
R8 – 4.7 k
R9 – 51 k
R10 – 1 k
R11 – 10 k
R12 – 270
R13 – 1 k
R14 – 7.5 k
R15 – 2.5 k
R16 – 5 k
R17 – 3.5 k

T1 – Core Magnetics Inc. 80623 - 1/2 D - 080
N1, N2 - 20 Turns ea. #30 AWG (Bifilar)
N3, N4 - 3 Turns ea. #20 AWG

T2 – Core - Arnold (6T 5800 D1)
N1, N2 - 100 Turns ea #20 AWG (Bifilar)
N3 - 7 Turns #26 AWG
N4 - 12 Turns ea #12 AWG (#16 AWG, 3 in parallel)

Z1 – 1N4733, 5.1 V
Z2, Z3 – 1N4760, 68 V
Z4 – 1N4736

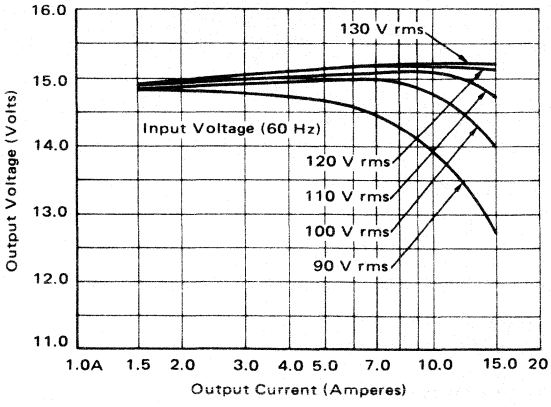


FIGURE 3– Output Voltage versus Output Current at Various Input Voltages

turns on transistor Q6 which repeats the cycle. Since this circuit depends on current in the load to drive the transistors, the inverter will not run into an open load. This problem is overcome by inclusion of winding N3 in transformer T2. This winding makes available positive feedback to the inverter when the load is open and enables the circuit to operate in this mode.

3) Output Rectifier and Filter

The output of T2 is rectified by a bridge rectifier composed of four MBD5500's. These units are hot carrier diodes which, due to their extremely fast switching speed and low forward drop, contribute significantly to the overall system efficiency.

4) Error Feedback Amplifier

The output of the bridge rectifier is filtered by capacitors C4 and C5 before going to the load. The output is simultaneously fed to the error amplifier circuit formed by Q8, Q9 and Q4. This feedback sets the output of Q1 to approximately 120 Volts depending on the setting of R16. In this way, the voltage across the load sets the inverter input voltage which in turn controls the load voltage by a negative feedback.

The purpose of zener diodes Z2 and Z3 is to clamp the output of Q1 at 130 Volts until the inverter is started and control voltage is established into the feedback network. This is done to protect the inverter transistors from peak voltages that could destroy them. When the inverter is operating and load voltage has been established, these zerners do not conduct.

The curves in Figure 3 show the output voltage regulation versus load current at various input voltages.

CONCLUSIONS

This power supply was developed to prove feasibility of a concept and was not optimized for ideal regulation. For information purposes, however, the circuit as shown yields a voltage regulation of ±0.43% no load to full load, ±1.5% with 13% line variation (100V to 130V).

The major advantage of this circuit is the considerable savings in size and weight. This circuit could be installed in a 3" x 6" x 6" package and should weigh approximately 2 pounds. The power transformer of a comparable supply weighs nearly 15 pounds and would be quite large.

AN-588

Application Note

A 20 KHz, 1 KW LINE OPERATED INVERTER

Prepared by
Robert J. Haver
Applications Engineering

This report describes a 1 kilowatt ultrasonic inverter for use in 208-volt, line-operated, computer main-frame power supply systems. This particular design has an output capability of 5 volts at 200 A.

MOTOROLA *Semiconductor Products Inc.*

A 20 KHz, 1 KW LINE OPERATED INVERTER

INTRODUCTION

Featured in this report is an inverter which could become the heart of a small computer power supply. The list of products includes high threshold logic (HTL), darlington power transistors, high voltage power transistors and Schottky barrier diodes. Using an ultrasonic inverter instead of a 60 hertz transformer for power conversion yields the design features of small size and high efficiency. Other features inherent in this particular design are low component count, crossover inhibit of the push-pull output, and internal means of regulation. Even though the output is intended for computer main frames, it can readily be adapted to any voltage/current requirements within the 1 kilowatt power constraint.

OUTPUT REQUIREMENTS

A typical small computer would require three dc voltages as follows:

1) 5 volts at 150 amps with a maximum ripple of 250 millivolts rms for the MTTL logic.
2) 30 volts at 5 amps for the core memory.
3) 100 volts at 1 amp for peripheral equipment including digital readouts, etc.

In addition, it would be operated from a 208 volt three phase line and should have a total load and line regulation of less than four percent.

SYSTEMS APPROACHES

At present, there are two methods of distributing power within the main frame of the computer: central and local. The local system features small on board regulators distributed throughout the computer. These voltage regulators may operate from the raw ac line or from a central high voltage dc supply. Each regulator would supply about 50 watts and approximately 20 of these circuits would be required. In the central method one centrally located regulator is used and must supply power to all the printed circuit cards. In this system, large bus bars are used to distribute the low-voltage, high-current power to the various bays and racks. Since both methods are in use today, it is obvious that many factors enter into the choice of which system to use, economy being one of them. We chose to design a kilowatt power supply simply to illustrate the power capability of our devices.

Several possible system approaches to the design of a large centrally located power supply are shown in Figure 1.

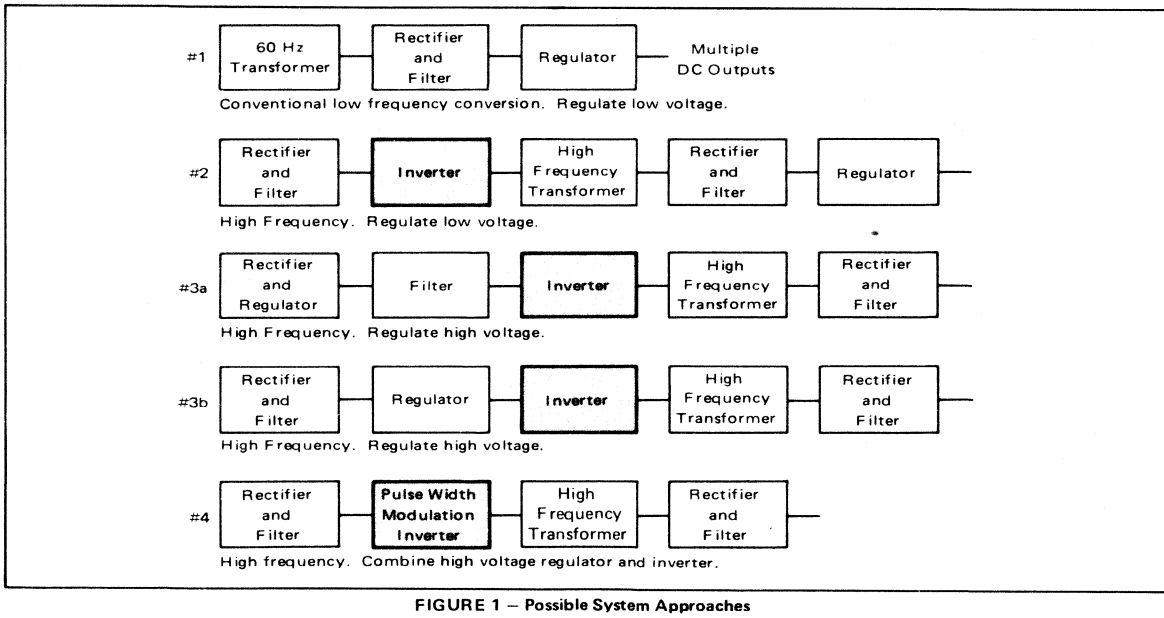


FIGURE 1 – Possible System Approaches

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

The advantages and disadvantages of each system are not too obvious but can be brought out more clearly by some practical considerations. The first system uses a low frequency conversion technique while the remaining three systems operate at ultrasonic frequencies.

System #1. This is a conventional approach which uses a 60 hertz transformer to step down the line voltage for the rectifier and regulator circuits. It has been more economical in the past but is bulky and generates more heat than the high frequency approaches.

System #2. This system uses the same building blocks required of all high frequency regulators but the sequence is varied. The line rectifier is followed by a high voltage, high frequency inverter and the regulation is accomplished at the low voltage, high current outputs of the inverter transformer. Each output can be individually regulated to provide precise voltage control over wide variations in load. There are two drawbacks to this approach: (1) several low-voltage, high-current regulators are required and (2), the efficiency will be lower than the remaining approaches which regulate the high voltage and low current power.

System #3. This system uses high voltage regulators to power the inverter which drives the low voltage rectifiers and filters. The regulator may use SCR's for the phase control (3a) or high voltage transistors in either a linear or switching mode (3b). Of the two approaches, the SCR may be preferred because of economy. In both this approach and approach #4, only one output can be regulated, usually the 5 volt. This is not a serious drawback because line regulation is common to all outputs and slight changes in the memory and peripheral equipment supplies due to load changes are not critical.

System #4. This system is similar to #3 except regulation is accomplished in the inverter circuit by using pulse width modulation (PWM) techniques. It conserves power devices but does require a more elaborate high-current LC output filter.

There is an obvious advantage in choosing a high frequency regulator over the low frequency version. The size and weight of the transformer and filter components will be reduced by an order of magnitude when operating with 20 kHz instead of 60 Hz. The semiconductor component cost is of course higher, but the cost savings in the large passive components generally offsets this increase. The heart of high frequency regulators is the high voltage, high frequency inverter. The inverter circuit shown in this note could be used with any one of the three high frequency approaches with only slight modifications. The most practical approach appears to be #4 (the PWM regulator/inverter).

BLOCK DIAGRAM DISCUSSION

The block diagram, Figure 2, functionally describes the system operation. A free-running oscillator generates the master control signal and determines the frequency of operation. This signal, routed to a phase splitter, provides complementary square waves which are individually processed for controlling the power outputs. The processing involves a three-input NAND function whose inputs are obtained from the phase splitter, the pulse ON delay, and the crossover sense.

The crossover sensors monitor the collector voltages of the output devices and provide a GO signal to the complementary channel only when its respective device is sufficiently turned off. This prohibits simultaneous conduction of both output devices.

The pulse ON delay provides the GO signal to the NAND function after a predetermined time delay. In essence, it provides a pulse-width modulation capability of the output that can be utilized for regulatory purposes. It primarily serves to induce a dead zone into the crossover region that effectively shapes the output load line and consequently permits the usage of lower voltage output devices (35C vs 700 V_{CEO}).

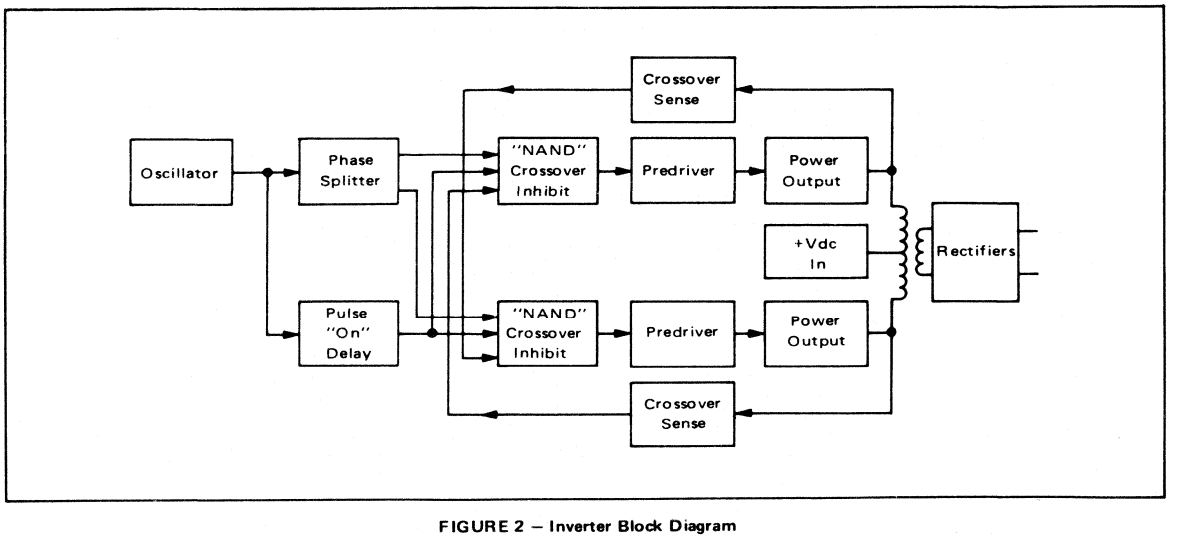


FIGURE 2 – Inverter Block Diagram

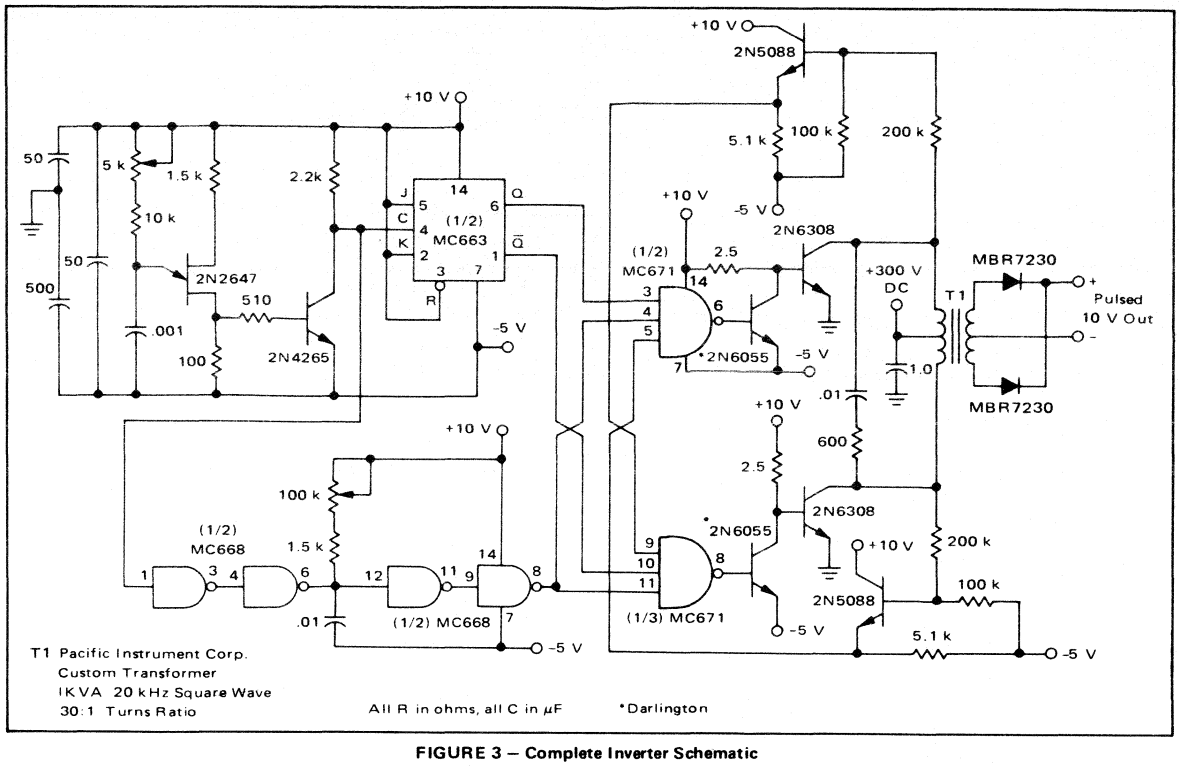


FIGURE 3 – Complete Inverter Schematic

Once the crossover inhibit NAND simultaneously receives the three go signals, it then enables its respective predriver that in turn drives the output device.

The output is in a push-pull configuration with a transformer output that provides the voltage/current conversion desired. The transformer output is then rectified and filtered.

The timing diagram and typical waveforms are shown in Figure 4. Basic timing begins with the sawtooth waveform (A) at the UJT emitter. The negative going clock pulse (B), triggers both the flip flop (C) and the one shot (E).

At this time, drive to the opposite power transistor has just been removed. The feedback signal (D) however, remains low and inhibits drive until storage time has elapsed. The one shot (E) also remains low for the first portion of each alternation. Drive from the NAND gate (F) is applied to the output stage when the one shot resets. On the second clock pulse the flip flop changes state and the same sequence of events occurs to drive the other channel (G). Basically, the power transistors are turned on (H & I) for the remaining portion of each alternation after the one shot delay. Power is supplied to the load (J) only during the time these transistors are on.

DETAILED CIRCUIT DESCRIPTION

The complete schematic, Figure 3, shows in detail how this is accomplished. The inverter requires three supplies to operate, +10 V, -5 V and +300 V. The +10/-5 V supplies provide forward and reverse base drive to the output transistors and drive the discrete and IC logic circuits which are floating between these supplies. The 300 V supply is for main power to the load and would normally be obtained from full wave rectifiers on a 3 phase, 208 volt power line.

The relaxation oscillator uses a UJT to generate clock pulses at 40 kHz rate. These pulses are shaped in the oscillator section and fed to a MHTL JK flip-flop which performs a phase splitting and frequency dividing function. The outputs of the JK are two 20 kHz square waves, phase shifted by 180°. The next stages now have duplicate internal circuits in order to drive the final pair of inverter transistors. NAND gates are used as a comparator circuit to control the output stage.

The one shot input signal to the NAND gate delays the leading edge of the drive signal. The one shot can thereby be used to effect variable duty cycle regulation.

During this delay, the transformer primary voltage drops from twice the line-to-line voltage. This secondary effect shapes the output transistor load lines and these devices operate in their active region only after the transformer voltage drops below their V_{CEO} rating (from 600 V to 300 V). Operation within SOA is thereby insured.

Manual control of the output duty cycle is obtained by using a pot in the one shot circuit. For closed loop feedback, we recommend an opto-coupler from the filtered output back to the one shot to maintain the load-line isolation inherent in the inverter transformer.

In the output stage, NPN low voltage darlington tran-

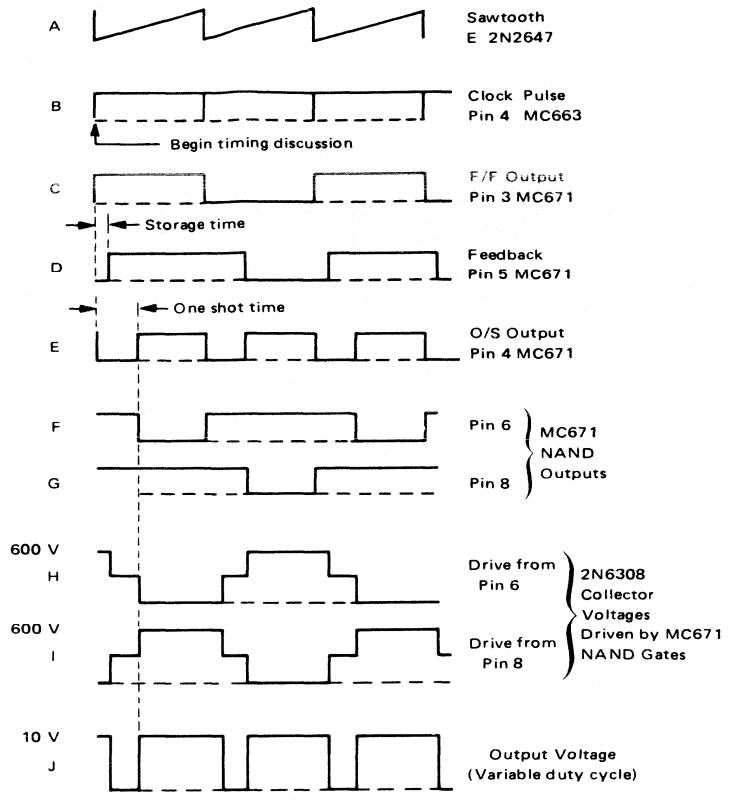


FIGURE 4 – TIMING DIAGRAM

sistors provide both forward and reverse base current drive to the high voltage power output transistors. The 350 V, 8A output transistors operate in a push-pull configuration to drive the center-tapped inverter transformer primary winding at a 20 kHz rate.

Waveforms of actual currents and voltages in our 2N6308 output power transistor are shown in Figure 5. In Figure 5 (A), the inverter is operating at rated power into a 50 milliohm resistive load. The load is receiving 10 V and 200A on a 60% duty cycle (15 of 25 μs) from the inverter. The collector current is relatively constant at 7A during this time. Forward base drive is 4A which gives excellent sat voltages (less than 2 V). Turn off is enhanced by using the darlington driver (our 2N6055) to sink reverse base current (about 2A) during the recovery time of the 2N6308. The fall time on collector current is about 1.0 μs. An output filter which would normally be used to smooth out the output voltage waveform was not available for this test. As a result of this, there is excessive ringing on the collector voltage waveform which could cause SOA failures.

In Figure 5 (B), available filter elements were used to illustrate their effect on load and collector voltages. The inverter is now operating at a reduced power level of 250 watts. The load voltage is 5 VDC and supplies 50A continuously into a 100 milliohm load. The load voltage is quite clean except for switching spikes of 100 mV peak-to-peak. Ringing in the collector voltage has essentially been eliminated and the distinct step waveform is now more obvious.

The load line for the output transistors is shown in Figure 6 and correspond to the time base information in Figure 5 which was previously discussed. The switching philosophy that was adopted for this design revolves around the V_{CEO} rating of the 2N6308 output transistors. The transistor may be allowed to operate in its active region and conduct current while switching below 350 V (the CEO rating) subject only to SOA limits. However, these devices have very little current capability when operated in an avalanche region beyond CEO and should only be required to block voltages up to their 700 V V_{CEX} rating. The load lines in Figure 6 (A) and (B) illustrate that this is the case. The delay in drive signals allows the transformer voltage to drop from 600 V to the line voltage of 300 V before turn on occurs. In a similar fashion, turn off currents decrease to zero at 300 V rather than 600 V because drive to the opposite side is delayed by the crossover and one shot circuits.

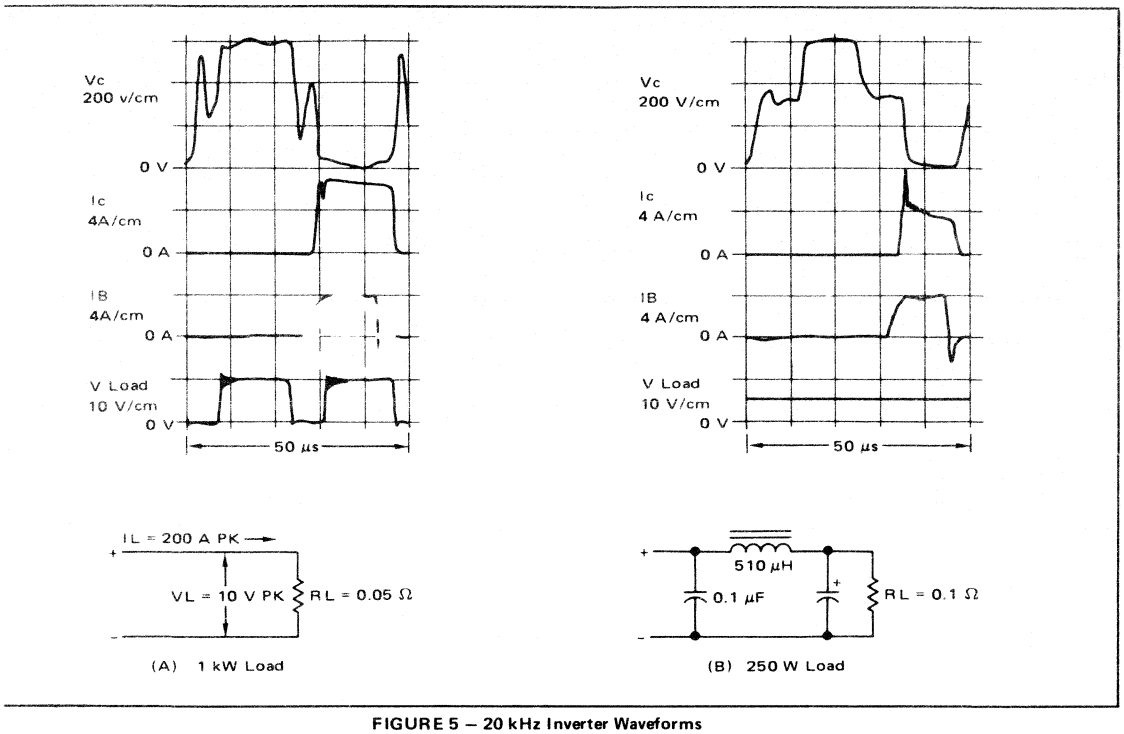
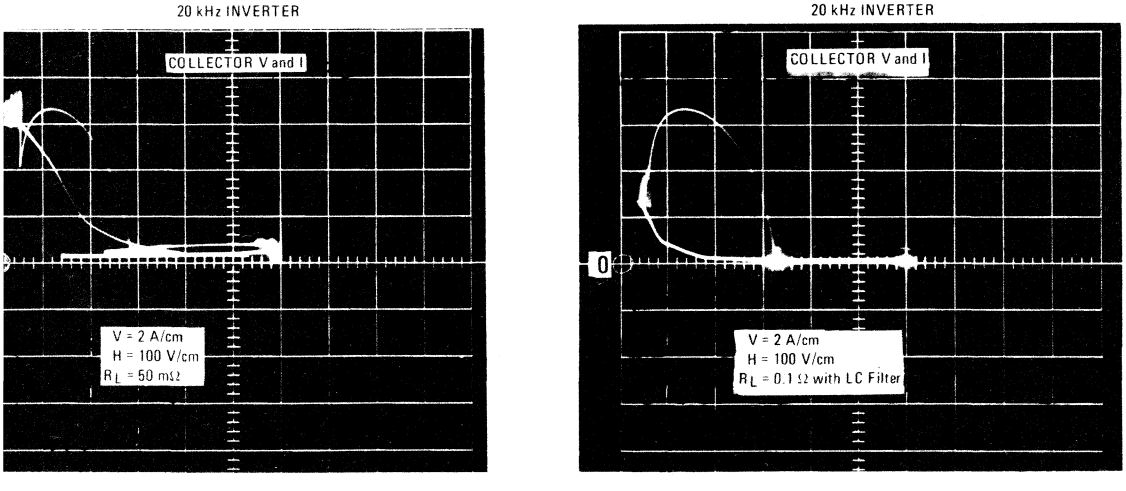


FIGURE 5 – 20 kHz Inverter Waveforms



(A) With 1 kW load (no filter)

(B) With 250 W load and LC filter

FIGURE 6 – Load Line of 2N6308

The crossover sense circuit senses the collector voltage of the output transistors and feeds a signal back to the comparator gates. Drive to one side of the inverter is inhibited by this stage until turn off of the opposite side has occurred. This feature was added primarily to eliminate the undesirable effects of the simultaneous on condition of the output devices normally attributed to the turn-off time being greater than the turn-on time. If both devices were permitted to be on at the same time, current spikes could cause SOA failure.

The transformer chosen to demonstrate the feasibility of this design was custom designed by the Pacific Instrument Corp. in Oakland, California. It's single output winding produces 10 V to the load (after rectification) from a 300 V line. This may not be the most optimum voltage in an actual design. The criteria involved in selecting the proper turns ratio are: low line, maximum duty cycle, and full load filter losses.

The transformer would normally be designed with three output windings in order to provide 5, 30 and 100 V through rectifiers and filters to the computer. In this design, the transformer has one low voltage center-tapped secondary winding to provide only the low voltage, high current output.

A pair of 30 V, 200 A barrier diodes are used to rectify the 20 kHz square wave. These multicell assemblies are used to maintain an excellent overall efficiency. Since barrier diodes are now available at 40 V, they could also be used in a bridge configuration to rectify the 30 V output. Conventional high voltage fast recovery rectifiers would be required for the 100 V supply.

CONCLUSIONS

The general circuit approach using high frequency power conversion techniques results in many advantages over the more conventional low frequency converters. In addition to this, many unique design features within this circuit tend to simplify the design and improve the reliability of the active components. The main features are as follows:

1) Small size and weight. The volume requirements for 60 Hz passive components such as filters and transformers has been reduced 10:1 by choosing an operating frequency of 20 kHz.

2) High efficiency, less cooling, The power transistors are operated in the switching mode and regulation can be achieved by using variable duty cycle techniques in the inverter or by phase control in the line pre-regulator. This practically eliminates the power dissipation problem in the voltage conversion and regulating sections. In addition, high efficiency barrier diodes are used as output rectifiers and reduce power dissipation in this section by 2:1 over conventional fast recovery rectifiers.

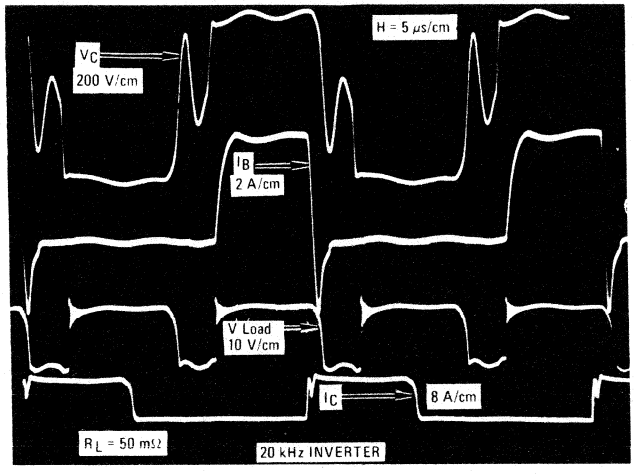
3) Circuit simplicity. The use of an MHTL flip flop and NAND gates eliminates the need for many discrete components. In addition, the use of power darlington transistors and a negative supply in the predriver simplifies what could be a very exotic switching circuit.

4) Reliable operation. The cross-over inhibit feature duces switching transients to a minimum without creat unnecessary dead time in the output waveform. This sures that the inverter transistors will stay within th safe operating area.

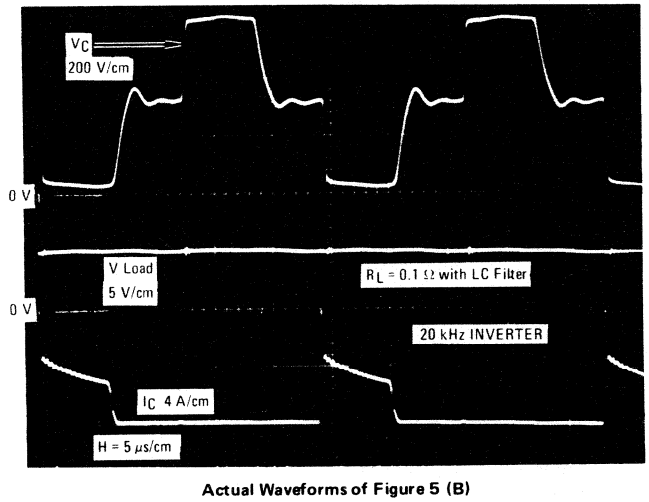
The inverter circuit described in this note proves t it is now feasible to build ultrasonic computer power s plies which can operate directly off a 208 V three ph AC line. Products that have just recently been introdu now make this supply practical. These include MHTL the control function, power darlington transistors drivers, high voltage power transistors for the inverter, a barrier diode assemblies for the output rectifier. T particular inverter could operate directly off a rectif three phase line at 300 V and pulse width control could added to regulate the output into an LC filter to compl the design. This inverter could also be used "as is" if a p regulator stage were added to control the output voltag

ACKNOWLEDGEMENTS

The author wishes to thank the following people f assistance in preparing this note. Ralph Greenberg, B Botos, Tom Mazur, Carl Dockendorf, and Larry Snyder.



Actual Waveforms of Figure 5 (A)
1 kW Load without filter
Note: I_C scope trace is out of sync



Actual Waveforms of Figure 5 (B)
250 W Load with LC filter
Note: I_B same as above

AN-719
Application Note

A NEW APPROACH TO SWITCHING REGULATORS

Prepared by:
R. J. Haver
Senior Industrial Applications Engineer

This article describes a 24-Volt, 3-Ampere switching mode supply. It operates at 20 kHz from a 120 Vac line with an overall efficiency of 70%. New techniques are used to shape the load line. The control portion uses a quad comparator and an opto coupler and features short circuit protection.

MOTOROLA *Semiconductor Products Inc.*

A NEW APPROACH TO SWITCHING REGULATORS

INTRODUCTION

The function of a switching regulator is to convert an unregulated dc input to a regulated dc output. The method used to accomplish this function differs dramatically from the conventional series pass regulators. In a switching regulator, the power transistor is used in a switching mode rather than a linear mode. Efficiencies are usually 70% or better which is about double that of the series pass regulator. High-frequency switching regulators offer considerable weight and size reductions and better efficiency at high power over conventional 60 Hz transformer-coupled, series regulated power supplies.

However, a debate continues on the value of switching type supplies as contrasted with conventional series pass regulators. One argument, frequently advanced when discussing switching regulators, is that the electro-magnetic interference (EMI) problems overcome most of the gains in efficiency. Eliminating high-frequency transients, not present in the linear case, adds a new dimension to the design of switching regulators. Controlling this undesired output actually requires very little bulk weight. Basically the necessary techniques come from good RF practice. Layout and lead length play significant roles when designing effective switching circuits.

EMI can be reduced to acceptable levels giving compact, fast and efficient control of power. Switching regulators have found wide use in aerospace and portable applications where power is expensive. Low loss ferrite cores for transformers and chokes, the use of high permeability magnetic alloys for shielding, and the wide range of miniature semiconductor and IC devices for the switching and regulation circuitry have contributed to the success of switching type supplies. The block diagram of a switching regulator is shown in Figure 1. This circuit regulates by switching the series transistor to either the ON or OFF condition, the duty cycle determining the average dc output. Duty cycle is adjusted in accordance with a feedback proportional to the difference between the dc output and a reference voltage.

Switching is usually a constant frequency just above the audible range (20 kHz typical), although some varieties show variable frequency with changing line and load. Higher frequencies are generally less efficient since transistor switching losses and ferrite core losses increase. Low frequency unibase transistors (F_T-200 kHz) are sufficient for series pass regulators; switching regulators must use epibase and triple diffused devices (F_T-4 MHz) to operate efficiently. For the ultimate in efficiency, even higher frequency annular and double diffused devices can be used, ($F_T > 30$ MHz). Darlington transistors are also used in these switching mode supplies; they can provide an overall gain in efficiency through lower base drive requirements even though their saturation voltages are higher than single chip devices.

A fast recovery rectifier or Schottky barrier diode is used as the free wheeling clamp diode to keep the switching transistor load line within SOA limits and to increase efficiency at these frequencies. Other products used in these supplies are shown in Table 1 below.

TABLE 1
Semiconductors Used in Switching Regulators

	CONTROL IC's	
POWER DEVICES	DIGITAL	LINEAR
Power Transistors	Gates Flip-Flops	Op Amps Comparators
Rectifiers	Monostable Multivibrator	Timers Regulators

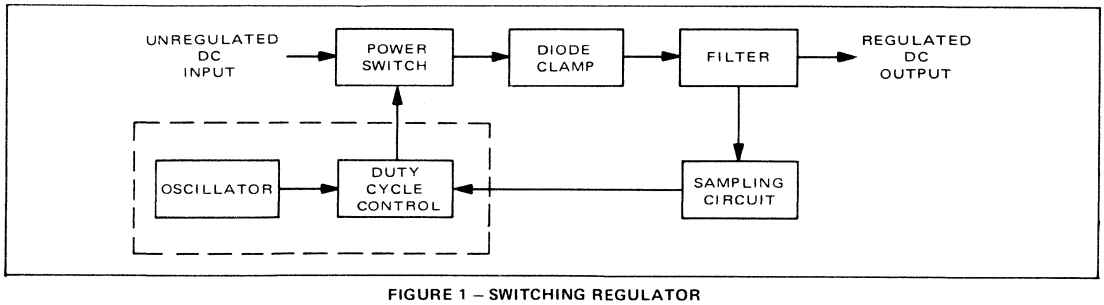


FIGURE 1 – SWITCHING REGULATOR

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

TYPICAL CIRCUITS

Various circuit configurations have been used in switching regulator designs. All have the following common elements:

1. Switching transistor
2. Clamp diode
3. LC filter
4. Logic or control block.

Representative circuits are shown in Figure 2. It should be noted that none of these circuits offers isolation between the line and load. (However, the one transistor design highlights simplicity and economy.) It is usually desirable to have at least one line in common with the input and output to reduce ground loops. The one line approach also determines whether the output voltage will be considered positive or negative. However, by definition this is academic since most circuits will operate from either supply since the input and output grounds are usually isolated. This is suitable for the most general use of switching regulators which power industrial controls and other logic circuits. In circuits 2(a) and 2(b) the logic operates from the load voltage. These circuits are not self-starting and provisions must be made to operate from the line during starting and short circuits. In circuits (c) and (d) the logic operates continuously from the line and is isolated from the load. The sense and feedback elements must be electrically isolated for this reason. An opto coupler or an equivalent device is ideal for this purpose.

Circuits (b) and (d) are generally used in line operated supplies because economical high voltage NPN transistors are available whereas PNP types are not. Of these two, circuit (d) is the most popular because the logic is tied directly to the series switch, and switching can be much more efficient.

Driver transformers are also used in many designs to interface between the logic and switching transistor. In such a case, there are no circuit constraints on the transistor type, and it may be an NPN or PNP device.

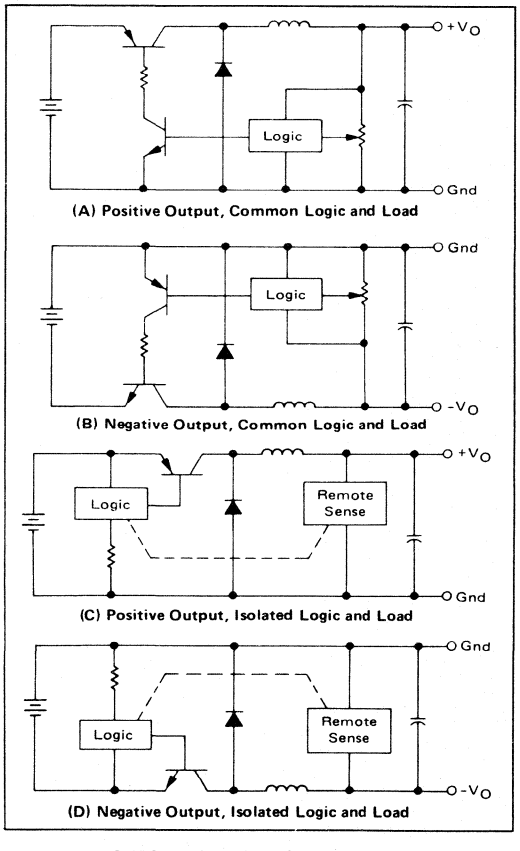


FIGURE 2 – SWITCHING REGULATOR CIRCUIT VARIATIONS

THEORY OF OPERATION

The high efficiency of switching regulators is a result of operating the series transistor in a switching mode. When the transistor is switched ON, full input voltage is applied to the LC filter; when it is OFF, the input voltage is zero. With the transistor turned on and off for equal amounts of time (50% duty cycle), the dc load voltage will be half the input voltage. The output voltage (V_O) will always equal the input voltage (V_{in}) times the duty cycle (D) as follows:

$$V_O = D\,V_{in}$$

Varying the duty cycle will therefore compensate for changes in the input voltage; this technique is used to obtain a regulated output voltage.

Repetitive operation of the switching transistors at a fixed duty cycle produces the steady state waveforms shown in Figure 3. With the switch closed, inductor current (I_L) flows from the input voltage (V_{in}) to the load. The difference between the input and output voltage (V_{in}-V_O) is applied across the inductor. This causes I_L to increase during this time.

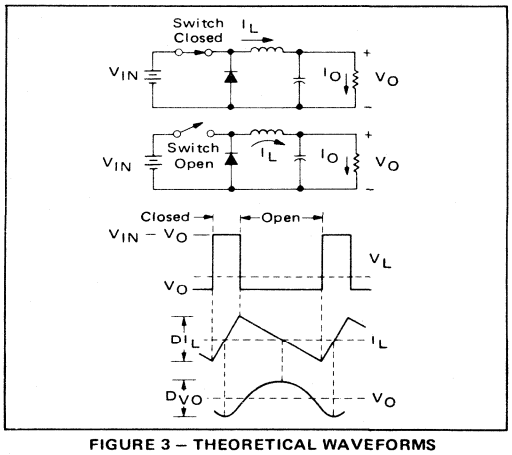


FIGURE 3 – THEORETICAL WAVEFORMS

With the switch open, stored energy in the inductor forces IL to continue to flow to the load and return through the free wheeling diode. The inductor voltage is now reversed and is approximately equal to V_O. During this time, IL decreases.

The average current through the inductor equals the load current. Since the capacitor keeps V_O constant, the load current (I_O) will also be constant. When IL increases above I_O, the capacitor will change and when IL drops below I_O, the capacitor will discharge. These waveform inflection points are indicated in Figure 3. The end results of steady state operation are as follows:

1. The average inductor voltage will be zero but a wide variation from (V_{in}-V_O) to V_O will be experienced.
2. The dc current flowing through the inductor will equal the load current. A small amount of sawtooth ripple will also be present.
3. The dc voltage on the capacitor is equal to the load voltage. A small amount of ripple (quasi-sine wave) will also be present here.

Transient operation must consider changes in V_{in} and I_O. Input voltage changes are automatically compensated for by appropriate duty cycle variations in a closed loop system. Input regulation and ripple rejection are dependent on loop gain but are generally adequate as indicated later.

Changes in I_O are more difficult to compensate for and load transient response is generally poor. Changes in I_O are compensated for with temporary duty cycle changes. For example, a change in load from half to full will result in the following:

1. Duty cycle increases to its maximum (the transistor may just stay ON).
2. The inductor current takes many cycles to increase to its new dc level.
3. Duty cycle returns to its original value.

DESIGN

The circuit in this article was designed to supply a regulated 24 Vdc output from a 120 Vac line. Typical load variations are from 1.5 to 3 Amperes and the line from 100 to 140 Vac. In addition to providing good regulation, the circuit is efficient and has short circuit protection. The design of this regulator utilized the functional blocks shown in Figure 4. Since it is line operated, an input rectifier and filter are required to convert the incoming ac to dc. The power switch uses a high voltage transistor operating at a switching frequency of 20 kHz to control the pulse width of the voltage applied to the LC output filter.

The control portion of this design uses an oscillator, a "one shot" comparator, and a feedback block which also includes an opto coupler. The oscillator generates the fixed frequency of operation. The resulting output forms a clock pulse for the comparator. The second input to the comparator is derived from the feedback amplifier. This amplifier senses the output voltage and controls the duty cycle of the "one shot" comparator. The output of the comparator is then fed directly to the power switch to complete the loop. Additional details regarding the design and operation of these blocks are provided in the following sections.

INPUT RECTIFIER AND FILTER

The input rectifier and filter consists of a bridge rectifier and filter capacitor. To improve the efficiency series limiting resistance is not specifically used; starting current surges are higher because of this and a 12 Ampere rectifier is therefore required even though the average output current is less than one Ampere. A 150 μF capacitor was used to limit the input ripple to under 20 V peak-to-peak with a full load.

OUTPUT FILTER

The output filter is also quite simple as shown in Figure 5. Calculations of the values for L and C are more involved but quite conventional. The appropriate design information is also shown in Figure 5. To design the filter

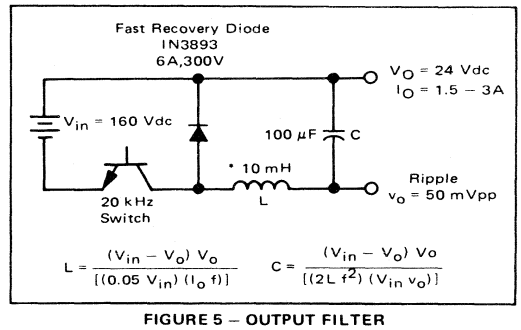


FIGURE 5 – OUTPUT FILTER AND DESIGN SPECIFICATIONS

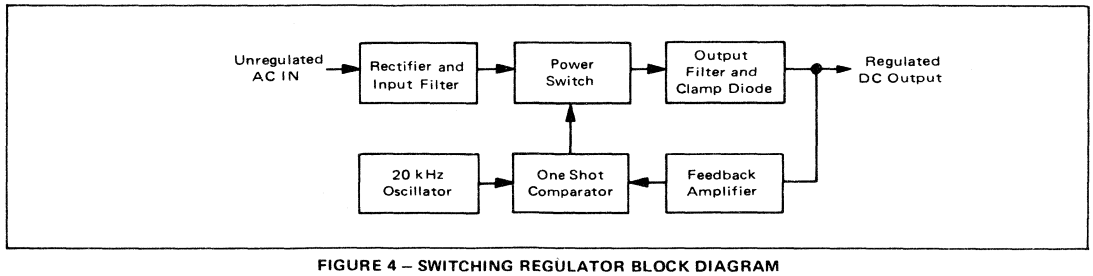


FIGURE 4 – SWITCHING REGULATOR BLOCK DIAGRAM

approximate values for the following must be known.

1. Input voltage, V_{in}
2. Output voltage, V_O
3. Frequency, f
4. Output current, I_O (and range)
5. Output ripple v_O (peak-to-peak)

A general "rule of thumb" is to restrict current variations in the choke (L) to 10% of the load current. Variations are restricted to 5% in this case since a regulation range of load current of at least a 2 to 1 ratio is required. Smaller values of inductance could be used to improve transient response as long as the choke does not run dry (allowing choke current to drop to zero during each alternation). A value for L can be found using:(1)

$$L = \frac{(V_{in} - V_O)\,V_O}{0.05\,I_O\,V_{in}\,f} \text{ (for } \Delta I_L = 5\%\, I_O)$$

$$L = \frac{(160 - 24)\,24}{0.05\,(3)\,160\,(20\text{ k})} = 6.8 \text{ mH}.$$

The nearest standard choke available in this design case was a 10 mH air core choke. A standard Triad C 58U or an equivalent custom designed ferrite core may be used if a small air gap is provided in the latter case to prevent saturation at currents up to 5 Amperes dc; this is the short circuit limit.

To keep v_O below 50 mV, a value for C can be found using:(1)

$$C = \frac{(V_{in} - V_O)\,V_O}{(2L)\,f^2\,V_{in}\,(v_O)},$$

$$C = \frac{(160 - 24)\,24}{2\,(10\text{ mH})\,(20\text{ kHz})^2\,160\,(50\text{ mV})} = 51\ \mu\text{F}.$$

The dissipation factor of most electrolytic capacitors is too high for this application; because of this, two 50 μF capacitors were used to obtain the desired performance. A more expensive stacked foil electrolytic or solid tantulum capacitor may also be used. High frequency bypass capacitors and an additional high frequency LC filter are used in similar designs to prevent switching spikes from reaching the load. This approach was not required in this design because the load line shaping which will be described later Operation at 20 kHz requires a fast recovery diode. A 6 Ampere, 300 Volt, 1N3893 was chosen to handle up to 5 Ampere free-wheeling currents and peak line voltage.

POWER SWITCH

The power switch includes a push-pull driver which provides the interface between the integrated circuit drive signal and the actual power switch, a high voltage NPN power transistor. Power to this stage and the logic is provided by a 12 Volt step-down transformer. The IC logic is in the position indicated earlier in the discussion of Figure 2(d). The main advantage of this layout is that the logic ground is common to the emitter of the power switch. Because of this, conventional speed-up capacitors can be used to couple the drive signal to the base terminal to improve switching speeds. This is especially important in this particular design. Because of the large step-down in voltage and the high switching frequency, ON times will be very short. The minimum switching time is found using the peak V_{in} of 200 V (high line) instead of 160 V.

The earlier discussion of switching regulator theory indicated the duty cycle would be approximately:

$$D = V_O/V_{in} = 24/200 = 12\%.$$

At 20 kHz, the ON-time will be 12% of 50 microseconds or approximately 6 μsec. With simple resistive termination of the base emitter junction, storage time alone can be as much as 10 μsec. For this reason, a special drive circuit and a high frequency 250 volt, 8 Ampere, 2N6306 power transistor were required for this application. This device has good saturation voltages at 3 Amperes with excellent switching speeds. The drive circuit shown in Figure 6 does the job of switching the 2N6306 at 3 Amperes and 20 kHz from the 120 Vac line. To do this, two unique design innovations were used.

1. An artificial negative bias supply was created from the single positive supply available to improve fall time.
2. Current limiting was added to the base current to limit overdrive and reduce storage time.

Turn-off of the power switch is accomplished by forcing the IC to a logic low. This turns on the 2N6034 and creates a path for reverse base current. The 10 μF capacitor which is used as a reverse bias supply then removes stored base charge from the 2N6306 and forces it to turn-off. Reverse base current flows for about 2 μsec. The diodes are added to prevent the capacitor from discharging into the 10 ohm resistor once the base is

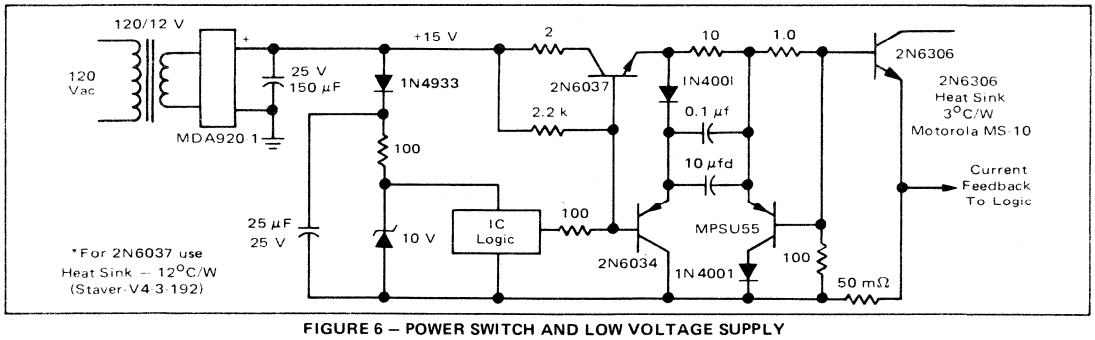
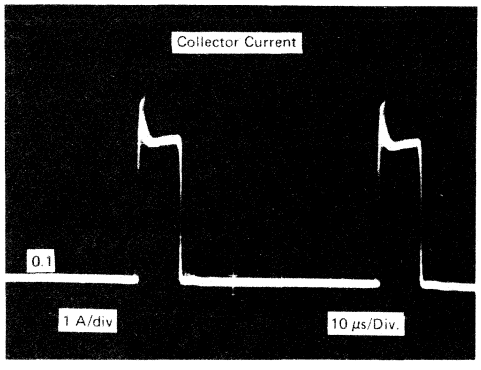


FIGURE 6 – POWER SWITCH AND LOW VOLTAGE SUPPLY

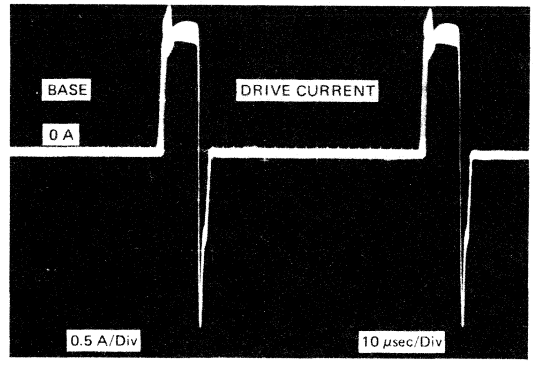
cleared. This minimizes the amount of charge that must be replaced during each alternation.

When the logic goes high, the 2N6037 turns on and forward base current flows through the 10 ohm resistor turning on the 2N6306. The 2N6034 and 2N6037 are both plastic Darlington power transistors. However, the 2N6037 should be used with an appropriate heat sink since it supplies both forward base drive for the device and recharge current for the 10 μF capacitor. With this high gain Darlington, recharge takes approximately 2 μsec. Most of the recharge current is bypassed around the 2N6306 base by the MPSU55; this device limits forward base drive to about 1 Ampere. This particular drive level was chosen to keep storage time low and at the same time ensures that the 2N6306 will remain saturated even under short circuit conditions. The actual operation waveforms of the power switch and drive circuit are shown in Figures 7 and 8, respectively.

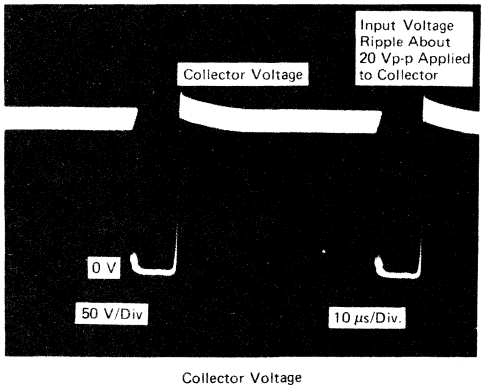


Collector Output Current

Both Measured
With 120 Vrms Input
and Output
24 V 3 A



Measured
With 120 Vrms Input
and Output
24 V 3 A



Collector Voltage

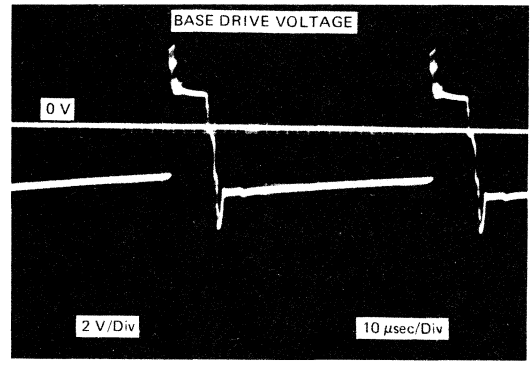


FIGURE 7 – POWER SWITCH WAVEFORMS

FIGURE 8 – DRIVE CIRCUIT WAVEFORMS

FEEDBACK AMPLIFIER

Because the load ground and logic ground are isolated, it is necessary to use a 4N28 opto coupler for the feedback amplifier. The schematic is shown in Figure 9. The 1N5290 is a 0.5 mA current limiting diode and causes the voltage drop across the 39 k sense resistor to remain fixed at about 20 V. This unique design causes changes in load voltage to appear directly at the base of the 2N5088 and results in sensing without attenuation. Load voltage changes produce a linear change in LED current and a proportional voltage change at the sense terminal of the logic circuitry.

The 0.5 mA diode is considered to be a zero temperature coefficient unit. Also, the output level of the opto coupler of 1 mA is chosen to minimize its temperature dependence. A photo Darlington coupler was tried for increased gain; however, it introduced low frequency oscillations because of its slow speed and thus, could not be used.

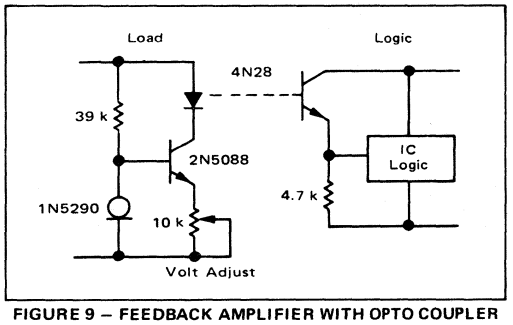


FIGURE 9 – FEEDBACK AMPLIFIER WITH OPTO COUPLER

OSCILLATOR, COMPARATOR, AND CURRENT LIMIT CIRCUITS

In addition to the feedback amplifier, the control circuit for this switching regulator also requires an oscillator, comparator, and current limiter as part of its control circuitry. These last three functions are all made possible by the use of a single IC chip, the MC3302 quad comparator.

The schematic diagram of the oscillator, comparator, and current limit circuits is shown in Figure 10. Comparator 1 is used as a 20 kHz oscillator. It supplies a sawtooth output which operates between the voltage limits defined by the 100 k positive feedback resistor and the logic supply voltage. The second comparator takes this output and compares it to the feedback signal to produce a variable duty cycle output pulse for the power switch. The timing diagram in Figure 11 illustrates how this happens. In normal operation, the feedback signal is a constant dc voltage which is between the limits of the oscillator sawtooth. When the sawtooth exceeds the feedback threshold, comparator 2 switches to a high output level. The comparator is reset when the sawtooth drops back below the feedback signal. In actual practice, the comparator output pulse is delayed by 2 μsec because of internal propagation time. This phase shift has no effect upon regulation. Variations in the output and feedback signals will still produce compensated changes in the power switch pulse width.

The remaining two comparators in Figure 10 are used to initiate current limiting action. Comparator 3 senses the over current and triggers comparator 4 which is used as a "one shot" multivibrator. The zero input voltage threshold is derived from the reference voltage of 0.24 V from comparator 3. Power dissipation in the 50 mΩ sense resistor is therefore kept at a minimum. With this combination of reference voltage and current resistor,

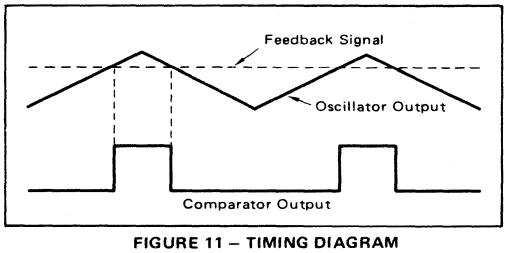


FIGURE 11 – TIMING DIAGRAM

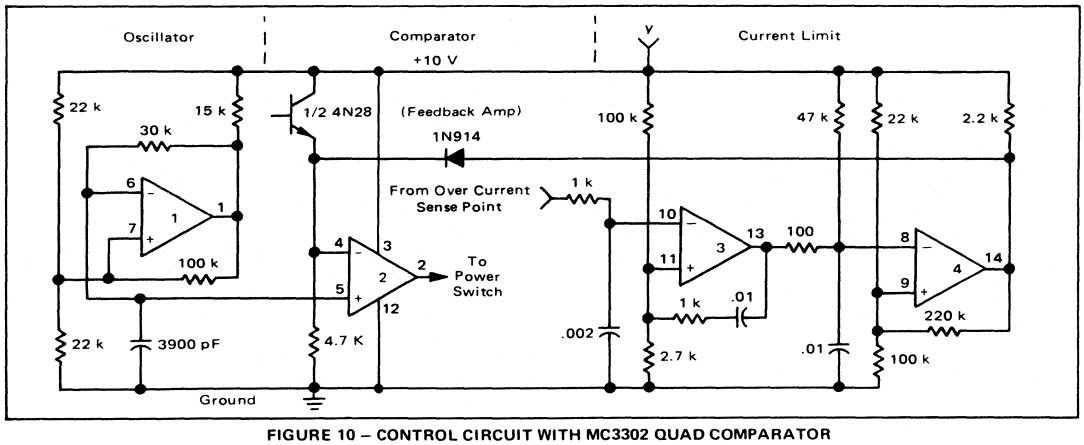


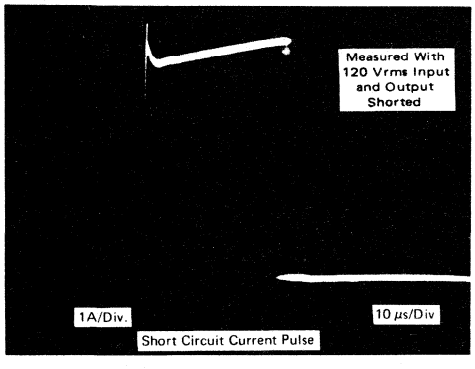
FIGURE 10 – CONTROL CIRCUIT WITH MC3302 QUAD COMPARATOR

current limiting occurs at approximately 4 Amperes. When this level is reached (due to overload or short circuit), the "one shot" capacitor is discharged and a millisecond time interval is initiated. Positive ac feedback is used to ensure that this capacitor does completely reset. An RC filter is also provided to prevent inductive transients from accidentally shutting the regulator down.

While the "one shot" device is recharging, the output of comparator 4 remains high to simulate excessive output voltage at this feedback sense point (comparator 2); drive pulses are completely inhibited during this down time. Comparator 4 is reset and drive pulses continue when the "one shot" device reaches an 8 volt threshold. Positive feedback to this reference prevents circuit oscillations as the threshold is approached. If the short is removed, the switching regulator will automatically reset into a full load. If the short remains, operation (with 30 μs4 Ampere pulse) continues at an audible 1 kHz rate set by the "one shot" multivibrator. The short circuit collector currents are shown in Figure 12.

LOAD LINE SHAPING

Load line shaping can be used to improve reliability and reduce EMI.[1][2] Shaping is basically done by using reactive elements to absorb what would normally be switching losses. Because resistors are used to dissipate the power stored in these reactive elements, there is no appreciable improvement in overall circuit efficiency. However, because safe operating area (SOA) stresses on the switching transistor are reduced, cooler and more reliable operation results. Illustrations of the load line before and after are shown in Figure 13 and 14. A secondary but very desirable effect can also be noticed at the output. Switching spikes, due to the abrupt recovery of the fast recovery diode and fast switching speed of the power transistors, are reduced from a 0.6 Volt to a 0.1 Volt peak. Because



Short Circuit Current
Measured at the Collector
with Current Probe

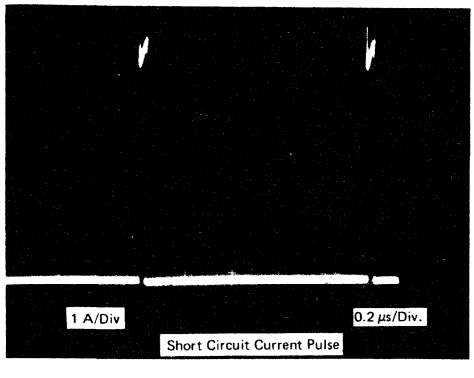
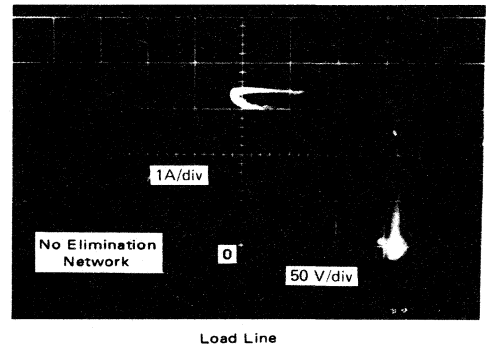


FIGURE 12 – SHORT CIRCUIT CURRENTS



Load Line

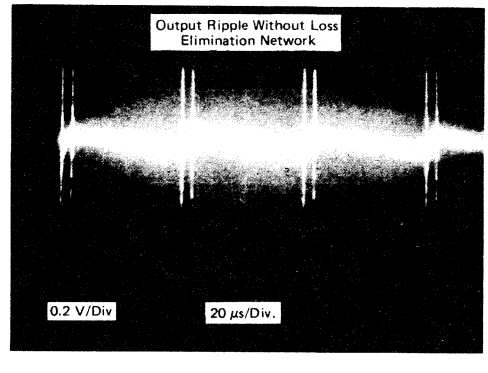


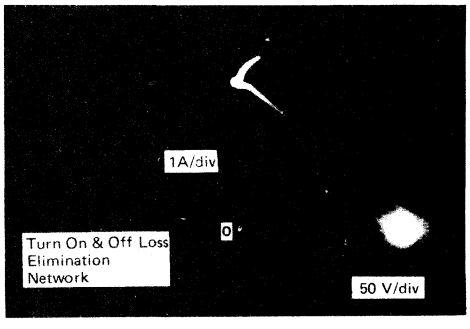
FIGURE 13 – BEFORE LOAD LINE SHAPING

these spikes are reduced to acceptable levels, additional high frequency output filters are not required. Calculations of the power losses reveal the following:

TABLE 2 – Comparison of Power Losses

POWER LOSS	BEFORE	AFTER
During turn-on	2.4 W	0.8 W
During turn-off	3.0 W	1.0 W
Total	5.4 W	1.8 W

The calculations show the dramatic improvement. The remaining power loss of approximately 0.4 watt, due to base and collector saturation voltages of 1.0 and 0.5 Volt respectively, is unaffected by these changes.



Load Line

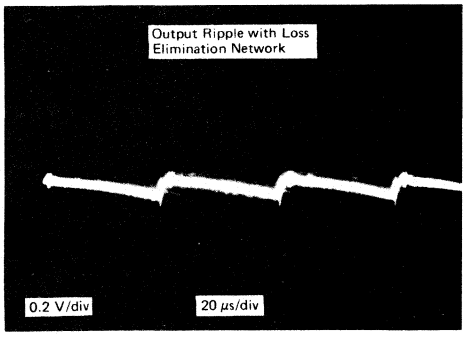


FIGURE 14 – AFTER LOAD LINE SHAPING

The actual loss elimination networks used in this design are shown in Figure 15 along with the design equations. During turn-on the inductor (L_X) must delay the input voltage (V_{in}) during the transistor turn-on time (t_r). Load current (I_O) will decrease to zero since it has been flowing in the free-wheeling diode and inductor prior to this time. Measured current rise and fall times on the transistor are 0.3 and 4 μsec respectively. Therefore:

$$L_X = \frac{V_{in}\, t_r}{I_O} = \frac{160\ (0.3\ \mu sec)}{3} = 16\ \mu H.$$

The value used was 20 μH. The inductor should not saturate at rated load to be effective and current must build back up to I_O during the free-wheeling time of 40 μsec. The resulting inductance/resistance (L/R) time constant of 4 μsec ensures this condition. Therefore:

$$R1 = 1/\gamma = 20/4 = 5\ \Omega$$

Using a 4.7 ohm resistor was practical since the collector voltage overshoot was limited to approximately 15 V.

During turn-off, the capacitor (C_X) must supply load current (I_O) while the transistor is turning OFF (t_f). The capacitor will have charged to the input voltage and will now discharge to zero. Therefore:

$$C_X = \frac{I_O\, t_f}{V_{in}} = \frac{3\ (0.4\ \mu sec)}{160} = 7500\ pF.$$

Because of parasitic circuit capacitance, only 7400 pF is required. The capacitor must recharge during the on-time of the transistor to 10 μsec. The RF time constant of 1.0 μsec is chosen to ensure this condition. Therefore:

$$R_C = \tau/C = 1\ \mu sec/4700\ pF = 210\ \Omega.$$

Using a 150 ohm resistor is practical because the collector current overshoot is limited to approximately 1 Ampere. Thus, parasitic capacitance has no effect on this recharge time. In actual practice, the values of L_X and C_X may be empirically adjusted to obtain the desired load line effect.

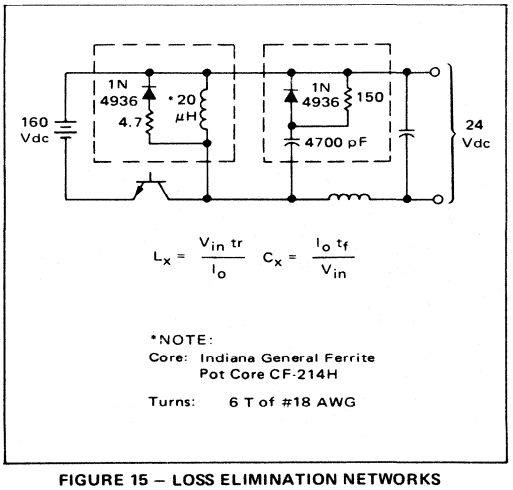


FIGURE 15 – LOSS ELIMINATION NETWORKS

CONCLUSION

This article has discussed the circuitry used to implement a line operated switching regulator as shown in Figure 16. The semiconductor components highlighted in this design include:

1. A 2N6306 power transistor. This device switches 3 Amperes from 200 Volt and is fast enough to handle the 20 kHz square waves generated by the design.
2. The 2N6034 and 2N6037 complementary power Darlingtons. These devices switch up to 3 Amperes and provide a single stage interface between the IC logic and the 2N6306.
3. An 4N28 opto coupler. This device provides an electrically isolated feedback signal from the load to the IC logic. It is fast enough to operate in a 20 kHz switching frequency loop.
4. The MC3302P quad comparator. The comparator itself provides all the logic functions necessary for voltage regulation and current limiting in a single package.

Several unique design innovations have been presented. The most significant design highlight is reactive load line shaping. By using techniques from a Bell Laboratories report,(1)(2) switching power losses are reduced by a factor of 3. The same reactive components are also responsible for a 6 to 1 reduction in output noise.

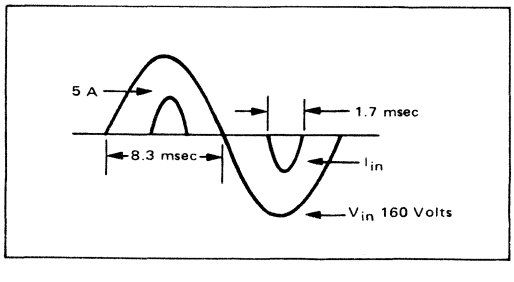
The ripple content of the output voltage (24 Volts dc) is shown in Figure 17. The 60 Hertz ripple frequency has been reduced significantly by a factor of 100 to yield a 200 mV peak-to-peak maximum ripple component. The ripple factor is approximately 10 mV per volt. The 20 kHz output ripple is only 50 mV peak-to-peak; this is less than 0.2% of the output voltage.

The output voltage variations due to line and load changes are as follows:

TABLE 3 – Line versus Load Variation Comparisons

Regulation	Conditions	ΔV_O	Percent Regulation
Load	I_O = 1.5 to 3 Ampere V_{in} = 120 Volts ac	0.2 V	0.8%
Line	V_{in} = 100 to 140 Volts ac I_O = 3 Amperes	0.7 V	3%

The efficiency is measured at rated load (24 Volts, 3 Amperes) with 120 Volt input. The oscilloscope display of input voltage and current is shown below:



The input voltage varied from 150 to 170 Volts during the power pulse but is considered constant at 160 Volts. The current pulse is essentially a sine wave. This allows the use of a peak-to-peak comparison on an average ratio of 2/k in calculating the total average current and input power as shown:

$$P_{in} = E_p \quad \frac{2}{\pi} I_p \quad \frac{\text{Pulse Width}}{\text{Period}}$$

$$= (160\text{ V}) \frac{2}{\pi} \quad (5\text{ A}) \quad \frac{1.7\text{ ms}}{8.3\text{ ms}} \quad = 103\text{ watts.}$$

The overall efficiency can then be found using:

$$\text{Efficiency (\%)} = \frac{P_O}{P_{in}} \; 100$$

$$= \frac{(24\text{ V})(3\text{ A})}{103} \; 100 = 70\%$$

As was indicated earlier, this is about twice that of a series-pass regulator.

This particular line operated switching regulator has many advantages over a conventional series-pass design; since the efficiency is high, less heat sinking is required. Because the switching regulator operates directly from the line, the need for a 60 Hertz transformer is eliminated. The size and weight reductions are therefore quite significant and are becoming increasingly important in many applications. The main drawback of most uncompensated switching regulators is noise. This drawback can be eliminated by using load line shaping. Load line shaping only reduces the high frequency electrical noise associated with switching mode supplies but also improves the reliability of the power stage. An opto coupler is used in the 20 kHz feedback loop to maintain a high degree of line and load isolation. A single package quad comparator is used to reduce component quantity for both pulse width control and short circuit protection.

This article has demonstrated a significant method of designing a regulated switching supply with 70% overall efficiency. The approach describes and illustrates how to decrease component counts and avoid using costly, cumbersome and inefficient transformer-operated industrial power supplies, while providing complete short circuit protection.

The author wishes to acknowledge Paul Fletcher for his assistance in preparing this note.

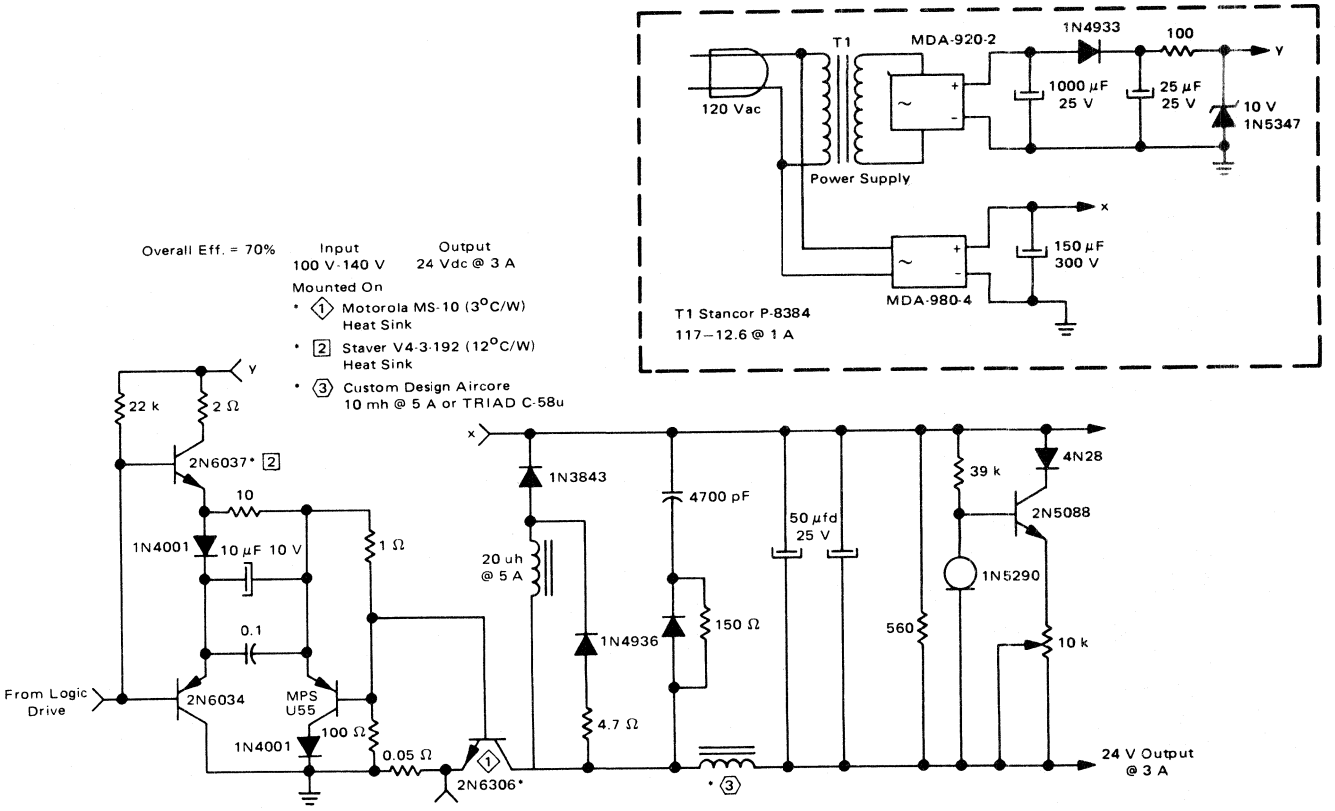
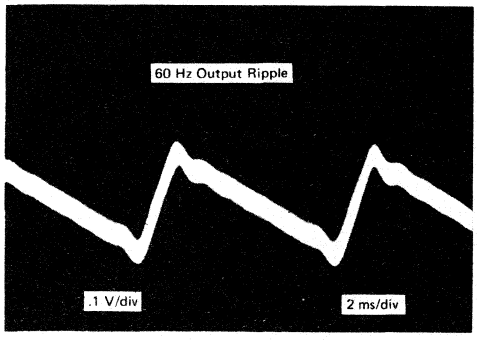


FIGURE 16 – Complete Regulator Schematic (for logic see Figure 10)



NOTE:
Both Measured
With 120 Vrms Input
and Output Ripple with Attendant
20 kHz ripple 24 V at 3 A

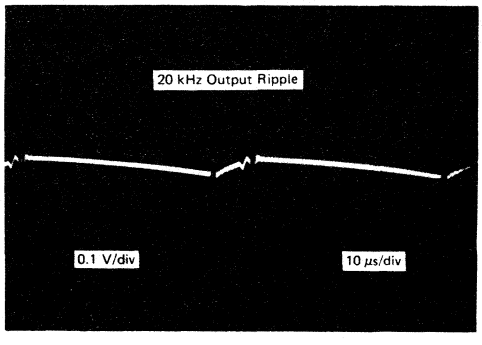


FIGURE 17 – OUTPUT RIPPLE WAVEFORMS

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AN-737A
Application Note

SWITCHED MODE POWER SUPPLIES-HIGHLIGHTING A 5-V, 40-A INVERTER DESIGN

Prepared by:
R. J. Haver
Applications Engineering

This application note identifies the features of various regulator circuits that are in use today in AC to DC power supplies. The note also illustrates how these circuits may be used as complementary building blocks in a system design. Primary emphasis is on switched mode regulators because they fill the present need for energy and space savings.

A complete 5-V, 40-A line operated inverter supply is described in detail including design procedures for the magnetic components. The inverter itself is a "state-of-the-art" design which features CMOS logic, high voltage power transistors, Schottky rectifiers and an optoelectronic coupler. It operates with a full load efficiency of 80% at a frequency of 20 kHz.

MOTOROLA Semiconductor Products Inc.

SWITCHED MODE POWER SUPPLIES - HIGHLIGHTING A A 5-V, 40-A INVERTER DESIGN

ITRODUCTION

There are many ways to build a power supply. The near or "series pass" supply is one that has dominated ie market for a long time. A more recent entry, the vitched mode power supply, however, is coming of age. has already replaced the linear regulator in many applications where high efficiency and small size are important considerations. In other cases, it is used in combination with linear regulators to obtain excellent regulaon and transient response with improved efficiencies. ecause the switched mode supply is now a proven design oncept, it is being considered for use in most new degns and has become a very popular topic of conversation mong design engineers.

In the first part of this article, the salient features of ll types of dc power supplies are identified. A brief utline of several system approaches illustrating the most opular combinations of these circuits is presented. In ie second part, the basic switched mode circuits are lentified and a design example is presented. The example eatures a 120 V line operated 200 W inverter with a egulated output capable of supplying 40 A at 5 V.

inear versus Switched Mode Supplies

Several voltage regulator circuits are available to the ower supply designer. The most popular circuits in use oday include:

1. Controlled Ferroresonant Transformer
2. SCR Phase Control
3. Linear Regulators
   a. Series
   b. Shunt
4. Switched Mode Regulators
   a. Switching Regulators
   b. Pulse Width Modulated (PWM) Inverters

In this article, switching regulators refer to one-transistor circuits whereas an inverter is considered to contain two transistors operating in a push-pull mode. The significant features of all these circuits are shown in Figure 1. In general, the table reflects typical size, cost, and performance data as found in current literature (magazines, technical brochures, etc.) Because the first three circuits all use bulky 60 Hz transformers for isolation between the line and load, they suffer the common disadvantage of large size. The switched mode regulators, however, operate above audio frequencies and use small 20 kHz power transformers. Because of the present emphasis on energy conservation, efficiency, and small size, the future appears bright for these switching supplies. The ferroresonant and SCR supplies are also making progress on the linear market, they are more efficient, and economical as well. The reason none of these supplies will completely replace the series regulator is also evident. The series regulator still offers the best regulation, ripple rejection, and transient response.

As shown in Figure 2, at the 100 W level, switching supplies cost more to build than series pass supplies. However, as was indicated earlier, they are still used at this power level and lower, when size is more important than cost. If we were to look at the characteristics of larger supplies, we would find that the performance data in Figure 1 remains basically the same. The size and weight numbers would tend to increase proportionally but the cost per watt has a tendency to decrease. Figure 2 offers a specific comparison between inverters and series pass regulators on this. The parts cost covers only the electronic components and heat sinks. Total parts cost is about $1/Watt at this level. Because inverter costs drop faster, they are more economical than series pass regulators at high power levels and cost about the same at the 200 to 300 W level. A couple of years ago, this break-even point was at the 500 W level.

Another advantage of transistor Switched Mode supplies is hold-up time which is better by an order of magnitude

Features	Ferroresonant	SCR	Series	Switching Regulator	Inverter
Major Advantage	Low Cost	Low Cost	Excellent Regulation	Small	Small
Major Disadvantage	Large	Poor Response	Poor Efficiency	Poor Response	Poor Response
*Cost (Electrical Parts)	$15	$15	$20	$25	$30
*Efficiency	80%	80%	30%	70%	70%
*Size (cu. in.)	600	200	300	70	70
*Weight (lbs.)	30	10	20	5	5
Regulation	3%	5%	0.1%	0.1	0.1
Ripple	160 mV	100 mV	5 mV	50 mV	50 mV
Maximum Power	2 kW	None	1 kW	200 W	1 kW
Transient Response	100 ms	100 ms	50 μs	1 ms	500 μs

*Note: These numbers apply to a 100 W supply.

FIGURE 1 – Comparative Features of DC Power Supplies in 1974

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

(20 ms versus 2 ms) due to high voltage energy storage. However, these supplies are more complex and generate more noise. Noise generation is roughly 10 times that of a series pass supply and since more sophisticated control circuitry is required, switches are also more difficult to design.

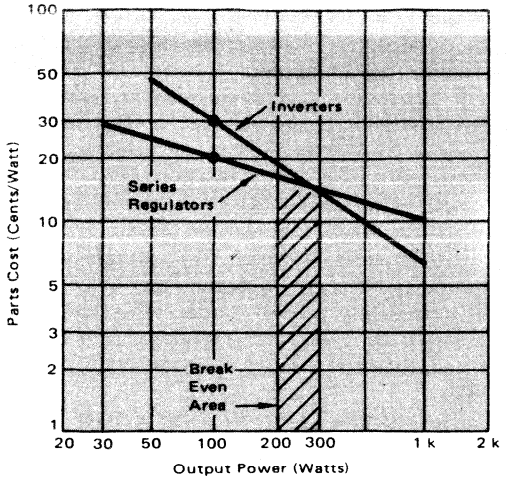


FIGURE 2 – Why Use Switching Supplies?

System Approaches

Now that the features and capabilities of various regulators have been reviewed, it is easier to understand the problem a designer faces in choosing which circuit or combination of circuits to use. The source of power is specified and would not be one of these design problems. When output power is 500 W or less, the single phase 120 V line is generally used. For larger supplies, three-phase power from a 208 V or 220 V source is used because energy storage in filter capacitors is more economical at these higher voltages. Tolerances on line voltage are typically +10% and -30%. Operation beyond these points can be prevented by voltage crowbars and shutdown circuits.

Before reviewing the popular circuit combination, it's well to consider the problem of power distribution. In a large system, such as a medium size TTL computer, up to 4 kW of power may be required at the 5 V level. This power capability may be designed into a large, centrally located supply or distributed in several smaller supplies at the "point of load". In the central supply, large bus bars are used to distribute the low-voltage, high-current power to the various bays and racks within the main frame. Distributed or "point of load" supplies may operate from the ac line or from a high voltage dc bus and supply from 50 to 250 Watts of power. There appears to be a general trend away from the single central supply to smaller distributed supplies at the 200 to 250 W level like the circuit shown in this note. Where a central supply is retained, it is used as a preregulator to power the high voltage bus. A ferroresonant supply is popular here because it also eliminates line transients. Of course, there are still many applications where all the power is for one load and it cannot be split up. In these cases, a single large regulated supply may be used or several small "current limited" supplies may be paralleled to make up the power.

Several possible system approaches to the design of a computer or industrial power supply are shown in Figure 3.[1] In each case there may be a requirement for multiple output voltages. The computer will use 5 V for the logic and 36 V, 48 V, and 100 V supplies for memories, read-

[1] See also reference #4

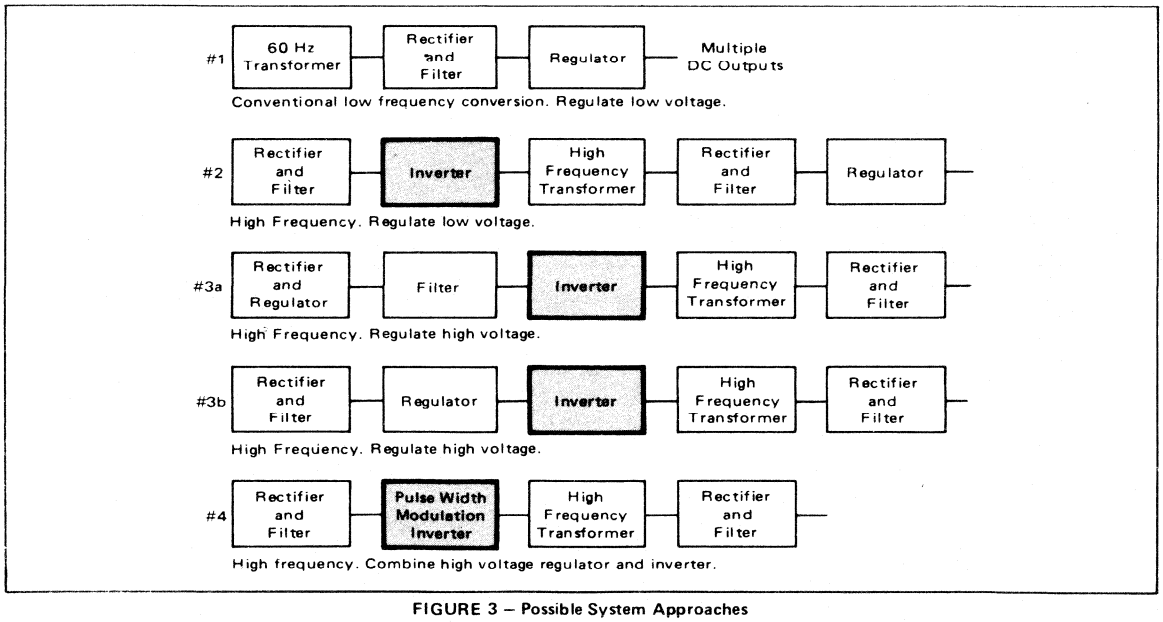


FIGURE 3 – Possible System Approaches

outs and peripheral equipment. Industrial systems generally have logic voltage requirements and may also need ±15 V and 24 V or 48 V for operational amplifiers and relay drivers. The advantages and disadvantages of each system are not too obvious, but can be brought out more clearly by some practical considerations. The first system uses a low frequency conversion technique while the remaining three systems operate at ultrasonic frequencies.

System #1. This is a conventional approach which uses a 60 Hz transformer or ferroresonant transformer to step down the line voltage for the rectifier and regulator circuits. It has been more economical in the past, but is bulky and generates more heat than the high frequency approaches.

System #2. This system uses the same building blocks required of all high frequency regulators but the sequence is varied. The line rectifier is followed by a high-voltage, high-frequency inverter and the regulation is accomplished at the low-voltage, high-current outputs of the inverter transformer. Each output can be individually regulated to provide precise voltage control over wide variations in load. There are two drawbacks to this approach: (1) several low-voltage, high-current regulators are required and (2), the efficiency will be lower than for the remaining approaches which regulate the high-voltage and low-current power.

System #3. This system uses high-voltage regulators to power the inverter which drives the low-voltage rectifiers and filters. The regulator may use SCR's for phase control (#3a) or high voltage transistors in either a linear or switching mode (#3b). Of the two approaches, the SCR may be preferred because of economy. In both this approach and approach #4, only one output can be regulated, usually the 5 V. This is not a serious drawback because line regulation is common to all outputs and slight changes in the memory and peripheral equipment supplies due to load changes are not critical.

System #4. This system is similar to #3 except regulation is accomplished in the inverter circuit by using pulse width modulation (PWM) techniques. It conserves power devices but does require a more elaborate high-current LC output filter. This appears to be the most practical approach because power is handled only once and its regulation is sufficient for most applications.

The inverter circuit common to all the high frequency approaches is the primary means for obtaining small size and higher efficiencies. For this reason, an inverter design is highlighted in the second part of this article. Before proceeding with a discussion of this design, it is worthwhile to discuss the most common switching regulator and inverter circuits in use today.

Switching Regulator Circuits

Single transistor regulators are very popular below 200 W but don't compete well with inverters at higher power levels because of cost and performance. Two of the most popular switching regulator circuits are shown in Figure 4. The circuit of Figure 4a has been around a long time. It uses a 60 Hz transformer for isolation and a low voltage switching transistor to supply a series of high frequency (20 kHz) power pulses to an LC filter. The duty cycle control circuit determines the average output voltage. It's popular today because it is simple to design and uses standard off-the-shelf components. Many of these circuits use a standard linear IC[2] regulator for the complete control function. The chief disadvantage of this circuit is the large size of the 60 Hz transformer.

The circuit in Figure 4b is more representative of present day switching regulator designs. It uses a high voltage switching transistor to drive a 20 kHz transformer directly from the rectified line. Primary inductance is the key to operation of this circuit. With variable pulse width control, the energy stored and switched to the output capacitor is adjusted to meet the demands of the load. Since this core must handle dc in the primary winding, it tends to be larger and more expensive than its inverter counterpart.

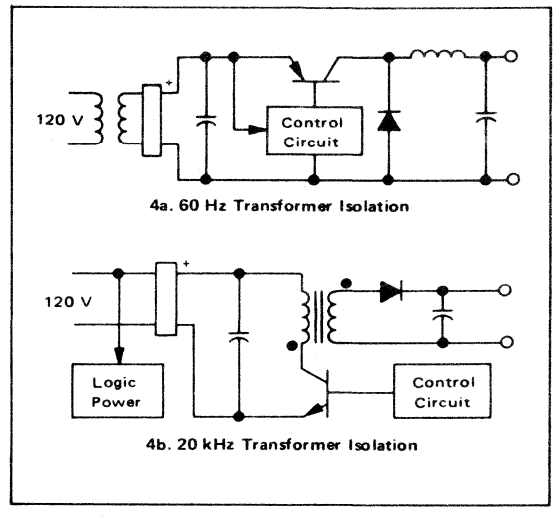


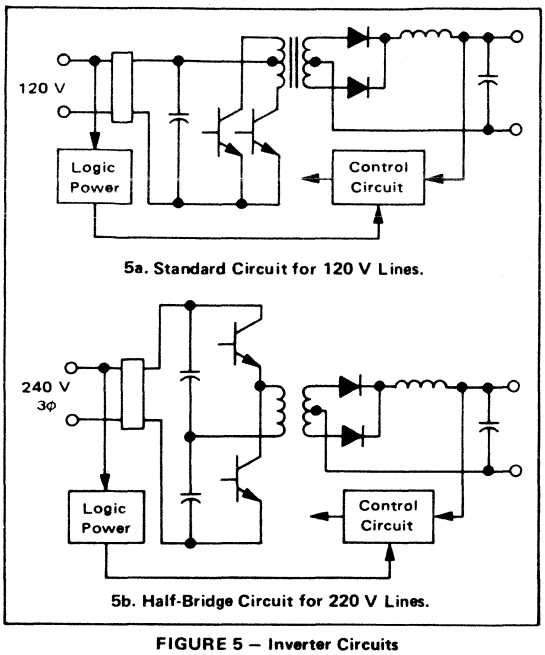
FIGURE 4 – Switching Regulator Circuits

PWM Inverter Circuits

The common inverter (two transistor) circuits operate from 120 V single phase and 208 or 220 V three phase lines and supply from 200 W to 1 kW. Most inverter transistors on the market today (including Motorola's 2N6542 through 47 family) have a nominal $V_{CEO(sus)}$ rating of 300-400 V. This means that the devices are characterized for Safe Operating Area (SOA) up to this point and that resistive and reactive loads may be switched in this region. However, these same devices may also be operated above this voltage limit in the blocking mode. Generally, the V_{CEX} or blocking rating is about 600-800 V except for Darlingtons. Because the standard transistor has this 400 V switching limit, two separate inverter circuits have evolved for use with the low and high voltage lines as shown in Figure 5. The standard

[2]See the MC1723 data sheet as an example.

inverter is used when 120 V power is available and the half bridge is generally chosen for 220 V applications. Both circuits operate in a similar fashion by alternately switching power to the 20 kHz transformer. The transformer output is rectified and the amplitude and duty cycle of the output voltage pulses determine the average output voltage. Because the output pulses are modulated to provide regulation, these circuits are known as pulse width modulated (PWM) inverters.



5a. Standard Circuit for 120 V Lines.

5b. Half-Bridge Circuit for 220 V Lines.

FIGURE 5 – Inverter Circuits

The transistor waveforms in Figure 6 represent the switching sequence for both circuits shown in Figure 5. Here it is easy to see why the dual voltage ratings of inverter transistors is important. In the standard inverter, the transistor switches collector current pulses (load current times the turns ratio) from the peak line voltage of 170 V. After some dead time, the opposite transistor is energized and the original must block twice the line voltage due to autotransformer action. In the half bridge operating from 220 V, the collector voltages are almost identical.[3] The dc bus is 340 V peak but each filter capacitor is charged to only 170 V. The transistors switch current at 170 V as before and again must block twice this voltage when the opposite side is energized. Actual waveforms are slightly different from the theoretical. The current pulse may have a spike on the leading edge and a slight positive slope due to the magnetizing current. An inductive kick during turn-off is usually present on the voltage waveform with some ringing during the dead time. These last effects are minimized by using an RC snubber across the primary to absorb the leakage reactance spikes and dampen the ringing.

Because the input filter capacitors in the half bridge must handle high RMS currents, these circuits tend to be

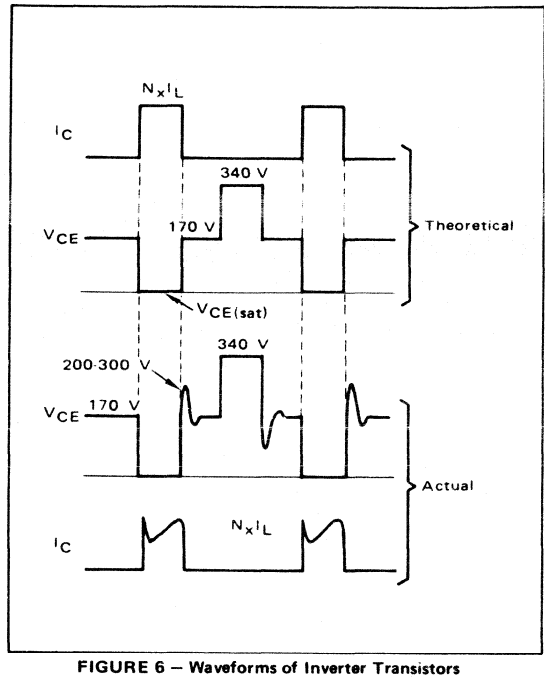


FIGURE 6 – Waveforms of Inverter Transistors

more expensive than the standard push-pull, but remain currently more popular for two reasons. One is that a coupling capacitor may be used to reduce transformer saturation problems (see reference 13 for the formula) and the second is that they can be made to conveniently operate from either 120 or 220 V (domestic or foreign). In these dual voltage designs, the capacitors are used as voltage doublers as shown in Figure 7. However, as the RMS currents are quite high in the 120 V mode, it is recommended that an additional switch contact be used to parallel the rectifier diodes as shown. The Motorola diode assemblies with ratings from 1 to 20 A are excellent for this application as the individual diodes are matched and will share current well.

The control circuits for these inverters may be located at the load or on the primary side of the transformer. Generally, power for these circuits is obtained from the ac line using either a free-running inverter or a standard 60 Hz transformer and series pass regulator. In the half bridge, the control circuits are grounded at the load. Voltage sense for the feedback signal is direct and transformers are used to couple the drive signals to the power transistors. The standard inverter may use this system or ground the control circuits at the power transistors. This latter approach simplifies the drive circuits and generally improves switching efficiency. Isolation is maintained by using an optoelectronic coupler in the feedback loop.

[3]For additional information on the half bridge inverter, see references #9, #10, and #13.

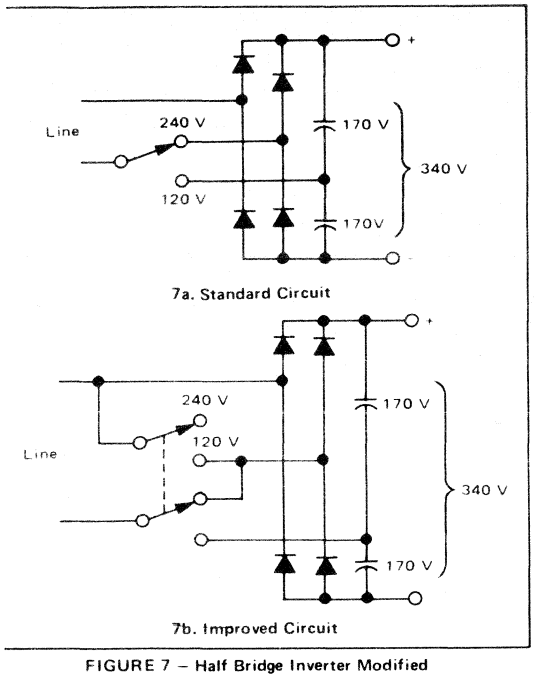


FIGURE 7 – Half Bridge Inverter Modified to Accept 120 or 240 V Inputs

5 V-40 A INVERTER SUPPLY EXAMPLE

This example deals with the design and performance of 200 W inverter supply. The design specifications are as ollows:

nput: 120 Vac ±10% @ 60 Hz
Output: 5 V @ 40 A (50 A capability; wire size, etc.)
Line/Load Regulation: ±1% (Half load to full)
Ripple: 120 Hz 10 mV_{RMS}
40 kHz 10 mV_{RMS} (Switching Frequency 20 kHz)
Ambient Temperature: 0-70°C
Efficiency: 70%

The standard inverter configuration is used with the control circuits on the primary side and an optoelectronic coupler for feedback. The block diagram is shown in Figure 8. The oscillator (an astable multivibrator) generates clock pulses which alternately set the outputs of the phase splitter (a bistable flip-flop) high. These clock pulses also enable a timing circuit in the pulse width control (a one-shot or monostable multivibrator). The splitter provides the mean for alternating these control pulses to the inverter transistor through gates 1 and 2 and the driver stage. The transistors operate the inverter transformer in a push-pull mode at 20 kHz. The output of this transformer is then rectified and filtered to become the 5 V, 40 A dc supply to the load. Logic power is obtained from the line using a 60 Hz transformer and IC series pass regulators.

CMOS logic is used for the control logic because its supply voltage is not critical and the large voltage swings provide good noise immunity. Two IC packages, a dual D flip-flop and a quad 2-input NAND gate, are used to provide all these functions (the circuitry will be described later). An operational amplifier and optoelectronic coupler are used to process the feedback signal. The high voltage supply to the inverter is a full wave bridge which operates from the 120 V line into a capacitive filter.

TRANSFORMER AND FILTER DESIGN

The power stage is the heart of an inverter; the correct choice of transistors, transformers, and filter is the most important part of this design. The magnetic design of inverter components is not too difficult when some practical guidelines are available.[4] Ferrite cores, which have a 100°C temperature limit, are normally used at 20 kHz because they have very little core loss. This loss increases slightly with 0.5 mil nickel-iron cores such as Permalloy and Orthonol, which must be used for higher

[4]See also reference #8.

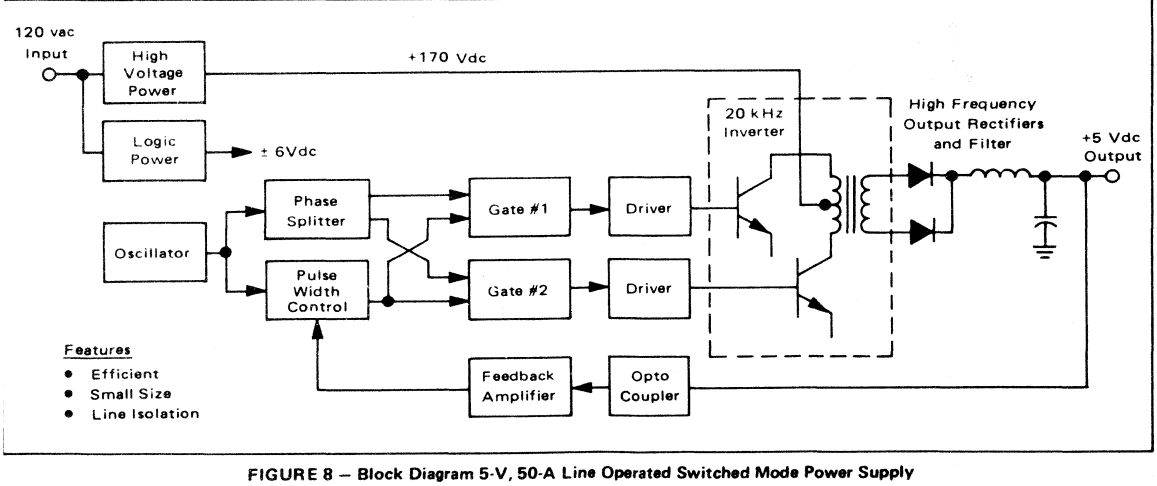


FIGURE 8 – Block Diagram 5-V, 50-A Line Operated Switched Mode Power Supply

temperature applications. For transformers, the best coupling comes from toroids, with pot cores a close second. Since toroids are difficult to wind and pot cores tend to trap heat (ferrite is a ceramic and a good insulator), C and E cores are generally used above 200 W. In addition to being easy to wind with bobbins, these latter cores facilitate the use of foil or strap to improve the winding efficiency of high current secondaries (> 50 A).

POWER TRANSFORMER

In this design, efficiency was more important than size and an oversize pot core was used for the transformer to obtain the following advantages:

1. Few turns required to operate at low flux densities
2. Low core loss (operate at 20% of B_m)
3. Low copper loss (minimized turns)
4. Good coupling
5. Relatively easy to wind (the #10 secondary was somewhat difficult to shape)

In transformer design, the turns ratio and wire size are calculated first, then the core is selected. The information in Figure 9 of transformer waveforms at low line is used to find the required turns ratio. The information required includes:

1. Low line voltage
2. Input ripple
3. Output voltage
4. Minimum dead time (and frequency)
5. Output rectifier and filter losses

The low line specification of 110 V and 20 V ripple voltage (peak-to-peak) gives a minimum dc input to the primary windings of 130 V. With 5 μs of dead time between pulses, the duty cycle is 80% and 6 V pulses are required at the filter to obtain 5 V output. Assuming the rectifier drops (0.5 V) and filter loss at full load is 1 V, the secondary voltage pulses must be 7 V minimum. An additional 10% safety factor (0.7 V) is recommended to make up for miscellaneous input rectifier, transistor, and transformer losses. The required turns ratio (N), is therefore:

$$N = V_p/V_s = 130\ V/7.7\ V = 16.8 \simeq 16 \qquad (1)$$

With the turns ratio and the control logic set to limit duty cycle to 80%, the supply stayed in regulation at 110 V and dropped out with the line at 100 V.

Some wire tables recommend using 1000 CM/A (circular mils per ampere) or 1000 A/sq inch but most designers use anywhere from 300 to 500 CM/A as a guideline. With 50 A in the secondary and a 16:1 turns ratio, primary current pulses are about 3 A. Since both windings are center-tapped, current pulses cannot exceed a 50% duty cycle. Therefore, the wire size was chosen for RMS values of 35 A and 2 A. Number 10 (12,000 CM) was chosen for the secondary and number 20 (1000 CM) for the primary. Two number 13 (6000 CM) or four number 16 (3000 CM) were considered to make the secondary easier to wind, but the pot core does not have space available to bring out the interconnections.

To determine the proper core and number of turns three steps are required as follows:[5]

Step 1. Find the minimum core size and choose core using

$$A_c A_w \geq \frac{2P_o}{f\,B_m} \times 10^{11}\ CM\ cm^2 \qquad (2$$

where A_c = core area (cm^2)
A_w = window area (CM)
P_o = output power
f = frequency
B_m = saturation flux density (gauss)

A typical ferrite material has B_m = 3000 gauss. For thi 200 W, 20 kHz inverter

$$A_c A_w \geq \frac{2 \times 250 \times 10^{11}}{20\ k \times 3\ k} = 0.83 \times 10^6\ CM\ cm^2$$

[5]The equations are from reference #7.

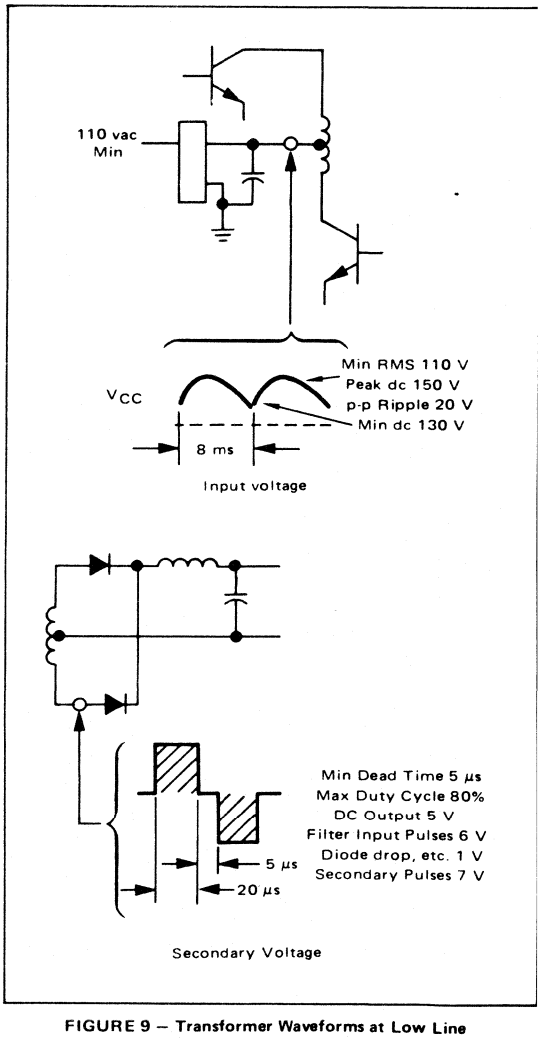


FIGURE 9 – Transformer Waveforms at Low Line

'wo cores available from the Ferroxcube catalog with ze information are listed in Table 1.

TABLE I – Ferroxcube Cup Cores

Core Number	A_c cm^2	A_w* in^2	A_w CM	A_cA_w CM $cm^2 \times 10^6$
4229	2.7	0.22	0.22×10^6	0.6
6656	7.5	0.62	0.62×10^6	4.6

*Note: This is the area available on the standard bobbin.

Because the formula uses the conservative wire rating f 1000 CM/A, it would be possible to use the 4229 core or this design. However, since it is desirable to operate ell below B_m to minimize core loss, the 6656, which is versize by a factor of five, is used.

Step 2. Find the required primary turns using

$$N_p \geq \frac{V_p \times 10^8}{4 f A_c B_m} \quad (3)$$

here N_p = primary turns
V_p = primary voltage

lere the primary voltage is the peak of the high line input 130 V) and

$$N_p \geq \frac{130 \times 1.4 \times 10^8}{4 \times 20\text{ k} \times 7.5 \times 3\text{ k}} = 10$$

his is the minimum number of turns required. Since ive turns are desirable on the secondary for good coupng, and the turns ratio is 16:1, 80 turns were used on he primary instead of 10.

Step 3. "Check the fit" of wire and window area using

$$A_w \geq 2(N_p A_{xp} + N_s A_{xs})/0.8 \text{ CM} \quad (4)$$

here N_s = secondary turns (N_p/N)
A_x = wire size (CM)

n this case the primary wire size is 1000 CM (#20) and the econdary wire size is 12,000 CM (#10). This gives

$$A_w \geq 2\ (80 \times 1\text{ k} + 5 \times 12\text{ k})/0.8 = 0.35 \times 10^6 \text{ CM}$$

he available winding area on the 6656 bobbin is 0.62 x 0^6 CM which indicates that only about half the availble space was used.

ILTER CHOKE

For the output filter choke, it was decided to use wo "U" cores, as these cores facilitate winding high urrent strap or foil. In filter design, the inductance and /ire size are calculated first, then the core choice follows. nductance can be calculated using

$$L \geq V_o/f\ (0.10)\ I_o(\text{min}) \quad (5)$$

here L = inductance (H)
V_o = output voltage
f = frequency
I_o(min) = minimum output current

n this case the minimum output current was chosen to be 20 A (just less than half load). The frequency is 40 kHz at this point (from the full wave rectifiers); therefore

$$L \geq \frac{5}{40\text{ k}\ (0.10)20} \simeq 60\ \mu\text{H}$$

The 0.10 factor limits choke current variations to 10% at light loads. To conserve space, it is possible to allow 100% current variations and use a 6 μH choke. However, most designs follow the 10% guideline.

Wire size is determined using 500 CM/A as the guide. The choke current can be 50 A continuous, so two 1.125" by 10 mil copper strap were used for the winding. Strap or foil is easier to wind than the large wire and is also preferred as it will lie close to the core for good magnetic coupling.

Four steps are required to choose the core and determine the proper number of turns and the required air gap size as follows.[6]

Step 1. Find the minimum core size and choose a core using

$$A_cA_w \geq \frac{A_x\ LI \times 10^8}{0.8\ B_m} \quad (6)$$

where I = Saturation current level

Ferrites used for U cores have B_m = 3800. For this design, it was already determined that a 60 μH, 50 A choke is required and that the strap size is 22,500 CM (2.25" x 10 mil"). Therefore

$$A_cA_w \geq \frac{22.5\text{ k} \times 60\ \mu \times 50 \times 10^8}{0.8 \times 3800} = 2.3 \times 10^6 \text{ CM cm}^2$$

Ferroxcube catalog information on two possible U cores is shown in Table II.

The 1F10 core is a good choice here, but a 1F5 was used instead as it was available.

Step 2. Find the required number of turns using

$$N = \frac{LI}{A_cB_M} \times 10^8 \quad (7)$$

In this case, A_c = 6.45 and

$$N = \frac{60\ \mu \times 50 \times 10^8}{6.45 \times 3800} = 14 \text{ turns}$$

Step 3. "Check the fit" of wire and window area using

$$A_w \geq NA_x/0.8 \quad (8)$$

which gives

The core used has a window area of 5.0 x 10^6 CM which allows plenty of room for this winding. Mylar tape was used to insulate the layers.

[6]The equations are from reference #7.

TABLE II – Ferroxcube U-U Cores

Core Number	A_c cm^2	A_w* in^2	A_cA_w CM $cm^2 \times 10^6$
1F10	2.04	1.5	3.0
1F5	6.45	5.0	32

*Note: Obtained from inside core dimensions.

Step 4. Determine the air gap required to prevent saturation using

$$l_g = \frac{0.4\pi NI}{B_M} - \frac{l_m}{\mu} \qquad (9)$$

where l_g = air gap length (cm)
l_m = magnetic path length (cm)
μ = core permeability

Using the catalog, we find that only 3C5 material is available for this U core configuration (with μ = 2000) and that l_m = 31.5 cm. Therefore,

$$l_g = \frac{0.4\pi \times 14 \times 50}{3800} - \frac{31.5}{2000}$$

$$= 230 \times 10^{-3} - 15 \times 10^{-3} = 215 \times 10^{-3} \text{ cm}$$

Converting l_g to inches gives a required gap of 80 mils or 40 on each side of the core. It should be noted that the gap reluctance is much higher than the core reluctance (230:15) and that it therefore is controlling L and I. This being the case, if the gap is doubled, L halves and I doubles. If the turns are doubled, L increases by 4 (N^2) and I is halved. Therefore, if both the turns and gap are doubled, I remains the same but L doubles. When there is additional winding space available, it is possible to increase the inductance by filling this area even though the gap must be increased appropriately to prevent saturation at the rated current.

In this case, these relationships were used to check the magnetic design just completed. 140 turns (instead of 14) of light wire were placed on the core and it was gapped at 80 mils. L and I were then measured at relatively low test levels resulting in 6 mH of inductance which saturated just over 5 A. Thus, the calculated 14 turns give us 60 μH at 50 A.

Filter Capacitor

With the completion of the transformer and filter designs, the remaining passive component required in the power stage is the output filter capacitor. The size of this capacitor is determined using[7]

$$C \geq \frac{(V_{in} - V_o)V_o}{2Lf^2 V_{in} v_o} \times 10^6 \,\mu F \qquad (10)$$

where C = capacitor size (μF)
V_{in} = filter input voltage (V)
V_o = filter output voltage (V)
v_o = peak to peak output ripple at the switching frequency (V)

There is no dependance on load in this formula, as only the changes in ductor current must be filtered out. These changes are dependent only on voltage, inductanc and frequency and not on the average inductor (or load current. With a nominal 160 V in to the 16:1 powe transformer, the input amplitude to the filter is 10 V Ripple frequency is 40 kHz and the ripple specification i 10 mV (RMS) or 28 mV peak to peak. This gives

$$C \geq \frac{(10 - 5) 5 \times 10^6}{2 \times 60\,\mu\,(40\text{ k})^2\, 10 \times 28\text{ m}} = 460\,\mu F$$

A 500 μF four terminal (high frequency) capacito could be used but a lower cost standard aluminum electrc lytic was chosen instead. Because series resistance an inductance are higher with the standard, a larger siz (2000 μF) was required to obtain the desired performance

POWER STAGE

The power stage is comprised of the following circuits:

1. High voltage power supply
2. Logic power supply
3. Drivers
4. Power transformer and transistors (inverter)
5. Output rectifiers and filter

The schematic of these circuits is shown in Figure 10. A bridge rectifier and capacitive filter are connected directly to the 120 Vac line to form the high voltage supply. The output is 160 Vdc with ≈ 20 V peak-to-peak of 120 Hz ripple. These voltage variations are attenuated 60 dB by the control circuits resulting in ≈ 10 mV of low frequency ripple at the load.

The logic supplies are obtained using a 15 W filament transformer, bridge rectifier, and filter to operate ±6 V three terminal IC regulators (the MC7806 and 7906). The logic is connected between these two low-voltage supplies.

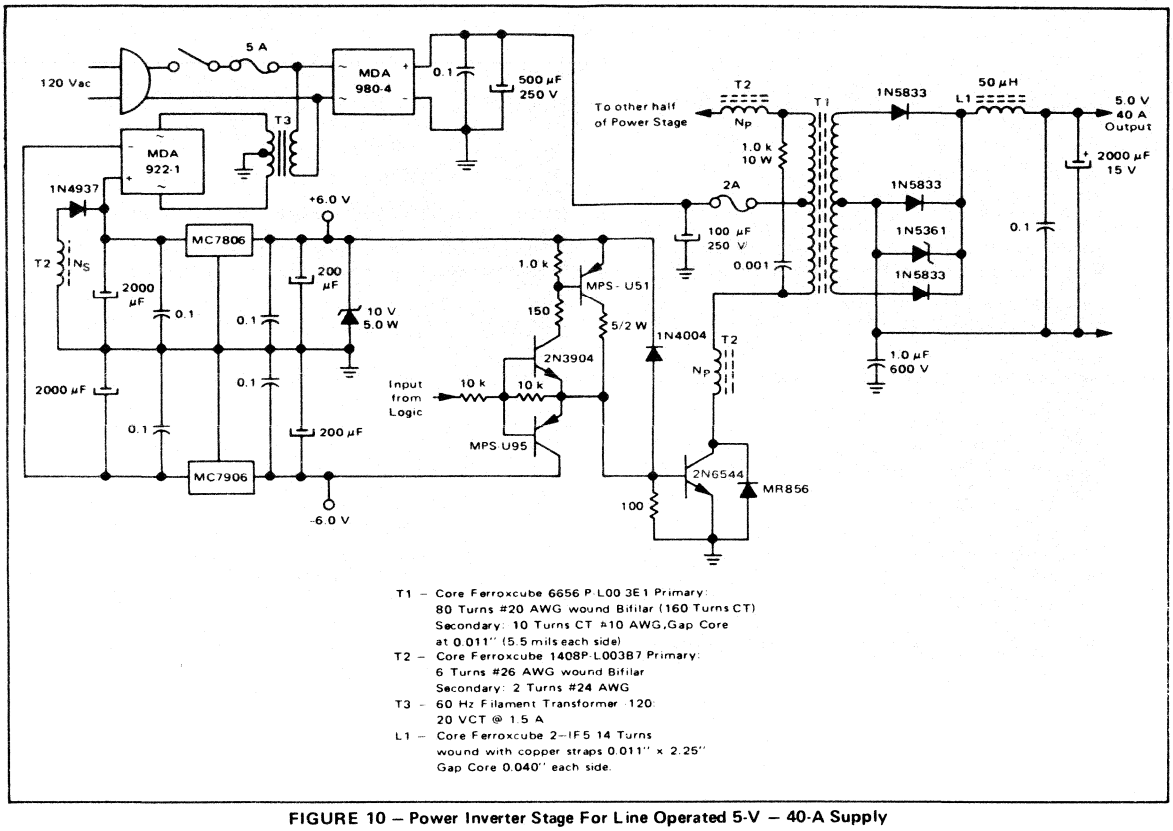
The two voltages are used with a push-pull drive stage to provide both positive and negative base drive to the inverter transistors. When the logic signal is high, the 2.0 A MPS-U51 saturates and supplies 1 A to the base of the 2N6306 inverter power transistor. When the logic is low, the 1.5 A MPS-U95 darlington operates in a current limited mode during storage time and then applies -5 V to the base to hold the inverter transistor off. Figure 11 shows this base current waveform at rated load. Storage time is under 2 μs with these fast switching Uniwatt▲ drivers and will increase slightly at lighter loads.

Power Transistors

Motorola 2N6544 power transistors were used in the inverter because they are fast and economical. These transistors have an 8 A current rating, but are specified for beta and switching speed and used here at 3 A of collector current. The switching sequence and load lines at full load of these devices (before and after shaping) are shown in Figure 12. A current spike observed during turn-on was contained using 80 μH of inductance on a common pot core in series with each collector. This improved the load line and reduced turn-on losses in

[7] This equation is from reference #3.

▲ Trademark of Motorola, Inc.



T1 – Core Ferroxcube 6656 P L00 3E1 Primary:
80 Turns #20 AWG wound Bifilar (160 Turns CT)
Secondary: 10 Turns CT #10 AWG, Gap Core
at 0.011" (5.5 mils each side)

T2 – Core Ferroxcube 1408P-L00387 Primary:
6 Turns #26 AWG wound Bifilar
Secondary: 2 Turns #24 AWG

T3 – 60 Hz Filament Transformer 120:
20 VCT @ 1.5 A

L1 – Core Ferroxcube 2–IF5 14 Turns
wound with copper straps 0.011" x 2.25"
Gap Core 0.040" each side.

FIGURE 10 – Power Inverter Stage For Line Operated 5-V – 40-A Supply

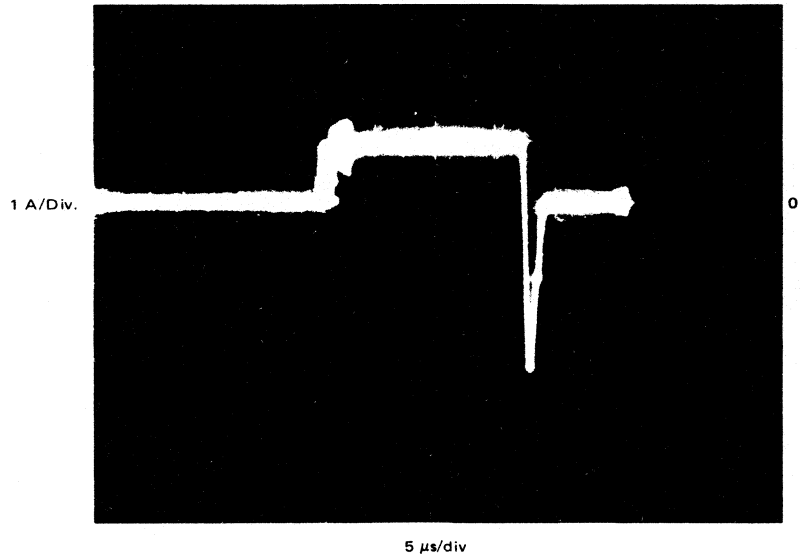
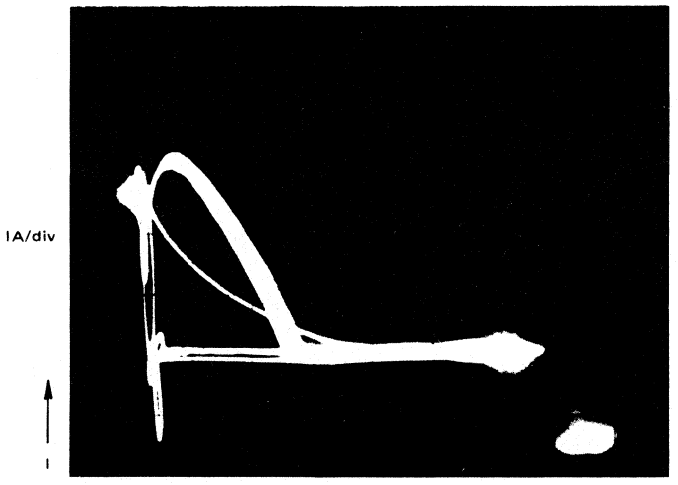
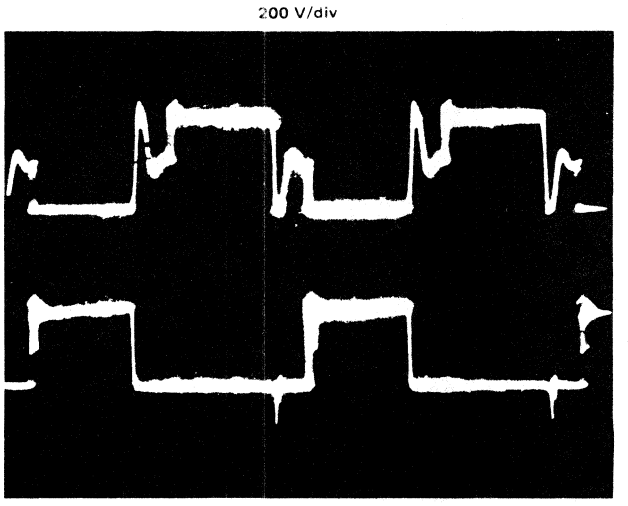
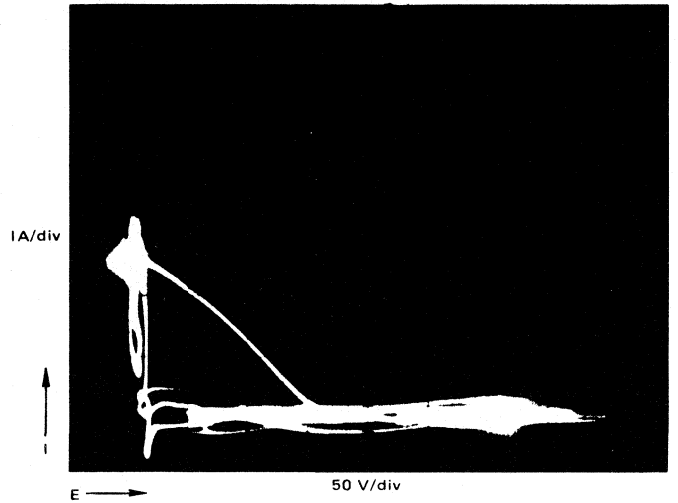


FIGURE 11 – Base Current







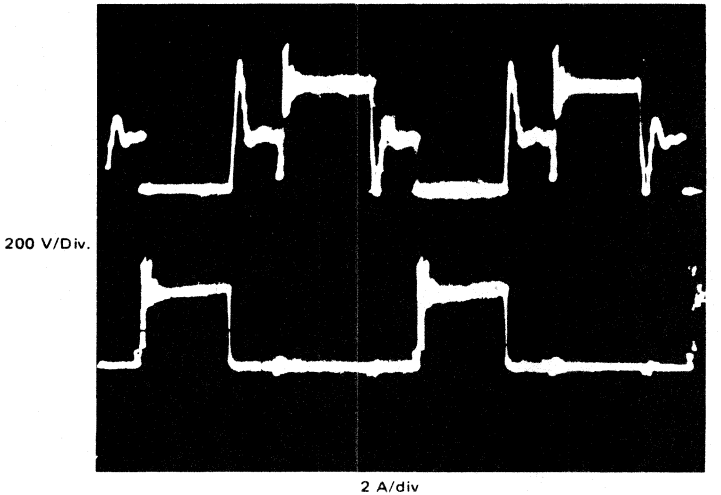


FIGURE 12 – Load Lines

the transistors without significantly affecting turn-off. Energy stored in these inductors is returned to the low voltage filter capacitor during the dead time interval (5 μs minimum) by the secondary winding on this core.[8] This technique therefore affords very efficient suppression of the current spikes with controlled voltage clamps. The resulting load line shows resistive switching during turn-off to 150 V and blocking to 400 V. The V_{CEO} and V_{CEX} ratings on this device are 300 and 650 V which are quite adequate for this application.

The inductive kick from the core can be observed as turn-off voltage spikes in Figure 12. These spikes are clamped to twice the supply by diodes across each transistor, and are "snubbed" by the standard RC network across the primary to allow the transistors to turn off before this voltage level is reached.

Transformer Saturation

The transformer, as discussed earlier, is a 2.5" ferrite pot core from Ferroxcube, hand wound with a 16-to-1 turns ratio. The collector current pulses of 2.5 A in Figure 12 therefore represent a load current of 40 A. The core was gapped empirically at 10 mils to provide about 100 mA of magnetizing current. This increases the saturation level and allows a slight imbalance in primary current pulses to exist. Such an imbalance can be created by component drifts or load changes and tends to build a dc component of flux in the core (a process known as "racheting"). This ultimately causes core saturation and destroys the power transistors.

Matched transistors (beta within 10% at 1 A) were initially used in this unit. However, subsequent field tests revealed that matched transistors are not sufficient to prevent long term transformer saturation. Based on these findings, it is now recommeded that either symmetry correction circuits or a simple over-current shutdown circuit be used for all direct coupled push-pull inverters. A suggested shutdown circuit is shown in Figure 13.

Output Rectifiers and Filter

Because efficiency is important, 50 A, 30 V barrier diodes (Motorola 1N5833) are used as the output rectifiers, although they are more expensive than fast recovery rectifiers. These diodes are fast and have low forward drops (0.5 V). However, junction temperature is limited to 100°C and for this reason, a fairly large heat sink is required (0.5°C/W) to operate safely in 70°C ambients without forced air cooling. A free wheeling diode was used but carries little current. All three diodes are protected against voltage transients (a 1 μs voltage transient can cause shorts) by a 27 V, 5 W zener placed across the free-wheeling diode. The rectifier current waveform is shown in Figure 14. The peak current is 40 A (full load) and drops to half during the dead time (each rectifier shares the filter choke current). The absence of reverse recovery spikes in this picture is an indication of the excellent high speed blocking characteristics of these parts.

The output filter elements were discussed earlier. The choke was made by winding copper strap on two "C" cores with outside dimensions of 4 x 4.5" and gapping it to prevent saturation. The capacitor is a standard 2000 μF electrolytic with a single 0.1 μF RF bypass in parallel. Worst case design of the choke allowed 2 A variation in choke current. The normal choke current variations shown in Figure 15 are only 0.8 A. With these components, the 40 kHz ripple is 25 mV peak to peak.

[8]For additional information, see references #1, 2, and 12.

[9]For additional information, see reference #11

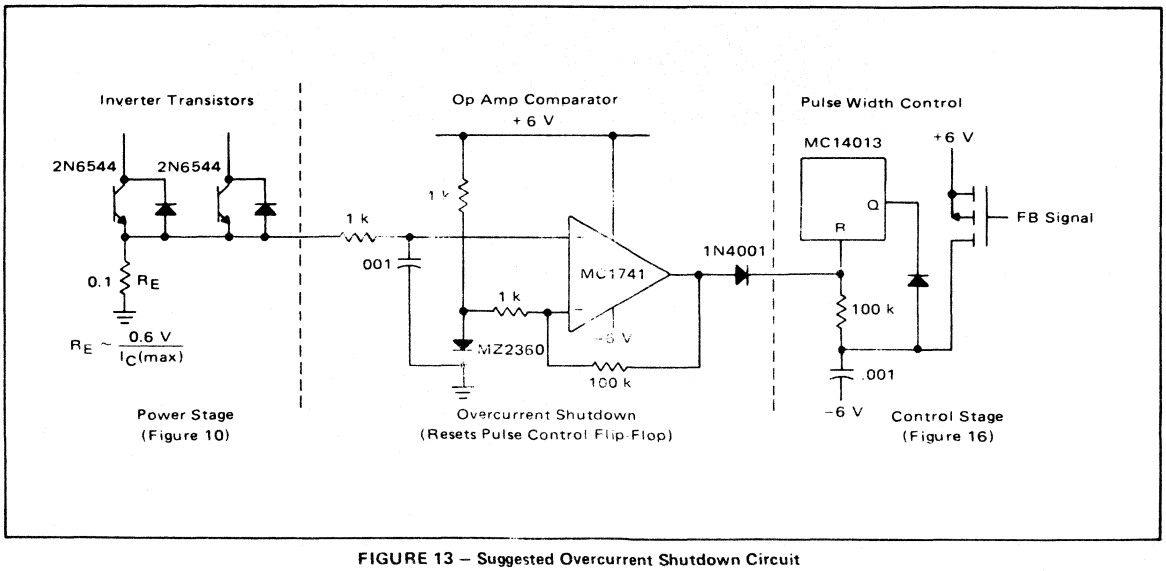


FIGURE 13 – Suggested Overcurrent Shutdown Circuit

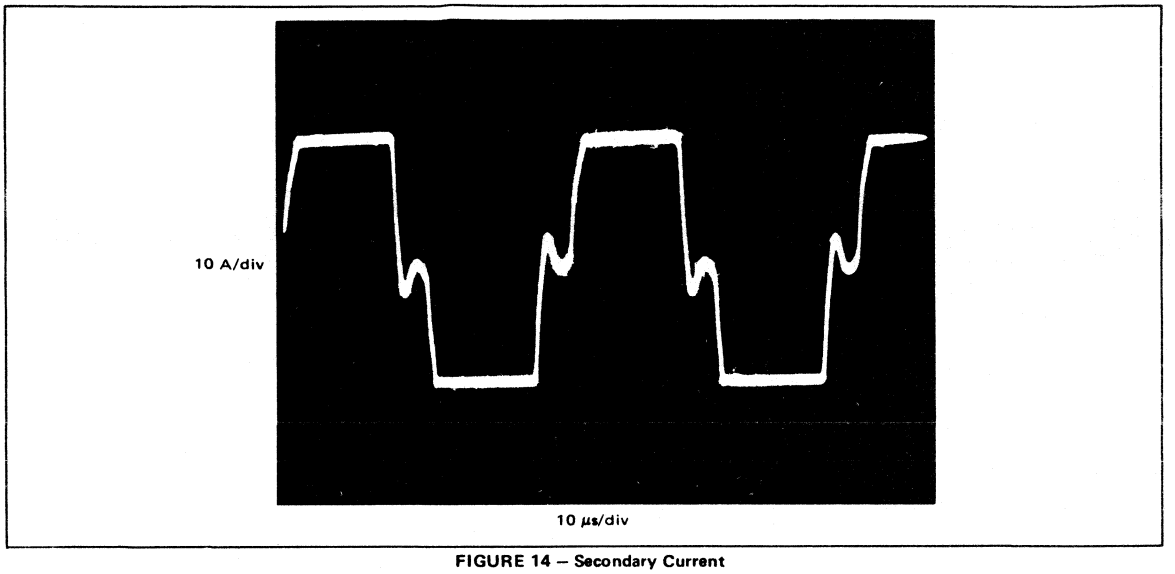


FIGURE 14 – Secondary Current

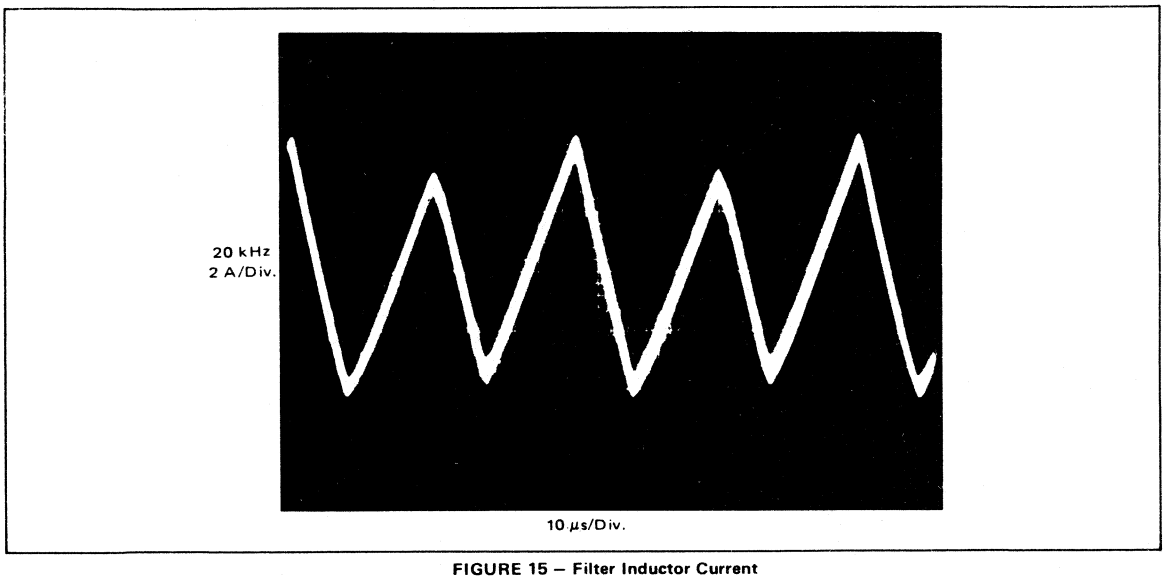


FIGURE 15 – Filter Inductor Current

CONTROL STAGE DETAILS

The basic functions of the control stage were discussed earlier in the block diagram section. The schematic of this stage is shown in Figure 16. The various circuits required for the control function include:

1. Oscillator
2. Phase splitter
3. Pulse width control
4. Gates
5. Opto isolation
6. Feedback amplifier

Functions 1 and 4 are obtained from a single CMOS package, the MC14001 quad 2-input NOR gate. A second CMOS package (the MC14013), a dual D flip-flop is used to implement functions 2 and 3. Two other dual-in-line IC packages, the 4N28 optoelectronic coupler and the MC1741 operational amplifier, contain the circuits used to implement functions 5 and 6.

The phase splitter is a flip-flop which operates in the toggle mode with $\overline{Q}$ connected to D. The pulse control flip-flop operates as a one shot and resets itself when the FET current charges the 0.001 μF timing capacitor to half

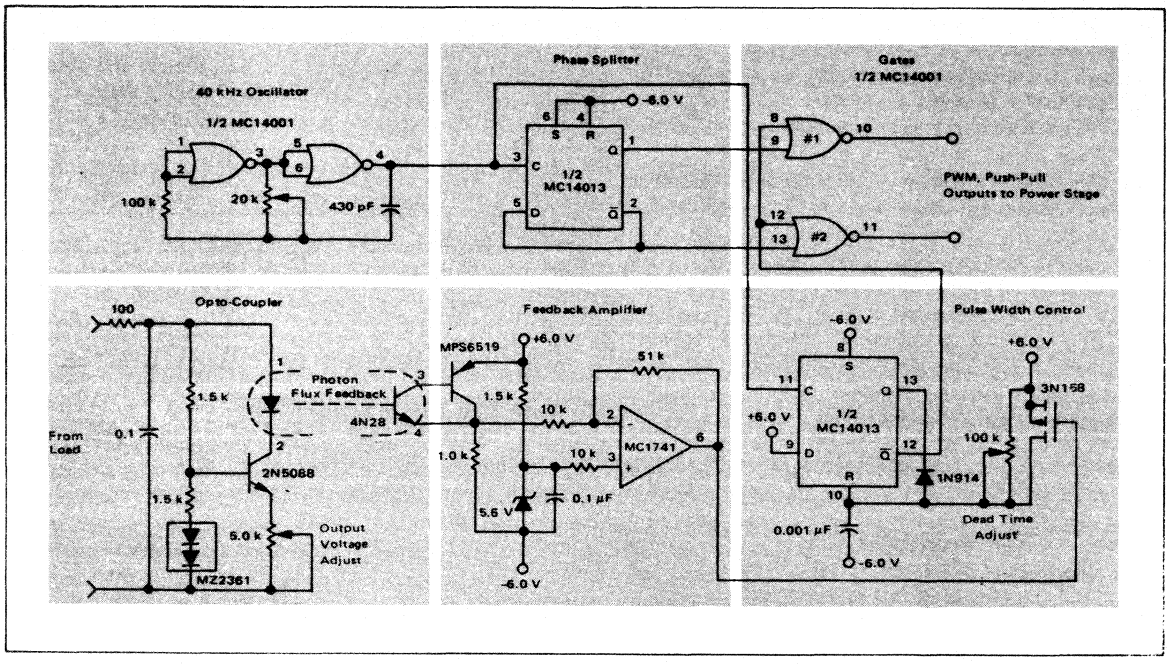


FIGURE 16 – Logic Schematic for Line Operated 5-V, 40-A Supply

the supply. The gates are enabled (high out) and turn on one of the power transistors only when both inputs are low. Since the splitter alternately causes one gate input to be low and then the other, both transistors can never be on at the same time. To further guard against simultaneous conduction and high "shoot through" currents, a resistor across the FET forces reset action in the one shot to occur in 20 μs, 5 μs before the opposite side is enabled. Because the one shot is also connected to both gates, it introduces inhibiting action even before the splitter changes state. The interaction of the stages may be easier to see in the timing diagram (Figure 17). Positive clock pulses toggle the splitter and enable the one shot (or pulse width control circuit). When the control is low and the Q output of the splitter is low, gate #1 is enabled and turns one of the inverter transistors on. On the next clock pulse, the control will go low again and the Q output of the splitter will be high ($\overline{Q}$ low). At this time, gate #2 is enabled and the remaining inverter transistor turns on.

The pulse width of the control circuit determines the output voltage and it in turn is controlled by the feedback elements in this closed loop system. The optoelectronic coupler makes use of the LED to sense output voltage changes and feed back a signal to the photo transistor and operational amplifier. The operational amplifier gain determines how good the line and load regulation will be and how much ripple reduction to expect. Too much gain will cause instability and high output ripple content. The excessive ripple is created when the pulse width control vacillates from wide to narrow pulses without ever settling on the appropriate width for the given line and load conditions. To improve stability, a low frequency filter is often added at this point (such as the RC filter shown at the LED input). The operational amplifier output voltage is fed to the gate of a P-channel MOSFET. The FET performs a voltage-to-current conversion in this design and controls the charge rate of the timing capacitor which determines the output pulse width.

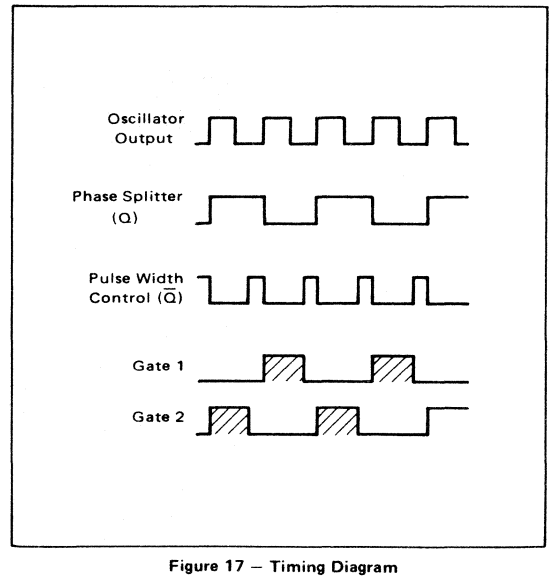


Figure 17 – Timing Diagram

Performance Data

The main features of this supply are that it is efficient and small. Some size was sacrificed in this design, in three areas specifically, to improve efficiency:

1. The barrier diode heat sink. Forced air cooling would reduce this size.
2. The inverter transformer. A large core which operates at low flux densities was used to reduce core losses.
3. The 60 Hz low voltage power transformer. A free running inverter could have been used.

Efficiency was measured with 40 A load current at 5 V. The input voltage and current waveforms are shown in Figure 18 and contain the information required to calculate input power. Assuming the input voltage is constant during current conduction:

$$P_{in} = \frac{V_{IN(peak)}}{T} \int_0^T Idt \qquad (11)$$

where P_{in} = average input power
$V_{IN(peak)}$ = peak input voltage
$\int Idt$ = area of the current pulse
T = half cycle period

with $V_{IN(peak)}$ = 165 V, T = 8.3 ms and counting 15 sq cm at 4 A and 0.2 ms per cm gives

$$P_{in} = \frac{165}{8.3\ m}(15 \times 4 \times 0.2\ m) = 240\ W$$

The efficiency therefore is

$$\eta = \frac{P_o}{P_{in}} = \frac{5\ V \times 40\ A}{240} \approx 83\% \qquad (12)$$

The total power loss in this design is about 40 W. Of this about 20 W is lost to the output rectifiers and 5 W to each IC regulator and both base resistors (another 15 W total). There was no noticeable heat rise in either the transformer or the power transistors.

This design also features line and load isolation which is made possible by the inverter transformer and optoelectronic coupler for feedback. Output voltage readings under the specified line and load variations are shown in Table III.

TABLE III – Output Voltage Readings

$V_{IN(RMS)}$	I_o	V_o
110	40	5.009
120	40	5.046
130	40	5.062
110	20	5.057
120	20	5.080
130	20	5.092

Using this data, and defining regulation as

$$\%\ Reg = \frac{\Delta V_o}{V_o} \times 100 \qquad (13)$$

gives

1. Line regulation at 40 A = 1.1% (53 mV)
2. Load Regulation at 120 V = 0.7% (34 mV)
3. Combined regulation = 1.7% (83 mV)

These figures represent the typical performance that can be obtained from this type of supply of 1% regulation before stability becomes a problem.

The ripple content of the output voltage at rated load is shown in Figure 19. In Figure 19A the 120 Hz ripple is 20 mV peak-to-peak or less than 10 mV_{RMS}. Input ripple was 20 V and with gain optimized, a 60 dB reduction was obtained. To further reduce 120 Hz ripple, the input filter capacitor would have to be increased. In Figure 19A, the 40 kHz ripple is also 20 mV peak-to-peak. In the previous filter design section, it was pointed out that this is strictly a function of the output filter elements. However, with practical high frequency limits of present components, the best designs can only reduce this num-

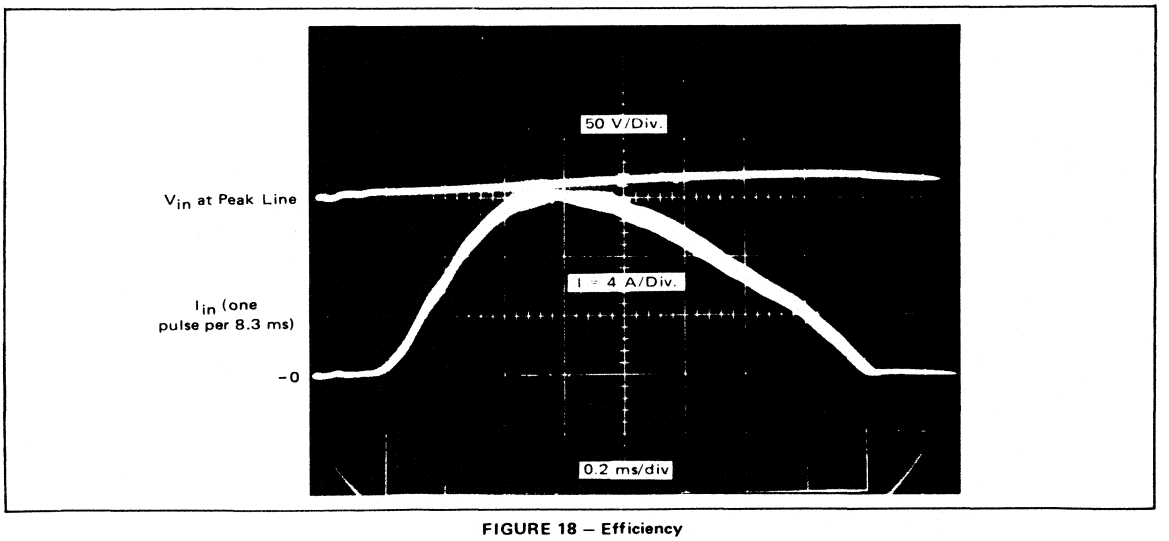


FIGURE 18 – Efficiency

ber to about 5 mV. Noise spikes, which are difficult to see in the pictures, were approximately 200 mV peak-to-peak. The spikes couple through the interwinding capacity of the filter inductor and are attenuated slightly by the 0.1 μF ceramic bypass capacitor. Further reduction would require an additional high frequency LC filter.

The overall performance of this regulator is quite good. The 10 mV ripple is more than adequate to drive standard TTL logic loads of small computers. In addition, several of these circuits could be operated from a dc bus between 140 and 200 V to supply the power requirements of a larger computer or industrial system. The 80% efficiency is exceptional. The completed supply required about 400 cubic inches and weighed about 10 pounds (see Figure 20). A further reduction in size and weight is possible with smaller heat sinks, forced air cooling and some sacrifice in efficiency by using a smaller inverter transformer and filter choke.

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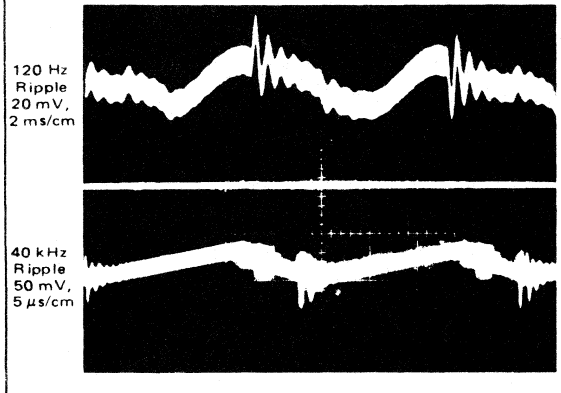

FIGURE 19 – Output Ripple

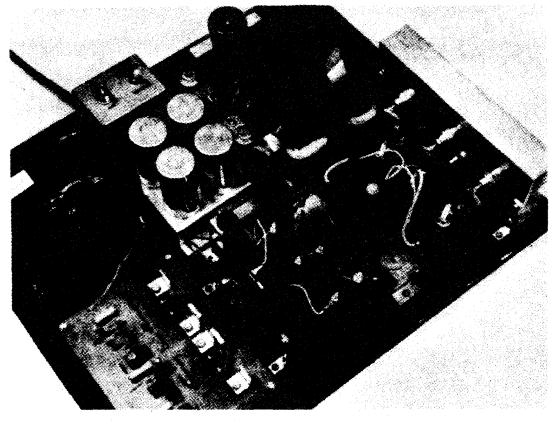

FIGURE 20 – Complete Supply

ACKNOWLEDGEMENT

The author wishes to acknowledge Paul Fletcher for the design improvements he contributed.

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MOTOROLA
Semiconductor Products Inc.

AN-785
Application Note

REVERSE BIAS SAFE OPERATING AREA

Prepared by
Bob Bailey

The rating of high voltage, high speed switching transistors for safe turn-off operations is examined. Clamped inductive turn-off measurements are used to generate a switching RBSOA—reverse bias safe operating area—which can be used in conjunction with load line analysis to assure proper transistor operation. The effects of inductance, temperature, base turn-off conditions and forward base drive on RBSOA are included in the discussion.

INTRODUCTION

Construction of power transistors with increased voltage, current, and speed required for applications such as switching power supplies, motor controls, and horizontal deflection has necessitated compromises in capability to handle turn-off switching energy. The specification typically used to show capability in this mode has been non-clamped Es/b, which was established many years ago as a figure of merit for extremely rugged, low voltage transistors generally used in series pass applications. Although modern devices can handle many thousands of volt-amperes during switching intervals, in general they have limited capability in avalanche. Therefore, to apply a non-clamped Es/b specification to the newer devices, one has to severely limit the time actually spent by the transistor in avalanche, making the choice of coil, turn-off base conditions, and collector current very delicate. The resulting specification has in most cases been of limited value to the circuit designer.

The use of a switching RBSOA (or just RBSOA) plot is proposed, similar to familiar forward-bias SOA, to demonstrate capability to handle turn-off switching energy. The circuit designer can then compare his turn-off load line with the RBSOA plot. Knowing his turn-off conditions and how they affect RBSOA, he can make sure that his design will not stress the transistor to the point of degradation or failure.

TURN-OFF AND RBSOA

In switching applications, two key parameters related to turn-off conditions are of interest to the circuit designer: storage time and switching losses. In many designs, storage time of pairs of devices must be either matched or greatly minimized to avoid saturation of magnetic cores; the alternative is fairly complex control circuitry. Storage time also can limit the range of regulation. Switching losses are of concern because they affect efficiency and determine required heat sinking for reliable operation. Figure 1 and 2 show switching waveforms for resistive and clamped inductive turn-off loads for a high voltage, high current Darlington. At 20 kHz, this device under these conditions would generate 13.2 watts of switching loss with a resistive load and 19 watts with an inductive load. Note that the inductive load generates much higher peak energy than the resistive load, and indeed could cause second breakdown failure if the RBSOA capability of the device is exceeded.

FIGURE 1 — Resistive Switching Turn-off Waveforms

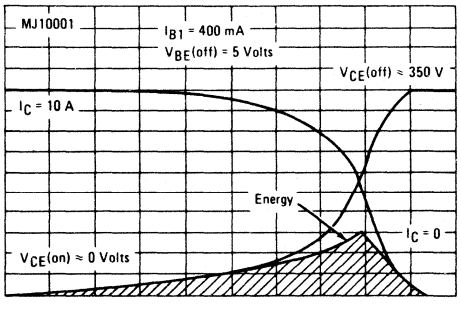
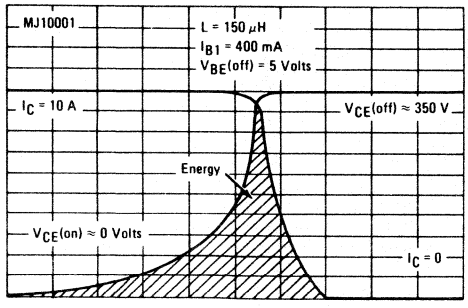


FIGURE 2 – Clamped Inductive Switching Turn-off Waveforms



Figures 3 and 4 show, respectively, t_{sv} and t_c versus base turn-off voltage for the high voltage Darlington and for a high voltage, moderate current discrete. (t_{sv} is defined as storage time from 90% I_{B1} to 10% V_{CE} and t_c as commutation time from 10% V_{CE} to 10% I_C in a clamped inductive switching circuit.) Obviously, a designer would choose V_{BE}(off) to be as high as possible to minimize t_c (switching losses) and t_{sv}.

Es/b

Degradation and/or failure of a transistor in the turn-off mode can be caused by Es/b reverse-bias secondary breakdown energy. Whereas Is/b occurs with energy concentrated at the emitter periphery, Es/b is different in many ways from Is/b forward-bias secondary breakdown, since the concentration of energy on the chip is focused during turn-off to the center of the emitter. Es/b can occur below actual device avalanche, and can be

FIGURE 3 – Storage Time versus V_{BE}(off)

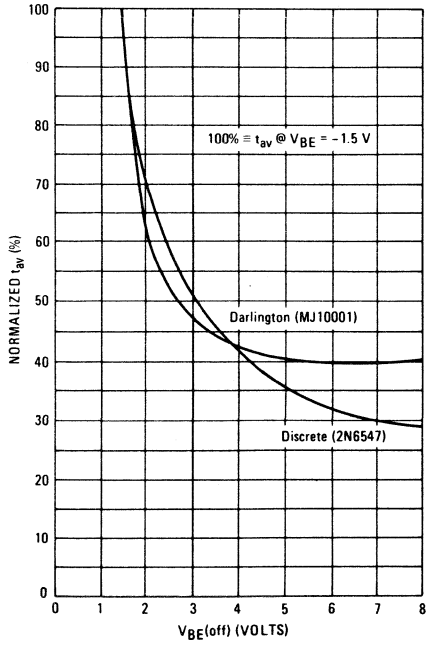
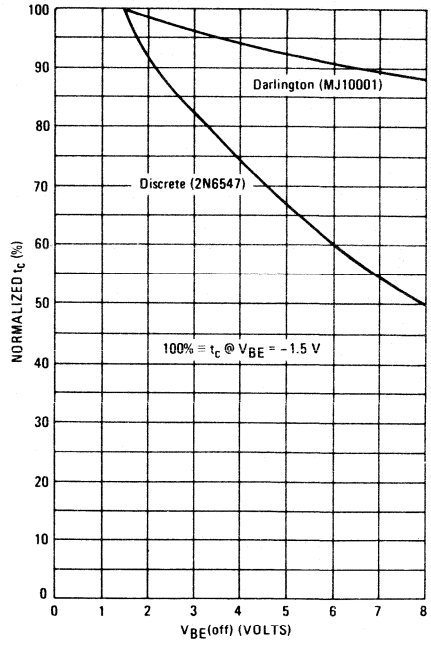


FIGURE 4 – Commutation Time versus V_{BE}(off)



less than Is/b for certain V-I combinations in a given device. And, as might be expected, it behaves differently from one device construction to the next.

From the earlier discussion, it seems apparent that one should use high off-bias to minimize storage time and switching losses. What does this do to second breakdown capability? Below actual device avalanche, increased off-bias can improve capability, and under avalanche conditions, capability can be decreased. This has led to some confusion about how a device should be rated, and how it should be operated to achieve satisfactory reliability.

The traditional method of rating reverse-bias second breakdown has been with an unclamped inductive switching circuit, as shown in Figure 5. The energy rating is calculated as:

$$Es/b = 1/2 L_{(eff)} I_C^2$$

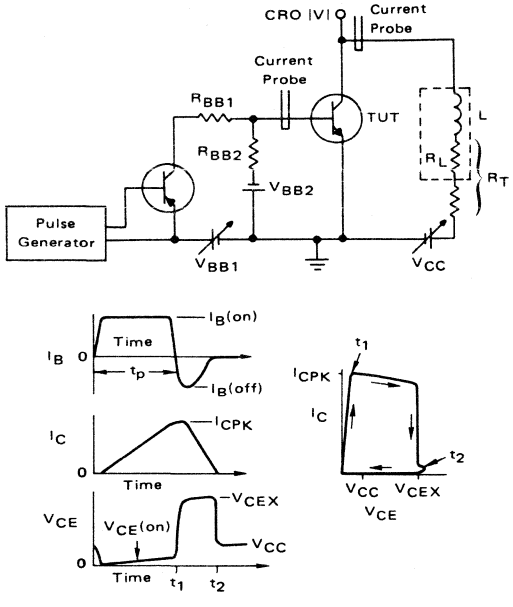
where $L_{(eff)} = \frac{V_{CEX}}{V_{CEX} - V_{CC}} L$.

If the inductor and collector current are high enough, and if the TUT turn-off time is fast enough, the TUT will go into a collector avalanche mode, clamping the voltage at V_{CEX}(sus). As stated earlier, the energy that a device can withstand in actual reverse-bias avalanche is small for high voltage, high speed transistors; therefore, reverse-bias second breakdown energy (often referred to simply as Es/b for this rating system) is many times specified with open base turn-off or with very high base impedance. This yields very high Es/b compared to hard turn-off conditions–in fact, ratings range from millijoules to joules

and indeed device capability varies by orders of magnitude depending upon conditions. In most cases, the circuit designer is interested in the hard turn-off conditions, under which unclamped Es/b seldom exceeds several millijoules.

FIGURE 5

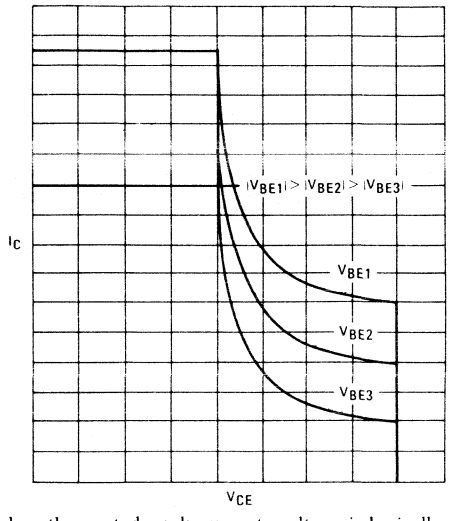
Suggested test circuit for verifying specifications of safe operating area for switching between conduction and cutoff with an unclamped inductive load, and waveforms while switching. (From JEDEC Suggested Standard No. 10, Jan. 1976)



AN ALTERNATIVE–RBSOA

Figure 6 shows a rating system–switching RBSOA–which is applicable to modern switching transistor applications. In form, it is similar to the very familiar forward-bias SOA plot. Collector current is constrained to be equal to

FIGURE 6 – Switching Reverse Biased Safe Operating Area (RBSOA)

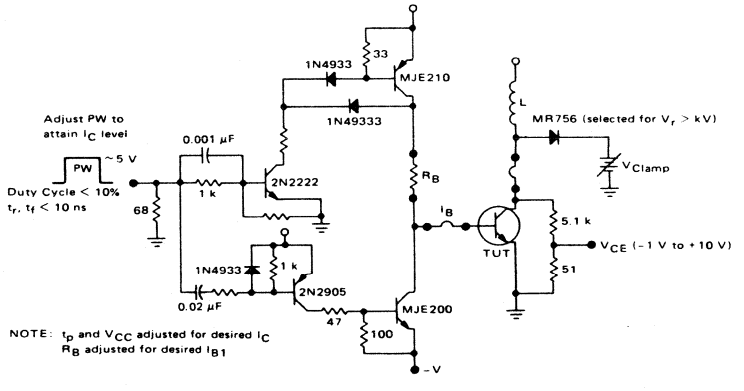


or less than rated peak current, voltage is basically constrained by maximum V_{CEX}, and the high simultaneous V-I portion is constrained by energy-handling capability. Following is a discussion of details of generating this rating, and the effect of variables such as inductance, temperature, turn-off bias, etc.

One circuit which can be used to verify switching RBSOA capability is shown in Figure 7. In this circuit, R_B and the +5 volt supply can be adjusted to set the desired I_{B1}, and V_{CC} and t_p are adjusted for desired I_C. Turn-off is accomplished via the MJE200 connected to -V. I_{B2} is determined by the TUT; if controlled I_{B2} is desired, resistance can be added to the turn-off circuit.

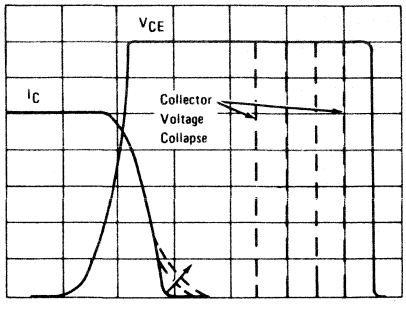
The collector circuit consists of V_{CC}, inductor L and a clamp circuit comprised of the MR756 connected to a clamping supply. To profile switching RBSOA of a device, one can either set V_{Clamp} and vary I_C, or fix I_C and vary V_{Clamp}, in each case detecting failure or onset of failure.

FIGURE 7 – Switching RBSOA Test Circuit (Clamped Inductive Testing)



Some devices "serve notice" just prior to breakdown, by exhibiting an increase of collector current near the tail end of on-time, as shown in Figure 8. If voltage or current is increased beyond this point, breakdown occurs and collector voltage collapses. This is usually destructive.

FIGURE 8 – Onset of RBSOA Failure



Switching RBSOA for a high voltage, high current discrete device is shown in Figure 9. The sharp-cornered "L"-shaped area shows the specified RBSOA for $V_{BE(off)} \leq 5$ volts per the data sheet. Actual profiled curves for a typical device are also shown for $V_{BE(off)}$ = 3 volts and 9 volts. Notice that RBSOA capability increases for increased $V_{BE(off)}$.

FIGURE 9 – High Current Discrete RBSOA

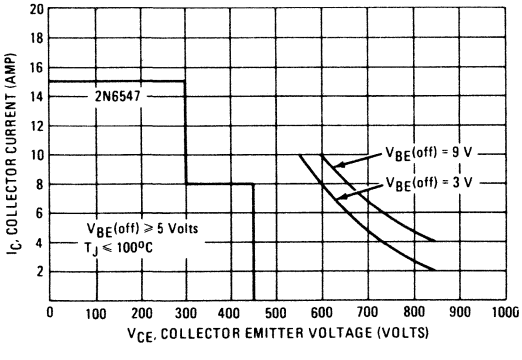


Figure 10 shows specified switching RBSOA for two high voltage, moderate current discrete devices. Below BV_{CEO}, RBSOA is not dependent on off-bias and the safe area is limited by the maximum I_C rating. Above BV_{CEO}, the collector current must be derated as shown and is very dependent upon off-bias. The higher the bias, the greater the safe area.

FIGURE 10 – Moderate Current Discrete RBSOA

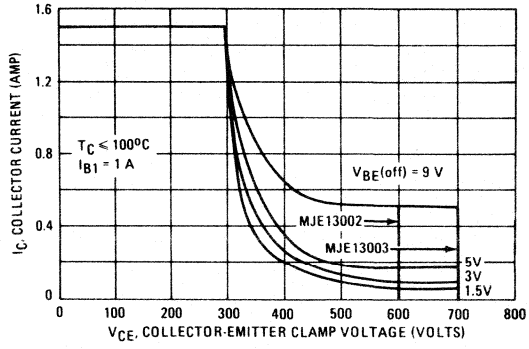
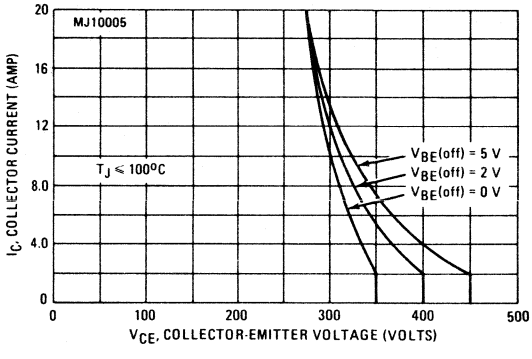


Figure 11 shows the specified RBSOA for a high voltage, high current Darlington. Current is constrained to maximum continuous collector current. In the energy limited region, capability is again seen to increase as $V_{BE(off)}$ is increased.

FIGURE 11 – High Current Darlington RBSOA



The fact that the shape of the specified RBSOA curves differs so much between devices in these examples is attributable to the evolution of rating technique as knowledge of device behavior has increased.

EFFECT OF VARIABLES

To understand how RBSOA applies for differing operating conditions, the effect of several key variables must be examined. First, what is the effect of inductance, and, therefore, load line? Most turn-off load lines lie in the range between pure resistance and pure inductance. It was noted that worst-case stress is imposed upon the device by pure inductive loads. Adding resistance to a given inductor decreases stress and is safe so long as the load line is maintained within the rated RBSOA.

Tests have shown that the inductance value has no measurable effect on RBSOA. For very low values, the collector load line "droops", as the voltage E = L(di/dt)

rises slowly, controlled by di/dt or current fall time dt of the device. At high inductance values, collector voltage quickly rises to V_{Clamp} at turn-off, but the stress on the device remains essentially unchanged as inductance is further increased, since the inductive energy is transferred to the clamping circuit as soon as the device turns off. This is representative of most circuit load line clamping or shaping techniques except, perhaps, those which turn the device back on at a given voltage such as utilization of a collector-base zener. This is a special case which combines both reverse- and forward-bias stresses, and is not within the scope of this discussion.

A second very important factor is the effect of temperature. Data taken to date indicates that RBSOA is relatively unaffected by temperature at high currents, but there does appear to be a definite decrease in RBSOA with increasing temperature at high voltages and low currents. Obviously, in rating a given device, the range of temperature over which RBSOA is guaranteed should be specified.

$V_{BE}(off)$, having a strong effect on storage time and switching losses, is also important to the designer; therefore, its effect on RBSOA is of interest. For the devices studied and reported upon, RBSOA always increased as $V_{BE}(off)$ was increased. It must be remembered, however, that device avalanche was purposely avoided, that is, clamped inductive rather than unclamped inductive tests were run. In avalanche, a device can generally handle more energy at lower $V_{BE}(off)$. This latter case is not considered to be revelant since operation of a device without the protection of either clamp diodes or snubbers is not recommended.

As a final note to the effect of $V_{BE}(off)$: The data reported was restricted to $V_{BE}(off) < V_{EBO}$, that is, in no case was the emitter-base junction avalanched. It is well known that turn-off switching times can be decreased by avalanching the emitter-base junction,[1,2] particularly in the case of Darlingtons without internal speed-up diodes. A form of this technique has been employed in television deflection applications with success—extending it for use in other switching applications is under consideration at present.

To complete the study of variables, the effect of I_{B1} on RBSOA was examined, and no measurable effect was noted. This included overdrive to the point of $I_{B1} = I_C$, and underdrive to the point where device saturation was just maintained.

CONCLUSION

The rating system offered—switching RBSOA—is believed to be pertinent for most switching applications, and it appears to be practical for transistor manufacturers to implement. With the assistance of this rating, the circuit designer can use one or more of several techniques to assure that his turn-off load line is constrained to be within rated RBSOA.

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AN-719
Application Note

A NEW APPROACH TO SWITCHING REGULATORS

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Senior Applications Engineer

This article describes a 24-Volt, 3-Ampere switching mode supply. It operates at 20 kHz from a 120 Vac line with an overall efficiency of 70%. New techniques are used to shape the load line. The control circuit uses a quad comparator and an opto coupler and features short circuit protection.

MOTOROLA *Semiconductor Products Inc.*

A NEW APPROACH TO SWITCHING REGULATORS

INTRODUCTION

The function of a switching regulator is to convert an unregulated dc input to a regulated dc output. The method used to accomplish this function differs dramatically from the conventional series pass regulators. In a switching regulator, the power transistor is used in a switching mode rather than a linear mode. Efficiencies are usually 70% or better which is about double that of the series pass regulator. High-frequency switching regulators offer considerable weight and size reductions and better efficiency at high power over conventional 60 Hz transformer-coupled, series regulated power supplies.

However, a debate continues on the value of switching type supplies as contrasted with conventional series pass regulators. One argument, frequently advanced when discussing switching regulators, is that the electro-magnetic interference (EMI) problems overcome most of the gains in efficiency. Eliminating high-frequency transients, not present in the linear case, adds a new dimension to the design of switching regulators. Controlling this undesired output actually requires very little bulk weight. Basically the necessary techniques come from good RF practice. Layout and lead length play significant roles when designing effective switching circuits.

EMI can be reduced to acceptable levels giving compact, fast and efficient control of power. Switching regulators have found wide use in aerospace and portable applications where power is expensive. Low loss ferrite cores for transformers and chokes, the use of high permeability magnetic alloys for shielding, and the wide range of miniature semiconductor and IC devices for the switching and regulation circuitry have contributed to the success of switching type supplies. The block diagram of a switching regulator is shown in Figure 1. This circuit regulates by switching the series transistor to either the ON or OFF condition, the duty cycle determining the average dc output. Duty cycle is adjusted in accordance with a feedback proportional to the difference between the dc output and a reference voltage.

Switching is usually a constant frequency just above the audible range (20 kHz typical), although some varieties show variable frequency with changing line and load. Higher frequencies are generally less efficient since transistor switching losses and ferrite core losses increase. Low frequency unibase transistors (f_T-200 kHz) are sufficient for series pass regulators; switching regulators must use epibase and triple diffused devices (f_T-4 MHz) to operate efficiently. For the ultimate in efficiency, even higher frequency annular and double diffused devices can be used, ($f_T > 30$ MHz). Darlington transistors are also used in these switching mode supplies; they can provide an overall gain in efficiency through lower base drive requirements even though their saturation voltages are higher than single chip devices.

A fast recovery rectifier or Schottky barrier diode is used as the free wheeling clamp diode to keep the switching transistor load line within SOA limits and to increase efficiency at these frequencies. Other products used in these supplies are shown in Table 1 below.

TABLE 1
Semiconductors Used in Switching Regulators

	CONTROL IC's	
POWER DEVICES	DIGITAL	LINEAR
Power Transistors	Gates Flip-Flops	Op Amps Comparators
Rectifiers	Monostable Multivibrator	Timers Regulators

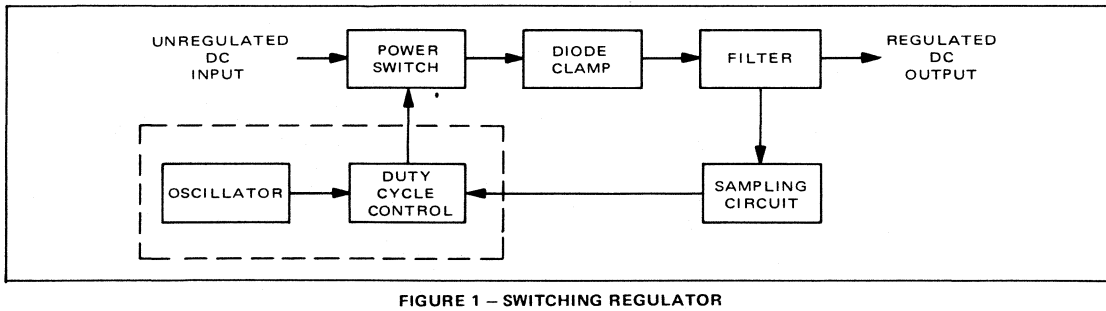


FIGURE 1 – SWITCHING REGULATOR

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

TYPICAL CIRCUITS

Various circuit configurations have been used in switching regulator designs. All have the following common elements:

1. Switching transistor
2. Clamp diode
3. LC filter
4. Logic or control block.

Representative circuits are shown in Figure 2. It should be noted that none of these circuits offers isolation between the line and load. (However, the one transistor design highlights simplicity and economy.) It is usually desirable to have at least one line in common with the input and output to reduce ground loops. The one line approach also determines whether the output voltage will be considered positive or negative. However, by definition this is academic since most circuits will operate from either supply since the input and output grounds are usually isolated. This is suitable for the most general use of switching regulators which power industrial controls and other logic circuits. In circuits 2(a) and 2(b) the logic operates from the load voltage. These circuits are not self-starting and provisions must be made to operate from the line during starting and short circuits. In circuits (c) and (d) the logic operates continuously from the line and is isolated from the load. The sense and feedback elements must be electrically isolated for this reason. An opto coupler or an equivalent device is ideal for this purpose.

Circuits (b) and (d) are generally used in line operated supplies because economical high voltage NPN transistors are available whereas PNP types are not. Of these two, circuit (d) is the most popular because the logic is tied directly to the series switch, and switching can be much more efficient.

Driver transformers are also used in many designs to interface between the logic and switching transistor. In such a case, there are no circuit constraints on the transistor type, and it may be an NPN or PNP device.

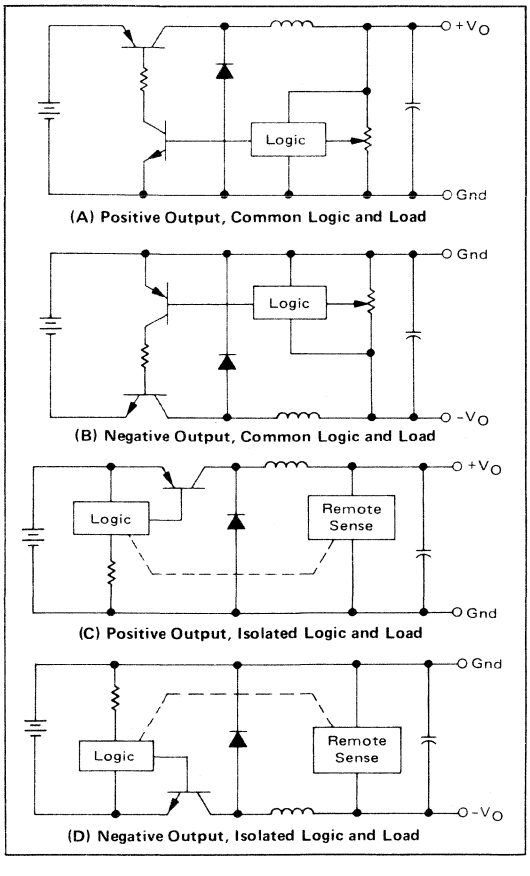


FIGURE 2 – SWITCHING REGULATOR CIRCUIT VARIATIONS

THEORY OF OPERATION

The high efficiency of switching regulators is a result of operating the series transistor in a switching mode. When the transistor is switched ON, full input voltage is applied to the LC filter; when it is OFF, the input voltage is zero. With the transistor turned on and off for equal amounts of time (50% duty cycle), the dc load voltage will be half the input voltage. The output voltage (V_O) will always equal the input voltage (V_{in}) times the duty cycle (D) as follows:

$$V_O = D\,V_{in}$$

Varying the duty cycle will therefore compensate for changes in the input voltage; this technique is used to obtain a regulated output voltage.

Repetitive operation of the switching transistors at a fixed duty cycle produces the steady state waveforms shown in Figure 3. With the switch closed, inductor current (I_L) flows from the input voltage (V_{in}) to the load. The difference between the input and output voltage (V_{in}-V_O) is applied across the inductor. This causes I_L to increase during this time.

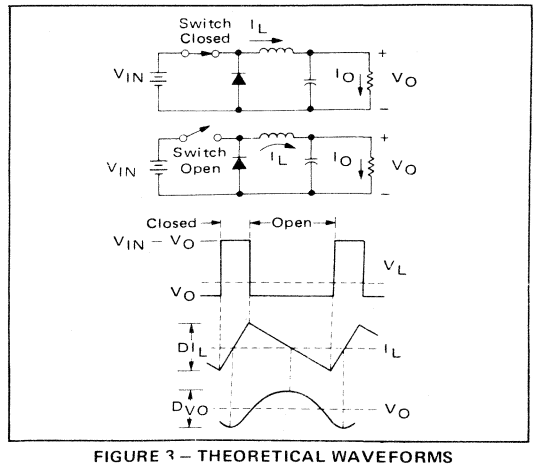


FIGURE 3 – THEORETICAL WAVEFORMS

With the switch open, stored energy in the inductor forces IL to continue to flow to the load and return through the free wheeling diode. The inductor voltage is now reversed and is approximately equal to V_O. During this time, IL decreases.

The average current through the inductor equals the load current. Since the capacitor keeps V_O constant, the load current (I_O) will also be constant. When IL increases above I_O, the capacitor will charge and when IL drops below I_O, the capacitor will discharge. These waveform inflection points are indicated in Figure 3. The end results of steady state operation are as follows:

1. The average inductor voltage will be zero but a wide variation from (V_{in}-V_O) to V_O will be experienced.
2. The dc current flowing through the inductor will equal the load current. A small amount of sawtooth ripple will also be present.
3. The dc voltage on the capacitor is equal to the load voltage. A small amount of ripple (quasi-sine wave) will also be present here.

Transient operation must consider changes in V_{in} and I_O. Input voltage changes are automatically compensated for by appropriate duty cycle variations in a closed loop system. Input regulation and ripple rejection are dependent on loop gain but are generally adequate as indicated later.

Changes in I_O are more difficult to compensate for and load transient response is generally poor. Changes in I_O are compensated for with temporary duty cycle changes. For example, a change in load from half to full will result in the following:

1. Duty cycle increases to its maximum (the transistor may just stay ON).
2. The inductor current takes many cycles to increase to its new dc level.
3. Duty cycle returns to its original value.

DESIGN

The circuit in this article was designed to supply a regulated 24 Vdc output from a 120 Vac line. Typical load variations are from 1.5 to 3 Amperes and the line from 100 to 140 Vac. In addition to providing good regulation, the circuit is efficient and has short circuit protection. The design of this regulator utilized the functional blocks shown in Figure 4. Since it is line operated, an input rectifier and filter are required to convert the incoming ac to dc. The power switch uses a high voltage transistor operating at a switching frequency of 20 kHz to control the pulse width of the voltage applied to the LC output filter.

The control portion of this design uses an oscillator, a "one shot" comparator, and a feedback block which also includes an opto coupler. The oscillator generates the fixed frequency of operation. The resulting output forms a clock pulse for the comparator. The second input to the comparator is derived from the feedback amplifier. This amplifier senses the output voltage and controls the duty cycle of the "one shot" comparator. The output of the comparator is then fed directly to the power switch to complete the loop. Additional details regarding the design and operation of these blocks are provided in the following sections.

INPUT RECTIFIER AND FILTER

The input rectifier and filter consists of a bridge rectifier and filter capacitor. To improve the efficiency series limiting resistance is not specifically used; starting current surges are higher because of this and a 12 Ampere rectifier is therefore required even though the average output current is less than one Ampere. A 150 μF capacitor was used to limit the input ripple to under 20 V peak-to-peak with a full load.

OUTPUT FILTER

The output filter is also quite simple as shown in Figure 5. Calculations of the values for L and C are more involved but quite conventional. The appropriate design information is also shown in Figure 5. To design the filter

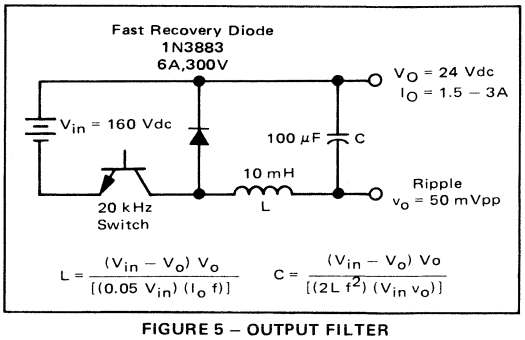


FIGURE 5 – OUTPUT FILTER AND DESIGN SPECIFICATIONS

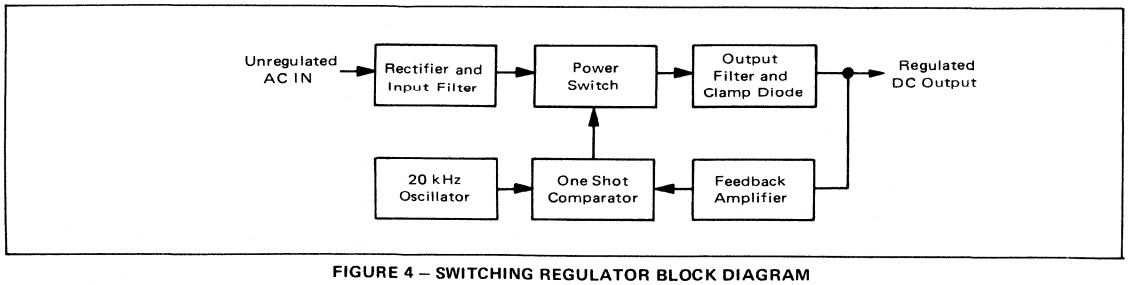


FIGURE 4 – SWITCHING REGULATOR BLOCK DIAGRAM

approximate values for the following must be known.

1. Input voltage, V_{in}
2. Output voltage, V_O
3. Frequency, f
4. Output current, I_O (and range)
5. Output ripple v_o (peak-to-peak)

A general "rule of thumb" is to restrict current variations in the choke (L) to 10% of the load current. Variations are restricted to 5% in this case since a regulation range of load current of at least a 2 to 1 ratio is required. Smaller values of inductance could be used to improve transient response as long as the choke does not run dry (allowing choke current to drop to zero during each alternation). A value for L can be found using:(1)

$$L = \frac{(V_{in} - V_O)\,V_O}{0.05\,I_O\,V_{in}\,f} \text{ (for } \Delta I_L = 5\%\, I_O)$$

$$L = \frac{(160 - 24)\,24}{0.05\,(3)\,160\,(20\text{ k})} = 6.8 \text{ mH}.$$

The nearest standard choke available in this design case was a 10 mH air core choke. A standard Triad C 58U or an equivalent custom designed ferrite core may be used if a small air gap is provided in the latter case to prevent saturation at currents up to 5 Amperes dc; this is the short circuit limit.

To keep v_o below 50 mV, a value for C can be found using:(1)

$$C = \frac{(V_{in} - V_O)\,V_O}{(2L)\,f^2\,V_{in}\,(v_o)},$$

$$C = \frac{(160 - 24)\,24}{2\,(10\text{ mH})\,(20\text{ kHz})^2\,160\,(50\text{ mV})} = 51\ \mu\text{F}.$$

The dissipation factor of most electrolytic capacitors is too high for this application; because of this, two 50 μF capacitors were used to obtain the desired performance. A more expensive stacked foil electrolytic or solid tantulum capacitor may also be used. High frequency bypass capacitors and an additional high frequency LC filter are used in similar designs to prevent switching spikes from reaching the load. This approach was not required in this design because of load line shaping which will be described later. Operation at 20 kHz requires a fast recovery diode. A 6 Ampere, 300 Volt, 1N3883 was chosen to handle up to 5 Ampere free-wheeling currents and peak line voltage.

POWER SWITCH

The power switch includes a push-pull driver which provides the interface between the integrated circuit drive signal and the actual power switch, a high voltage NPN power transistor. Power to this stage and the logic is provided by a 12 Volt step-down transformer. The IC logic is in the position indicated earlier in the discussion of Figure 2(d). The main advantage of this layout is that the logic ground is common to the emitter of the power switch. Because of this, conventional speed-up capacitors can be used to couple the drive signal to the base terminal to improve switching speeds. This is especially important in this particular design. Because of the large step-down in voltage and the high switching frequency, ON times will be very short. The minimum switching time is found using the peak V_{in} of 200 V (high line) instead of 160 V.

The earlier discussion of switching regulator theory indicated the duty cycle would be approximately:

$$D = V_O/V_{in} = 24/200 = 12\%.$$

At 20 kHz, the ON-time will be 12% of 50 microseconds or approximately 6 μsec. With simple resistive termination of the base emitter junction, storage time alone can be as much as 10 μsec. For this reason, a special drive circuit and a high frequency 250 volt, 8 Ampere, 2N6306 power transistor were required for this application. This device has good saturation voltages at 3 Amperes with excellent switching speeds. The drive circuit shown in Figure 6 does the job of switching the 2N6306 at 3 Amperes and 20 kHz from the 120 Vac line. To do this, two unique design innovations were used.

1. An artificial negative bias supply was created from the single positive supply available to improve fall time.
2. Current limiting was added to the base current to limit overdrive and reduce storage time.

Turn-off of the power switch is accomplished by forcing the IC to a logic low. This turns on the 2N6034 and creates a path for reverse base current. The 10 μF capacitor which is used as a reverse bias supply then removes stored base charge from the 2N6306 and forces it to turn-off. Reverse base current flows for about 2 μsec. The diodes are added to prevent the capacitor from discharging into the 10 ohm resistor once the base is

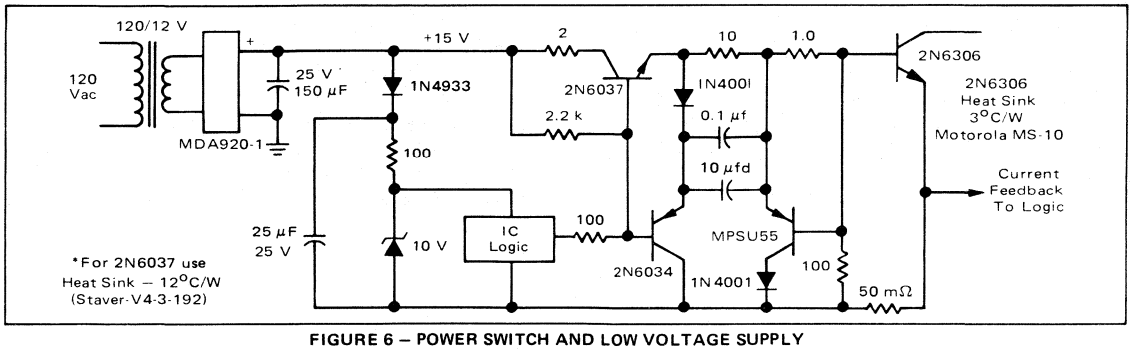
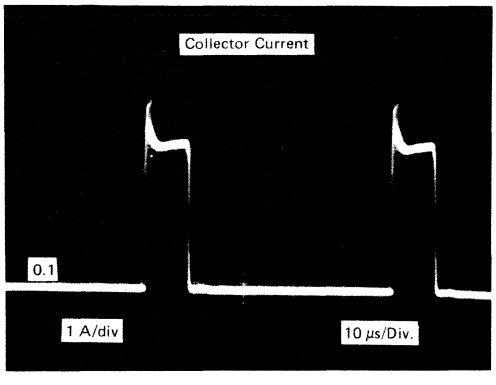


FIGURE 6 – POWER SWITCH AND LOW VOLTAGE SUPPLY

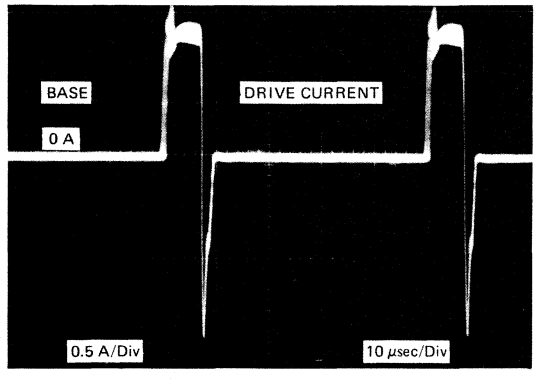
cleared. This minimizes the amount of charge that must be replaced during each alternation.

When the logic goes high, the 2N6037 turns on and forward base current flows through the 10 ohm resistor turning on the 2N6306. The 2N6034 and 2N6037 are both plastic Darlington power transistors. However, the 2N6037 should be used with an appropriate heat sink since it supplies both forward base drive for the device and recharge current for the 10 μF capacitor. With this high gain Darlington, recharge takes approximately 2 μsec. Most of the recharge current is bypassed around the 2N6306 base by the MPSU55; this device limits forward base drive to about 1 Ampere. This particular drive level was chosen to keep storage time low and at the same time ensures that the 2N6306 will remain saturated even under short circuit conditions. The actual operation waveforms of the power switch and drive circuit are shown in Figures 7 and 8, respectively.

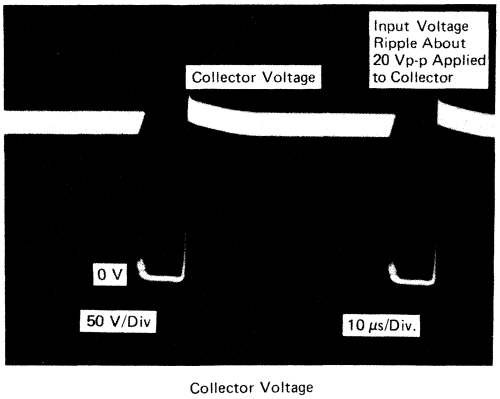


Collector Output Current

Both Measured
With 120 Vrms Input
and Output
24 V 3 A



Measured
With 120 Vrms Input
and Output
24 V 3 A



Collector Voltage

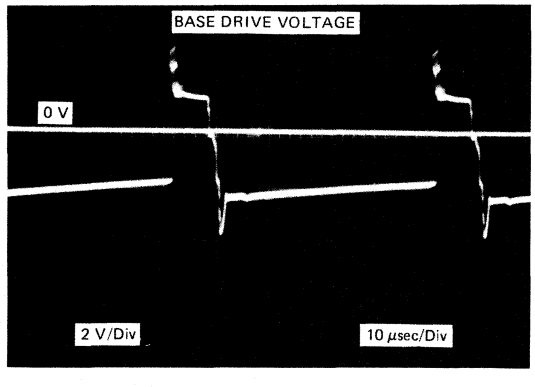


FIGURE 7 – POWER SWITCH WAVEFORMS

FIGURE 8 – DRIVE CIRCUIT WAVEFORMS

FEEDBACK AMPLIFIER

Because the load ground and logic ground are isolated, it is necessary to use a 4N28 opto coupler for the feedback amplifier. The schematic is shown in Figure 9. The 1N5290 is a 0.5 mA current limiting diode and causes the voltage drop across the 39 k sense resistor to remain fixed at about 20 V. This unique design causes changes in load voltage to appear directly at the base of the 2N5088 and results in sensing without attenuation. Load voltage changes produce a linear change in LED current and a proportional voltage change at the sense terminal of the logic circuitry.

The 0.5 mA diode is considered to be a zero temperature coefficient unit. Also, the output level of the opto coupler of 1 mA is chosen to minimize its temperature dependence. A photo Darlington coupler was tried for increased gain; however, it introduced low frequency oscillations because of its slow speed and thus, could not be used.

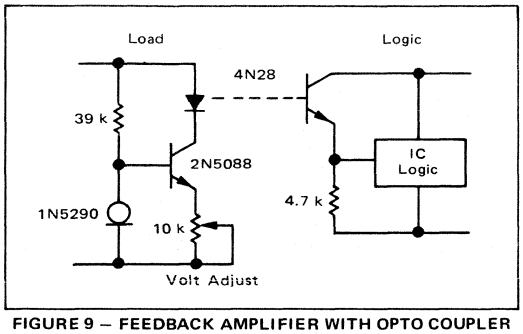


FIGURE 9 – FEEDBACK AMPLIFIER WITH OPTO COUPLER

OSCILLATOR, COMPARATOR, AND CURRENT-LIMIT CIRCUITS

In addition to the feedback amplifier, the control circuit for this switching regulator also requires an oscillator, comparator, and current limiter as part of its control circuitry. These last three functions are all made possible by the use of a single IC chip, the MC3302 quad comparator.

The schematic diagram of the oscillator, comparator, and current limit circuits is shown in Figure 10. Comparator 1 is used as a 20 kHz oscillator. It supplies a sawtooth output which operates between the voltage limits defined by the 100 k positive feedback resistor and the logic supply voltage. The second comparator takes this output and compares it to the feedback signal to produce a variable duty cycle output pulse for the power switch. The timing diagram in Figure 11 illustrates how this happens. In normal operation, the feedback signal is a constant dc voltage which is between the limits of the oscillator sawtooth. When the sawtooth exceeds the feedback threshold, comparator 2 switches to a high output level. The comparator is reset when the sawtooth drops back below the feedback signal. In actual practice, the comparator output pulse is delayed by 2 μsec because of internal propagation time. This phase shift has no effect upon regulation. Variations in the output and feedback signals will still produce compensated changes in the power switch pulse width.

The remaining two comparators in Figure 10 are used to initiate current limiting action. Comparator 3 senses the over current and triggers comparator 4 which is used as a "one shot" multivibrator. The zero input voltage threshold is derived from the reference voltage of 0.24 V from comparator 3. Power dissipation in the 50 mΩ sense resistor is therefore kept at a minimum. With this combination of reference voltage and current resistor,

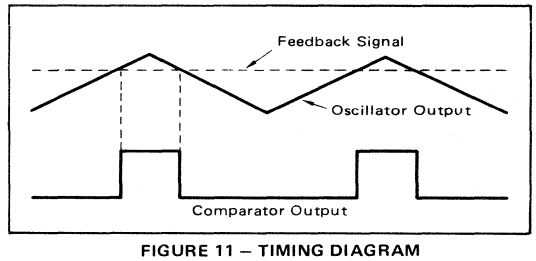


FIGURE 11 – TIMING DIAGRAM

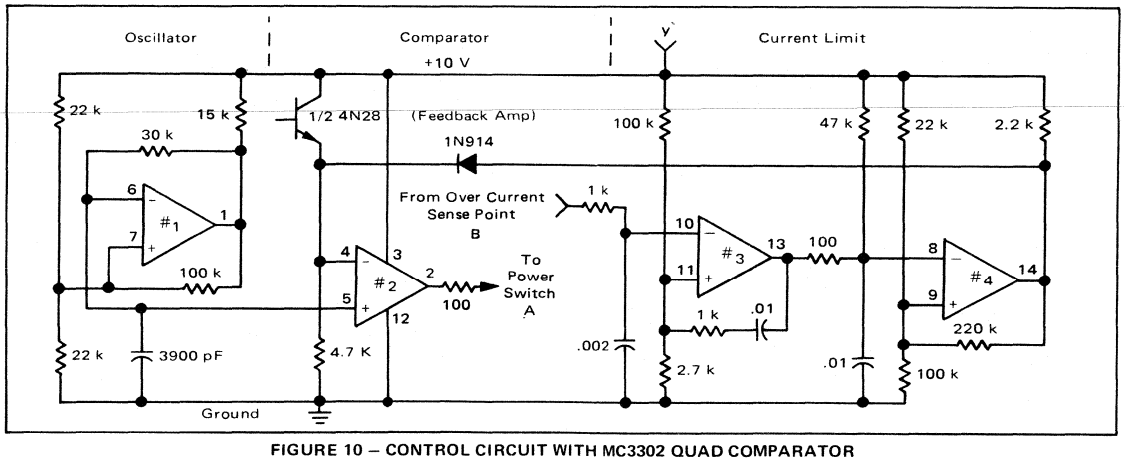


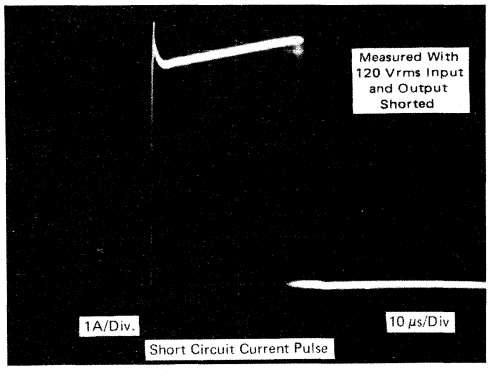
FIGURE 10 – CONTROL CIRCUIT WITH MC3302 QUAD COMPARATOR

current limiting occurs at approximately 4 Amperes. When this level is reached (due to overload or short circuit), the "one shot" capacitor is discharged and a millisecond time interval is initiated. Positive ac feedback is used to ensure that this capacitor does completely reset. An RC filter is also provided to prevent inductive transients from accidentally shutting the regulator down.

While the "one shot" device is recharging, the output of comparator 4 remains high to simulate excessive output voltage at this feedback sense point (comparator 2); drive pulses are completely inhibited during this down time. Comparator 4 is reset and drive pulses continue when the "one shot" device reaches an 8 volt threshold. Positive feedback to this reference prevents circuit oscillations as the threshold is approached. If the short is removed, the switching regulator will automatically reset into a full load. If the short remains, operation (with 30 μs 4 Ampere pulse) continues at an audible 1 kHz rate set by the "one shot" multivibrator. The short circuit collector currents are shown in Figure 12.

LOAD LINE SHAPING

Load line shaping can be used to improve reliability and reduce EMI.[1][2] Shaping is basically done by using reactive elements to absorb what would normally be switching losses. Because resistors are used to dissipate the power stored in these reactive elements, there is no appreciable improvement in overall circuit efficiency. However, because safe operating area (SOA) stresses on the switching transistor are reduced, cooler and more reliable operation results. Illustrations of the load line before and after are shown in Figure 13 and 14. A secondary but very desirable effect can also be noticed at the output. Switching spikes, due to the abrupt recovery of the fast recovery diode and fast switching speed of the power transistors, are reduced from a 0.6 Volt to a 0.1 Volt peak. Because



Short Circuit Current
Measured at the Collector
with Current Probe

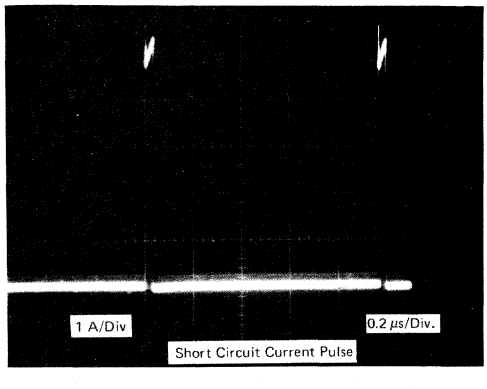
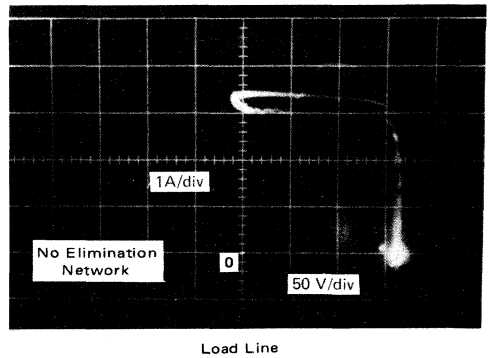


FIGURE 12 – SHORT CIRCUIT CURRENTS



Load Line

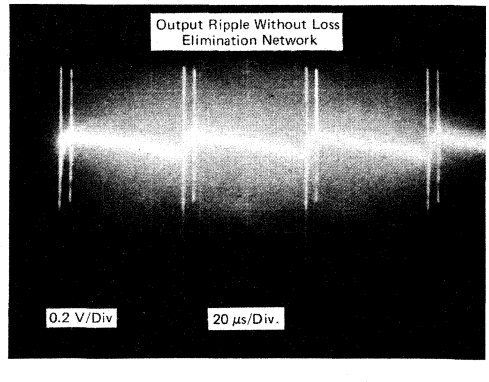


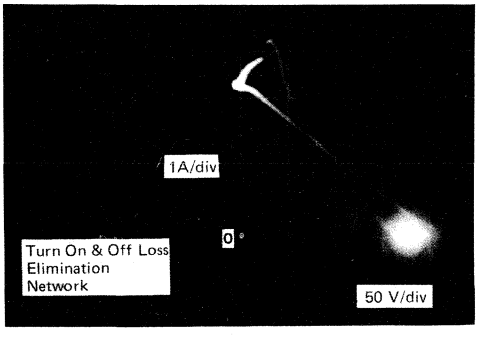
FIGURE 13 – BEFORE LOAD LINE SHAPING

these spikes are reduced to acceptable levels, additional high frequency output filters are not required. Calculations of the power losses reveal the following:

TABLE 2 – Switching Power Losses (Watts)

Power	Transistor Only	Transistor with Snubber		
		Transistor	Snubber	Total
turn on	2.4	0.8	1.8	2.6
turn off	3.0	1.0	1.9	2.9
Total	5.4	1.8	3.7	5.4

The calculations show the dramatic improvement. The remaining power loss of approximately 0.4 watt, due to base and collector saturation voltages of 1.0 and 0.5 Volt respectively, is unaffected by these changes.



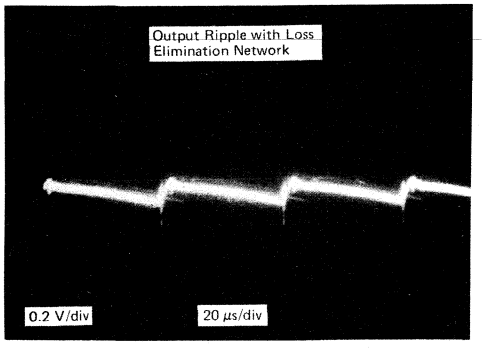


FIGURE 14 – AFTER LOAD LINE SHAPING

The actual loss elimination networks used in this design are shown in Figure 15 along with the design equations. During turn-on the inductor (L_X) must block the input voltage (V_{in}) during the transistor turn-on time (t_r). Diode current (I_O) which has been flowing in the free-wheeling diode and inductor prior to this time, will decrease to zero. Measured current rise and fall times on the transistor are 0.3 and 0.4 μsec respectively. Therefore:

$$L_X = \frac{V_{in}\, t_r}{I_O} = \frac{160\ (0.3\ \mu\text{sec})}{3} = 16\ \mu\text{H}.$$

The value used was 20 μH. The inductor should not saturate at rated load to be effective and current must build back up to I_O during the free-wheeling time of 40 μsec. The resulting inductance/resistance (L/R) time constant of 4 μsec ensures this condition. Therefore:

$$R_L = L_X/\gamma = 20/4 = 5\ \Omega \text{ and}$$

$$P_R = \tfrac{1}{2}LI^2f = \tfrac{1}{2} \times 20\ \mu \times (3)^2 \times 20\ \text{k} = 1.8\ \text{W}$$

Using a 4.7 ohm resistor was practical since the collector voltage overshoot was limited to approximately 15 V.

During turn-off, the capacitor (C_X) must supply load current (I_O) while the transistor is turning OFF (t_f). The capacitor will have charged to the input voltage and will now discharge to zero. Therefore:

$$C_X = \frac{I_O\, t_f}{V_{in}} = \frac{3\ (0.4\ \mu\text{sec})}{160} = 7500\ \text{pF}.$$

Because of parasitic circuit capacitance, only 4700 pF is required. The capacitor must recharge during the on-time of the transistor to 10 μsec. The RC time constant of 1.0 μsec is chosen to ensure this condition. Therefore:

$$R_C = \tau/C_X = 1\ \mu\text{sec}/4700\ \text{pF} = 210\ \Omega.$$

and

$$P_R = \tfrac{1}{2}CV^2f = \tfrac{1}{2} \times 7500\ \text{pF} \times (160)^2 \times 20\ \text{k} = 1.9\ \text{W}$$

Using a 150 ohm resistor is practical because the collector current overshoot is limited to approximately 1 Ampere. Thus, parasitic capacitance has no effect on this recharge time. In actual practice, the values of L_X and C_X may be empirically adjusted to obtain the desired load line effect.

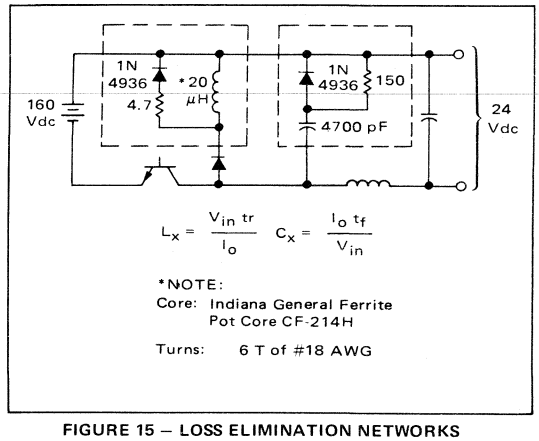


FIGURE 15 – LOSS ELIMINATION NETWORKS

CONCLUSION

This article has discussed the circuitry used to implement a line operated switching regulator as shown in Figure 16. The semiconductor components highlighted in this design include:

1. A 2N6306 power transistor. This device switches 3 Amperes from 200 Volt and is fast enough to handle the 20 kHz square waves generated by the design.
2. The 2N6034 and 2N6037 complementary power Darlingtons. These devices switch up to 3 Amperes and provide a single stage interface between the IC logic and the 2N6306.
3. An 4N28 opto coupler. This device provides an electrically isolated feedback signal from the load to the IC logic. It is fast enough to operate in a 20 kHz switching frequency loop.
4. The MC3302P quad comparator. The comparator itself provides all the logic functions necessary for voltage regulation and current limiting in a single package.

Several unique design innovations have been presented. The most significant design highlight is reactive load line shaping. By using techniques from a Bell Laboratories report,[1][2] switching power losses are reduced by a factor of 3. The same reactive components are also responsible for a 6 to 1 reduction in output noise.

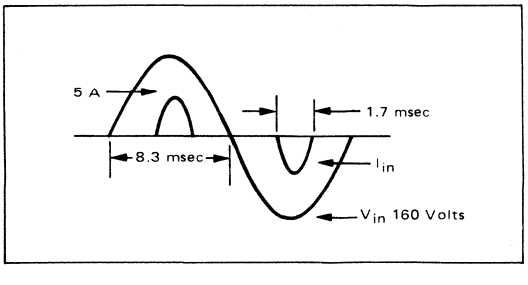
The ripple content of the output voltage (24 Volts dc) is shown in Figure 17. The 60 Hertz ripple frequency has been reduced significantly by a factor of 100 to yield a 200 mV peak-to-peak maximum ripple component. The ripple factor is approximately 10 mV per volt. The 20 kHz output ripple is only 50 mV peak-to-peak; this is less than 0.2% of the output voltage.

The output voltage variations due to line and load changes are as follows:

TABLE 3 – Line versus Load Variation Comparisons

Regulation	Conditions	ΔV_O	Percent Regulation
Load	I_o = 1.5 to 3 Ampere V_{in} = 120 Volts ac	0.2 V	0.8%
Line	V_{in} = 100 to 140 Volts ac I_o = 3 Amperes	0.7 V	3%

The efficiency is measured at rated load (24 Volts, 3 Amperes) with 120 Volt input. The oscilloscope display of input voltage and current is shown below:



The input voltage varied from 150 to 170 Volts during the power pulse but is considered constant at 160 Volts. The current pulse is essentially a sine wave. This allows the use of a peak-to-peak comparison on an average ratio of $2/\pi$ in calculating the total average current and input power as shown:

$$P_{in} = E_p \quad \frac{2}{\pi} I_p \quad \frac{\text{Pulse Width}}{\text{Period}}$$

$$= (160\text{ V})\ \frac{2}{\pi} \quad (5\text{ A})\ \frac{1.7\text{ ms}}{8.3\text{ ms}} = 103 \text{ watts.}$$

The overall efficiency can then be found using:

$$\text{Efficiency } (\%) = \frac{P_o}{P_{in}}\ 100$$

$$= \frac{(24\text{ V})\ (3\text{ A})}{103}\ 100 = 70\%$$

As was indicated earlier, this is about twice that of a series-pass regulator.

This particular line operated switching regulator has many advantages over a conventional series-pass design; since the efficiency is high, less heat sinking is required. Because the switching regulator operates directly from the line, the need for a 60 Hertz transformer is eliminated. The size and weight reductions are therefore quite significant and are becoming increasingly important in many applications. The main drawback of most uncompensated switching regulators is noise. This drawback can be eliminated by using load line shaping. Load line shaping not only reduces the high frequency electrical noise associated with switching mode supplies but also improves the reliability of the power stage. An opto coupler is used in the 20 kHz feedback loop to maintain a high degree of line and load isolation. A single package quad comparator is used to reduce component quantity for both pulse width control and short circuit protection.

This article has demonstrated a significant method of designing a regulated switching supply with 70% overall efficiency. The approach describes and illustrates how to decrease component counts and avoid using costly, cumbersome and inefficient transformer-operated industrial power supplies, while providing complete short circuit protection.

The author wishes to acknowledge Paul Fletcher for his assistance in preparing this note.

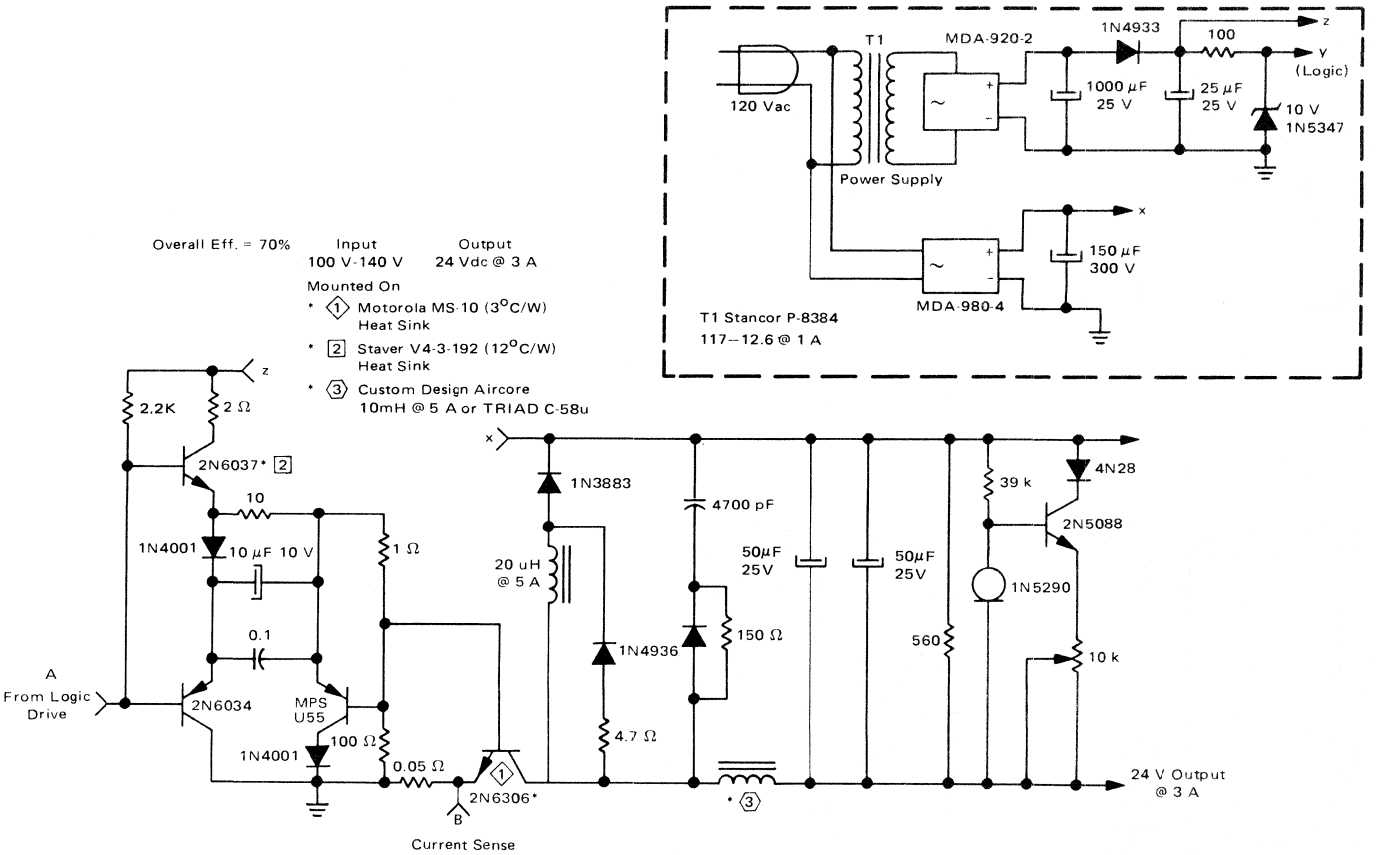
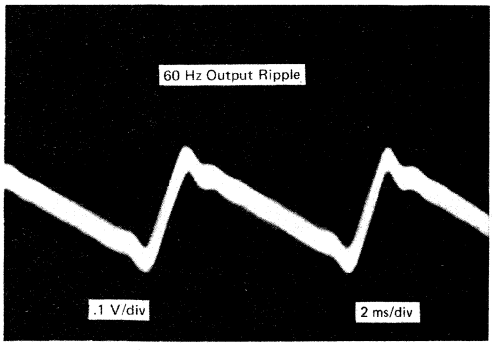


FIGURE 16 – Complete Regulator Schematic (for logic see Figure 10)



NOTE:
Both Measured
With 120 Vrms Input
and Output Ripple with Attendant
20 kHz ripple 24 V at 3 A

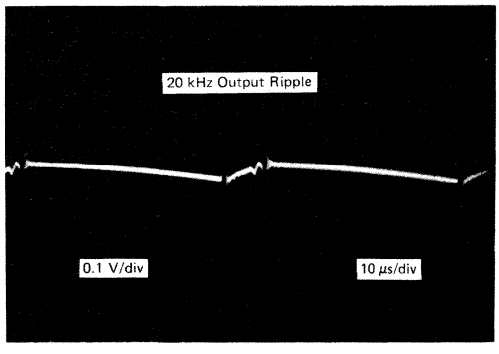


FIGURE 17 – OUTPUT RIPPLE WAVEFORMS

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AN-737A
Application Note

SWITCHED MODE POWER SUPPLIES-HIGHLIGHTING A 5-V, 40-A INVERTER DESIGN

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This application note identifies the features of various regulator circuits that are in use today in AC to DC power supplies. The note also illustrates how these circuits may be used as complementary building blocks in a system design. Primary emphasis is on switched mode regulators because they fill the present need for energy and space savings.

A complete 5-V, 40-A line operated inverter supply is described in detail including design procedures for the magnetic components. The inverter itself is a "state-of-the-art" design which features CMOS logic, high voltage power transistors, Schottky rectifiers and an optoelectronic coupler. It operates with a full load efficiency of 80% at a frequency of 20 kHz.

MOTOROLA Semiconductor Products Inc.

SWITCHED MODE POWER SUPPLIES - HIGHLIGHTING A A 5-V, 40-A INVERTER DESIGN

INTRODUCTION

There are many ways to build a power supply. The linear or "series pass" supply is one that has dominated the market for a long time. A more recent entry, the switched mode power supply, however, is coming of age. It has already replaced the linear regulator in many applications where high efficiency and small size are important considerations. In other cases, it is used in combination with linear regulators to obtain excellent regulation and transient response with improved efficiencies. Because the switched mode supply is now a proven design concept, it is being considered for use in most new designs and has become a very popular topic of conversation among design engineers.

In the first part of this article, the salient features of all types of dc power supplies are identified. A brief outline of several system approaches illustrating the most popular combinations of these circuits is presented. In the second part, the basic switched mode circuits are identified and a design example is presented. The example features a 120 V line operated 200 W inverter with a regulated output capable of supplying 40 A at 5 V.

Linear versus Switched Mode Supplies

Several voltage regulator circuits are available to the power supply designer. The most popular circuits in use today include:

1. Controlled Ferroresonant Transformer
2. SCR Phase Control
3. Linear Regulators
   a. Series
   b. Shunt
4. Switched Mode Regulators
   a. Switching Regulators
   b. Pulse Width Modulated (PWM) Inverters

In this article, switching regulators refer to one-transistor circuits whereas an inverter is considered to contain two transistors operating in a push-pull mode. The significant features of all these circuits are shown in Figure 1. In general, the table reflects typical size, cost, and performance data as found in current literature (magazines, technical brochures, etc.) Because the first three circuits all use bulky 60 Hz transformers for isolation between the line and load, they suffer the common disadvantage of large size. The switched mode regulators, however, operate above audio frequencies and use small 20 kHz power transformers. Because of the present emphasis on energy conservation, efficiency, and small size, the future appears bright for these switching supplies. The ferroresonant and SCR supplies are also making progress on the linear market, they are more efficient, and economical as well. The reason none of these supplies will completely replace the series regulator is also evident. The series regulator still offers the best regulation, ripple rejection, and transient response.

As shown in Figure 2, at the 100 W level, switching supplies cost more to build than series pass supplies. However, as was indicated earlier, they are still used at this power level and lower, when size is more important than cost. If we were to look at the characteristics of larger supplies, we would find that the performance data in Figure 1 remains basically the same. The size and weight numbers would tend to increase proportionally but the cost per watt has a tendency to decrease. Figure 2 offers a specific comparison between inverters and series pass regulators on this. The parts cost covers only the electronic components and heat sinks. Total parts cost is about $1/Watt at this level. Because inverter costs drop faster, they are more economical than series pass regulators at high power levels and cost about the same at the 200 to 300 W level. A couple of years ago, this break-even point was at the 500 W level.

Another advantage of transistor Switched Mode supplies is hold-up time which is better by an order of magnitude

Features	Ferroresonant	SCR	Series	Switching Regulator	Inverter
Major Advantage	Low Cost	Low Cost	Excellent Regulation	Small	Small
Major Disadvantage	Large	Poor Response	Poor Efficiency	Poor Response	Poor Response
*Cost (Electrical Parts)	$15	$15	$20	$25	$30
*Efficiency	80%	80%	30%	70%	70%
*Size (cu. in.)	600	200	300	70	70
*Weight (lbs.)	30	10	20	5	5
Regulation	3%	5%	0.1%	0.1	0.1
Ripple	160 mV	100 mV	5 mV	50 mV	50 mV
Maximum Power	2 kW	None	1 kW	200 W	1 kW
Transient Response	100 ms	100 ms	50 μs	1 ms	500 μs

*Note: These numbers apply to a 100 W supply.

FIGURE 1 – Comparative Features of DC Power Supplies in 1974

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

(20 ms versus 2 ms) due to high voltage energy storage. However, these supplies are more complex and generate more noise. Noise generation is roughly 10 times that of a series pass supply and since more sophisticated control circuitry is required, switches are also more difficult to design.

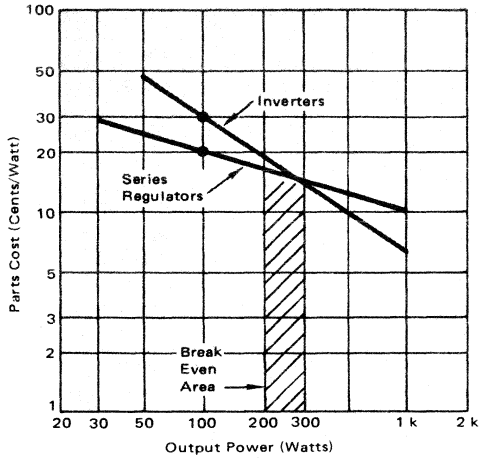


FIGURE 2 – Why Use Switching Supplies?

System Approaches

Now that the features and capabilities of various regulators have been reviewed, it is easier to understand the problem a designer faces in choosing which circuit or combination of circuits to use. The source of power is specified and would not be one of these design problems. When output power is 500 W or less, the single phase 120 V line is generally used. For larger supplies, three-phase power from a 208 V or 220 V source is used because energy storage in filter capacitors is more economical at these higher voltages. Tolerances on line voltage are typically +10% and -30%. Operation beyond these points can be prevented by voltage crowbars and shutdown circuits.

Before reviewing the popular circuit combination, it's well to consider the problem of power distribution. In a large system, such as a medium size TTL computer, up to 4 kW of power may be required at the 5 V level. This power capability may be designed into a large, centrally located supply or distributed in several smaller supplies at the "point of load". In the central supply, large bus bars are used to distribute the low-voltage, high-current power to the various bays and racks within the main frame. Distributed or "point of load" supplies may operate from the ac line or from a high voltage dc bus and supply from 50 to 250 Watts of power. There appears to be a general trend away from the single central supply to smaller distributed supplies at the 200 to 250 W level like the circuit shown in this note. Where a central supply is retained, it is used as a preregulator to power the high voltage bus. A ferroresonant supply is popular here because it also eliminates line transients. Of course, there are still many applications where all the power is for one load and it cannot be split up. In these cases, a single large regulated supply may be used or several small "current limited" supplies may be paralleled to make up the power.

Several possible system approaches to the design of a computer or industrial power supply are shown in Figure 3.[1] In each case there may be a requirement for multiple output voltages. The computer will use 5 V for the logic and 36 V, 48 V, and 100 V supplies for memories, read-

[1] See also reference #4

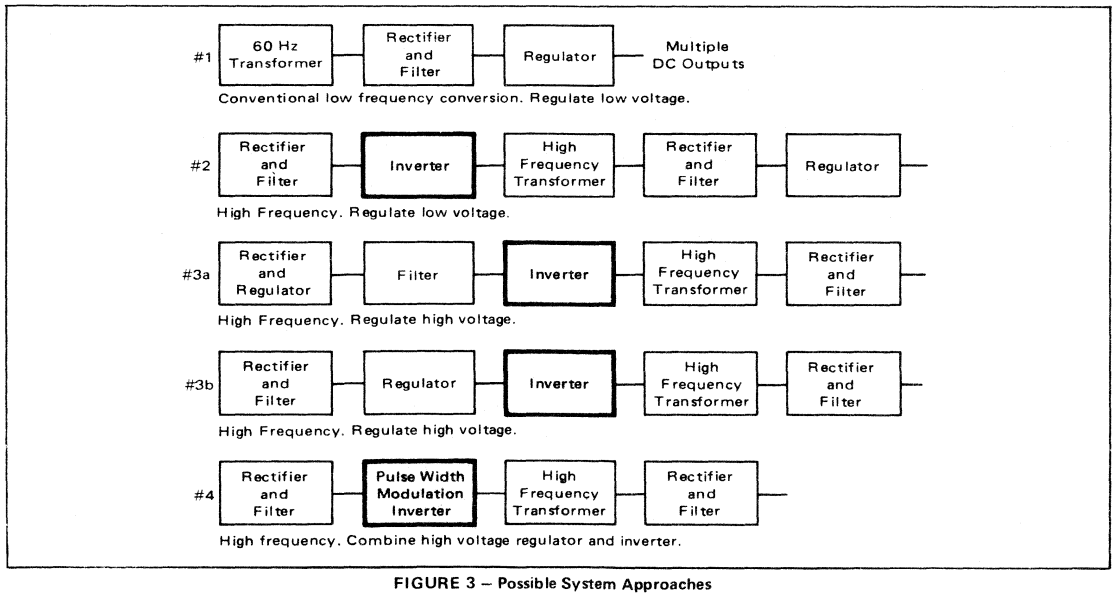


FIGURE 3 – Possible System Approaches

outs and peripheral equipment. Industrial systems generally have logic voltage requirements and may also need ±15 V and 24 V or 48 V for operational amplifiers and relay drivers. The advantages and disadvantages of each system are not too obvious, but can be brought out more clearly by some practical considerations. The first system uses a low frequency conversion technique while the remaining three systems operate at ultrasonic frequencies.

System #1. This is a conventional approach which uses a 60 Hz transformer or ferroresonant transformer to step down the line voltage for the rectifier and regulator circuits. It has been more economical in the past, but is bulky and generates more heat than the high frequency approaches.

System #2. This system uses the same building blocks required of all high frequency regulators but the sequence is varied. The line rectifier is followed by a high-voltage, high-frequency inverter and the regulation is accomplished at the low-voltage, high-current outputs of the inverter transformer. Each output can be individually regulated to provide precise voltage control over wide variations in load. There are two drawbacks to this approach: (1) several low-voltage, high-current regulators are required and (2), the efficiency will be lower than for the remaining approaches which regulate the high-voltage and low-current power.

System #3. This system uses high-voltage regulators to power the inverter which drives the low-voltage rectifiers and filters. The regulator may use SCR's for phase control (#3a) or high voltage transistors in either a linear or switching mode (#3b). Of the two approaches, the SCR may be preferred because of economy. In both this approach and approach #4, only one output can be regulated, usually the 5 V. This is not a serious drawback because line regulation is common to all outputs and slight changes in the memory and peripheral equipment supplies due to load changes are not critical.

System #4. This system is similar to #3 except regulation is accomplished in the inverter circuit by using pulse width modulation (PWM) techniques. It conserves power devices but does require a more elaborate high-current LC output filter. This appears to be the most practical approach because power is handled only once and its regulation is sufficient for most applications.

The inverter circuit common to all the high frequency approaches is the primary means for obtaining small size and higher efficiencies. For this reason, an inverter design is highlighted in the second part of this article. Before proceeding with a discussion of this design, it is worthwhile to discuss the most common switching regulator and inverter circuits in use today.

Switching Regulator Circuits

Single transistor regulators are very popular below 200 W but don't compete well with inverters at higher power levels because of cost and performance. Two of the most popular switching regulator circuits are shown in Figure 4. The circuit of Figure 4a has been around a long time. It uses a 60 Hz transformer for isolation and a low voltage switching transistor to supply a series of high frequency (20 kHz) power pulses to an LC filter. The duty cycle control circuit determines the average output voltage. It's popular today because it is simple to design and uses standard off-the-shelf components. Many of these circuits use a standard linear IC[2] regulator for the complete control function. The chief disadvantage of this circuit is the large size of the 60 Hz transformer.

The circuit in Figure 4b is more representative of present day switching regulator designs. It uses a high voltage switching transistor to drive a 20 kHz transformer directly from the rectified line. Primary inductance is the key to operation of this circuit. With variable pulse width control, the energy stored and switched to the output capacitor is adjusted to meet the demands of the load. Since this core must handle dc in the primary winding, it tends to be larger and more expensive than its inverter counterpart.

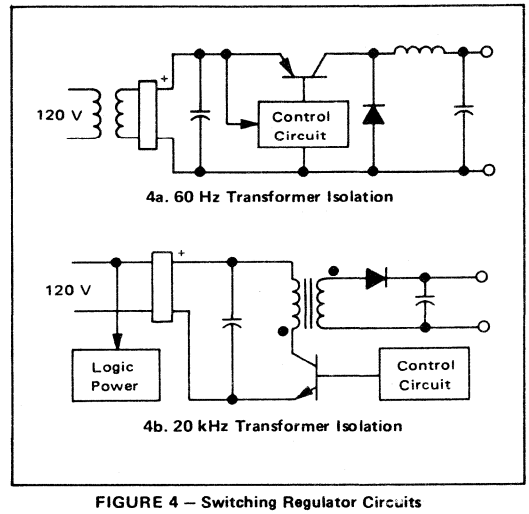


FIGURE 4 – Switching Regulator Circuits

PWM Inverter Circuits

The common inverter (two transistor) circuits operate from 120 V single phase and 208 or 220 V three phase lines and supply from 200 W to 1 kW. Most inverter transistors on the market today (including Motorola's 2N6542 through 47 family) have a nominal $V_{CEO(sus)}$ rating of 300-400 V. This means that the devices are characterized for Safe Operating Area (SOA) up to this point and that resistive and reactive loads may be switched in this region. However, these same devices may also be operated above this voltage limit in the blocking mode. Generally, the V_{CEX} or blocking rating is about 600-800 V except for Darlingtons. Because the standard transistor has this 400 V switching limit, two separate inverter circuits have evolved for use with the low and high voltage lines as shown in Figure 5. The standard

[2]See the MC1723 data sheet as an example.

inverter is used when 120 V power is available and the half bridge is generally chosen for 220 V applications. Both circuits operate in a similar fashion by alternately switching power to the 20 kHz transformer. The transformer output is rectified and the amplitude and duty cycle of the output voltage pulses determine the average output voltage. Because the output pulses are modulated to provide regulation, these circuits are known as pulse width modulated (PWM) inverters.

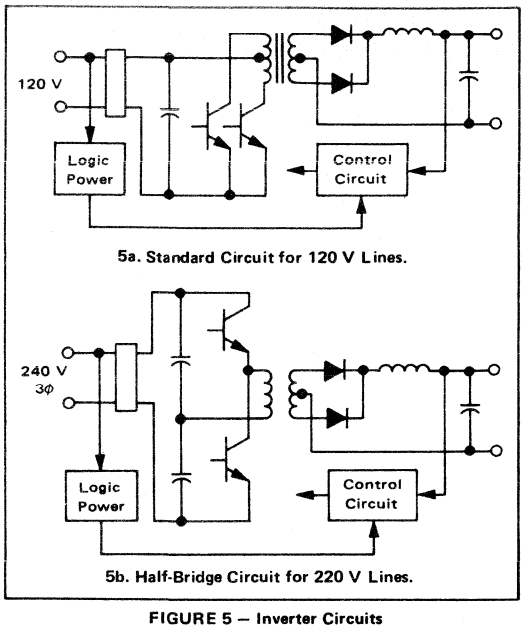


FIGURE 5 – Inverter Circuits

The transistor waveforms in Figure 6 represent the switching sequence for both circuits shown in Figure 5. Here it is easy to see why the dual voltage ratings of inverter transistors is important. In the standard inverter, the transistor switches collector current pulses (load current times the turns ratio) from the peak line voltage of 170 V. After some dead time, the opposite transistor is energized and the original must block twice the line voltage due to autotransformer action. In the half bridge operating from 220 V, the collector voltages are almost identical.[3] The dc bus is 340 V peak but each filter capacitor is charged to only 170 V. The transistors switch current at 170 V as before and again must block twice this voltage when the opposite side is energized. Actual waveforms are slightly different from the theoretical. The current pulse may have a spike on the leading edge and a slight positive slope due to the magnetizing current. An inductive kick during turn-off is usually present on the voltage waveform with some ringing during the dead time. These last effects are minimized by using an RC snubber across the primary to absorb the leakage reactance spikes and dampen the ringing.

Because the input filter capacitors in the half bridge must handle high RMS currents, these circuits tend to be

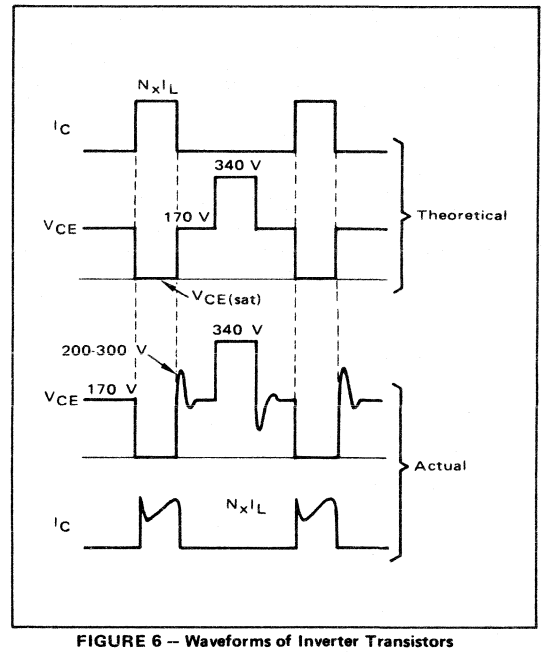


FIGURE 6 – Waveforms of Inverter Transistors

more expensive than the standard push-pull, but remain currently more popular for two reasons. One is that a coupling capacitor may be used to reduce transformer saturation problems (see reference 13 for the formula) and the second is that they can be made to conveniently operate from either 120 or 220 V (domestic or foreign). In these dual voltage designs, the capacitors are used as voltage doublers as shown in Figure 7. However, as the RMS currents are quite high in the 120 V mode, it is recommended that an additional switch contact be used to parallel the rectifier diodes as shown. The Motorola diode assemblies with ratings from 1 to 20 A are excellent for this application as the individual diodes are matched and will share current well.

The control circuits for these inverters may be located at the load or on the primary side of the transformer. Generally, power for these circuits is obtained from the ac line using either a free-running inverter or a standard 60 Hz transformer and series pass regulator. In the half bridge, the control circuits are grounded at the load. Voltage sense for the feedback signal is direct and transformers are used to couple the drive signals to the power transistors. The standard inverter may use this system or ground the control circuits at the power transistors. This latter approach simplifies the drive circuits and generally improves switching efficiency. Isolation is maintained by using an optoelectronic coupler in the feedback loop.

[3]For additional information on the half bridge inverter, see references #9, #10, and #13.

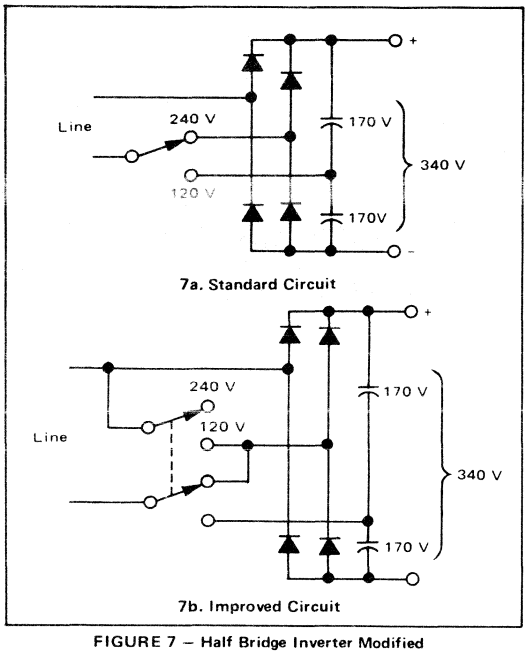


FIGURE 7 – Half Bridge Inverter Modified to Accept 120 or 240 V Inputs

A 5 V-40 A INVERTER SUPPLY EXAMPLE

This example deals with the design and performance of a 200 W inverter supply. The design specifications are as follows:

Input: 120 Vac ±10% @ 60 Hz
Output: 5 V @ 40 A (50 A capability; wire size, etc.)
Line/Load Regulation: ±1% (Half load to full)
Ripple: 120 Hz 10 mV_{RMS}
40 kHz 10 mV_{RMS} (Switching Frequency 20 kHz)
Ambient Temperature: 0-70°C
Efficiency: 70%

The standard inverter configuration is used with the control circuits on the primary side and an optoelectronic coupler for feedback. The block diagram is shown in Figure 8. The oscillator (an astable multivibrator) generates clock pulses which alternately set the outputs of the phase splitter (a bistable flip-flop) high. These clock pulses also enable a timing circuit in the pulse width control (a one-shot or monostable multivibrator). The splitter provides the mean for alternating these control pulses to the inverter transistor through gates 1 and 2 and the driver stage. The transistors operate the inverter transformer in a push-pull mode at 20 kHz. The output of this transformer is then rectified and filtered to become the 5 V, 40 A dc supply to the load. Logic power is obtained from the line using a 60 Hz transformer and IC series pass regulators.

CMOS logic is used for the control logic because its supply voltage is not critical and the large voltage swings provide good noise immunity. Two IC packages, a dual D flip-flop and a quad 2-input NAND gate, are used to provide all these functions (the circuitry will be described later). An operational amplifier and optoelectronic coupler are used to process the feedback signal. The high voltage supply to the inverter is a full wave bridge which operates from the 120 V line into a capacitive filter.

TRANSFORMER AND FILTER DESIGN

The power stage is the heart of an inverter; the correct choice of transistors, transformers, and filter is the most important part of this design. The magnetic design of inverter components is not too difficult when some practical guidelines are available.[4] Ferrite cores, which have a 100°C temperature limit, are normally used at 20 kHz because they have very little core loss. This loss increases slightly with 0.5 mil nickel-iron cores such as Permalloy and Orthonol, which must be used for higher

[4]See also reference #8.

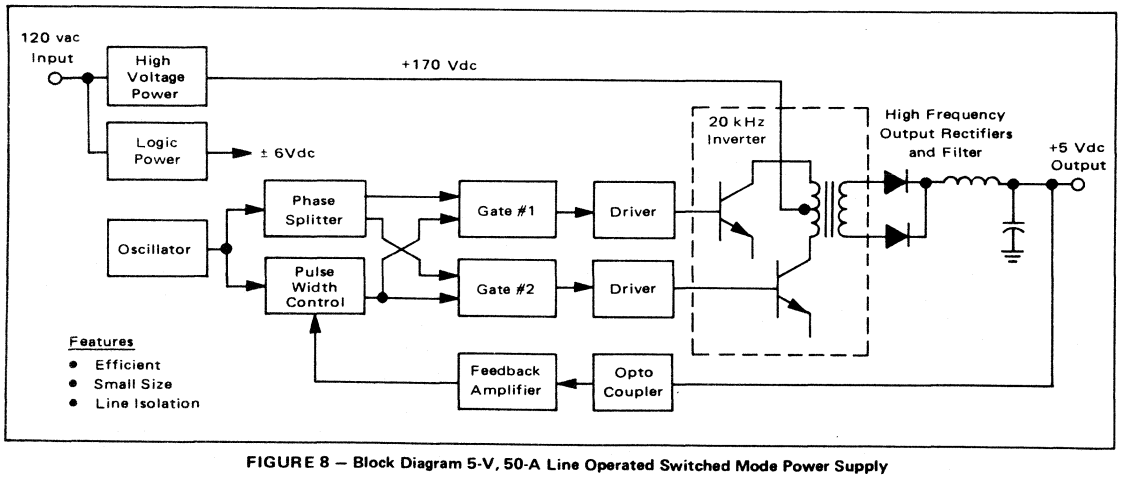


FIGURE 8 – Block Diagram 5-V, 50-A Line Operated Switched Mode Power Supply

temperature applications. For transformers, the best coupling comes from toroids, with pot cores a close second. Since toroids are difficult to wind and pot cores tend to trap heat (ferrite is a ceramic and a good insulator), C and E cores are generally used above 200 W. In addition to being easy to wind with bobbins, these latter cores facilitate the use of foil or strap to improve the winding efficiency of high current secondaries (>50 A).

POWER TRANSFORMER

In this design, efficiency was more important than size and an oversize pot core was used for the transformer to obtain the following advantages:

1. Few turns required to operate at low flux densities
2. Low core loss (operate at 20% of B_m)
3. Low copper loss (minimized turns)
4. Good coupling
5. Relatively easy to wind (the #10 secondary was somewhat difficult to shape)

In transformer design, the turns ratio and wire size are calculated first, then the core is selected. The information in Figure 9 of transformer waveforms at low line is used to find the required turns ratio. The information required includes:

1. Low line voltage
2. Input ripple
3. Output voltage
4. Minimum dead time (and frequency)
5. Output rectifier and filter losses

The low line specification of 110 V and 20 V ripple voltage (peak-to-peak) gives a minimum dc input to the primary windings of 130 V. With 5 μs of dead time between pulses, the duty cycle is 80% and 6 V pulses are required at the filter to obtain 5 V output. Assuming the rectifier drops (0.5 V) and filter loss at full load is 1 V, the secondary voltage pulses must be 7 V minimum. An additional 10% safety factor (0.7 V) is recommended to make up for miscellaneous input rectifier, transistor, and transformer losses. The required turns ratio (N), is therefore:

$$N = V_p/V_s = 130\ V/7.7\ V = 16.8 \simeq 16 \qquad (1)$$

With the turns ratio and the control logic set to limit duty cycle to 80%, the supply stayed in regulation at 110 V and dropped out with the line at 100 V.

Some wire tables recommend using 1000 CM/A (circular mils per ampere) or 1000 A/sq inch but most designers use anywhere from 300 to 500 CM/A as a guideline. With 50 A in the secondary and a 16:1 turns ratio, primary current pulses are about 3 A. Since both windings are center-tapped, current pulses cannot exceed a 50% duty cycle. Therefore, the wire size was chosen for RMS values of 35 A and 2 A. Number 10 (12,000 CM) was chosen for the secondary and number 20 (1000 CM) for the primary. Two number 13 (6000 CM) or four number 16 (3000 CM) were considered to make the secondary easier to wind, but the pot core does not have space available to bring out the interconnections.

To determine the proper core and number of turns three steps are required as follows:[5]

Step 1. Find the minimum core size and choose a core using

$$A_cA_w \geq \frac{2P_o}{f\,B_m} \times 10^{11}\ CM\ cm^2 \qquad (2)$$

where A_c = core area (cm^2)
A_w = window area (CM)
P_o = output power
f = frequency
B_m = saturation flux density (gauss)

A typical ferrite material has B_m = 3000 gauss. For this 200 W, 20 kHz inverter

$$A_cA_w \geq \frac{2 \times 250 \times 10^{11}}{20\ k \times 3\ k} = 0.83 \times 10^6\ CM\ cm^2$$

[5]The equations are from reference #7.

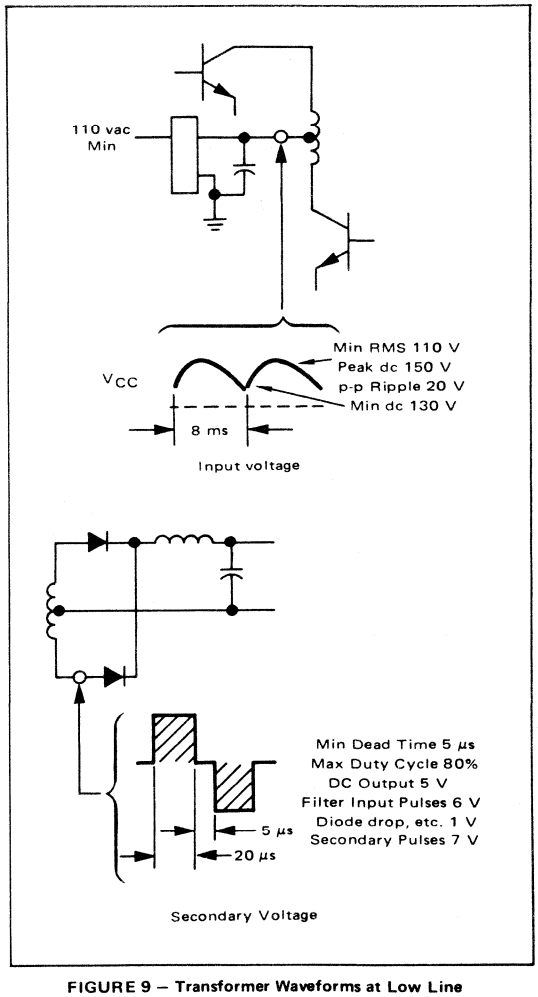


FIGURE 9 – Transformer Waveforms at Low Line

Two cores available from the Ferroxcube catalog with size information are listed in Table 1.

TABLE I — Ferroxcube Cup Cores

Core Number	A_c cm^2	A_w* in^2	A_w CM	A_cA_w CM $cm^2 \times 10^6$
4229	2.7	0.22	0.22×10^6	0.6
6656	7.5	0.62	0.62×10^6	4.6

*Note: This is the area available on the standard bobbin.

Because the formula uses the conservative wire rating of 1000 CM/A, it would be possible to use the 4229 core for this design. However, since it is desirable to operate well below B_m to minimize core loss, the 6656, which is oversize by a factor of five, is used.

Step 2. Find the required primary turns using

$$N_p \geq \frac{V_p \times 10^8}{4 f A_c B_m} \qquad (3)$$

where N_p = primary turns
V_p = primary voltage

Here the primary voltage is the peak of the high line input (130 V) and

$$N_p \geq \frac{130 \times 1.4 \times 10^8}{4 \times 20\text{ k} \times 7.5 \times 3\text{ k}} = 10$$

This is the minimum number of turns required. Since five turns are desirable on the secondary for good coupling, and the turns ratio is 16:1, 80 turns were used on the primary instead of 10.

Step 3. "Check the fit" of wire and window area using

$$A_W \geq 2(N_p A_{xp} + N_s A_{xs})/0.8 \text{ CM} \qquad (4)$$

where N_S = secondary turns (N_p/N)
A_X = wire size (CM)

In this case the primary wire size is 1000 CM (#20) and the secondary wire size is 12,000 CM (#10). This gives

$$A_W \geq 2\,(80 \times 1\text{ k} + 5 \times 12\text{ k})/0.8 = 0.35 \times 10^6 \text{ CM}$$

The available winding area on the 6656 bobbin is 0.62×10^6 CM which indicates that only about half the available space was used.

FILTER CHOKE

For the output filter choke, it was decided to use two "U" cores, as these cores facilitate winding high current strap or foil. In filter design, the inductance and wire size are calculated first, then the core choice follows. Inductance can be calculated using

$$L \geq V_O/f\,(0.10)\,I_O(\text{min}) \qquad (5)$$

where L = inductance (H)
V_O = output voltage
f = frequency
I_O(min) = minimum output current

In this case, the minimum output current was chosen to be 20 A (just less than half load). The frequency is 40 kHz at this point (from the full wave rectifiers); therefore

$$L \geqslant \frac{5}{40\text{ k}\,(0.10)20} \simeq 60\ \mu\text{H}$$

The 0.10 factor limits choke current variations to 10% at light loads. To conserve space, it is possible to allow 100% current variations and use a 6 μH choke. However, most designs follow the 10% guideline.

Wire size is determined using 500 CM/A as the guide. The choke current can be 50 A continuous, so two 1.125" by 10 mil copper strap were used for the winding. Strap or foil is easier to wind than the large wire and is also preferred as it will lie close to the core for good magnetic coupling.

Four steps are required to choose the core and determine the proper number of turns and the required air gap size as follows.[6]

Step 1. Find the minimum core size and choose a core using

$$A_cA_W \geqslant \frac{A_X\,LI \times 10^8}{0.8\,B_m} \qquad (6)$$

where I = Saturation current level

Ferrites used for U cores have B_m = 3800. For this design, it was already determined that a 60 μH, 50 A choke is required and that the strap size is 22,500 CM (2.25" x 10 mil"). Therefore

$$A_cA_W \geqslant \frac{22.5\text{ k} \times 60\ \mu \times 50 \times 10^8}{0.8 \times 3800} = 2.3 \times 10^6 \text{ CM cm}^2$$

Ferroxcube catalog information on two possible U cores is shown in Table II.

The 1F10 core is a good choice here, but a 1F5 was used instead as it was available.

Step 2. Find the required number of turns using

$$N = \frac{LI}{A_cB_M} \times 10^8 \qquad (7)$$

In this case, A_c = 6.45 and

$$N = \frac{60\ \mu \times 50 \times 10^8}{6.45 \times 3800} = 14 \text{ turns}$$

Step 3. "Check the fit" of wire and window area using

$$A_W \geqslant NA_X/0.8 \qquad (8)$$

which gives

The core used has a window area of 5.0×10^6 CM which allows plenty of room for this winding. Mylar tape was used to insulate the layers.

[6]The equations are from reference #7.

TABLE II – Ferroxcube U-U Cores

Core Number	A_c cm^2	A_W* in^2	$A_c A_W$ CM $cm^2 \times 10^6$
1F10	2.04	1.5	3.0
1F5	6.45	5.0	32

*Note: Obtained from inside core dimensions.

Step 4. Determine the air gap required to prevent saturation using

$$l_g = \frac{0.4\pi NI}{B_M} - \frac{l_m}{\mu} \qquad (9)$$

where l_g = air gap length (cm)
l_m = magnetic path length (cm)
μ = core permeability

Using the catalog, we find that only 3C5 material is available for this U core configuration (with $\mu = 2000$) and that $l_m = 31.5$ cm. Therefore,

$$l_g = \frac{0.4\pi \times 14 \times 50}{3800} - \frac{31.5}{2000}$$

$$= 230 \times 10^{-3} - 15 \times 10^{-3} = 215 \times 10^{-3} \text{ cm}$$

Converting l_g to inches gives a required gap of 80 mils or 40 on each side of the core. It should be noted that the gap reluctance is much higher than the core reluctance (230:15) and that it therefore is controlling L and I. This being the case, if the gap is doubled, L halves and I doubles. If the turns are doubled, L increases by 4 (N^2) and I is halved. Therefore, if both the turns and gap are doubled, I remains the same but L doubles. When there is additional winding space available, it is possible to increase the inductance by filling this area even though the gap must be increased appropriately to prevent saturation at the rated current.

In this case, these relationships were used to check the magnetic design just completed. 140 turns (instead of 14) of light wire were placed on the core and it was gapped at 80 mils. L and I were then measured at relatively low test levels resulting in 6 mH of inductance which saturated just over 5 A. Thus, the calculated 14 turns give us 60 μH at 50 A.

Filter Capacitor

With the completion of the transformer and filter designs, the remaining passive component required in the power stage is the output filter capacitor. The size of this capacitor is determined using[7]

$$C \geq \frac{(V_{in} - V_O)V_O}{2Lf^2 V_{in}\, v_o} \times 10^6\ \mu F \qquad (10)$$

where C = capacitor size (μF)
V_{in} = filter input voltage (V)
V_O = filter output voltage (V)
v_o = peak to peak output ripple at the switching frequency (V)

There is no dependance on load in this formula, as only the changes in inductor current must be filtered out. These changes are dependent only on voltage, inductance and frequency and not on the average inductor (or load) current. With a nominal 160 V in to the 16:1 power transformer, the input amplitude to the filter is 10 V. Ripple frequency is 40 kHz and the ripple specification is 10 mV (RMS) or 28 mV peak to peak. This gives

$$C \geq \frac{(10 - 5)\, 5 \times 10^6}{2 \times 60\, \mu\, (40\text{ k})^2\, 10 \times 28\text{ m}} = 460\ \mu F$$

A 500 μF four terminal (high frequency) capacitor could be used but a lower cost standard aluminum electrolytic was chosen instead. Because series resistance and inductance are higher with the standard, a larger size (2000 μF) was required to obtain the desired performance.

POWER STAGE

The power stage is comprised of the following circuits:

1. High voltage power supply
2. Logic power supply
3. Drivers
4. Power transformer and transistors (inverter)
5. Output rectifiers and filter

The schematic of these circuits is shown in Figure 10. A bridge rectifier and capacitive filter are connected directly to the 120 Vac line to form the high voltage supply. The output is 160 Vdc with $\approx$ 20 V peak-to-peak of 120 Hz ripple. These voltage variations are attenuated 60 dB by the control circuits resulting in $\approx$ 10 mV of low frequency ripple at the load.

The logic supplies are obtained using a 15 W filament transformer, bridge rectifier, and filter to operate ±6 V three terminal IC regulators (the MC7806 and 7906). The logic is connected between these two low-voltage supplies.

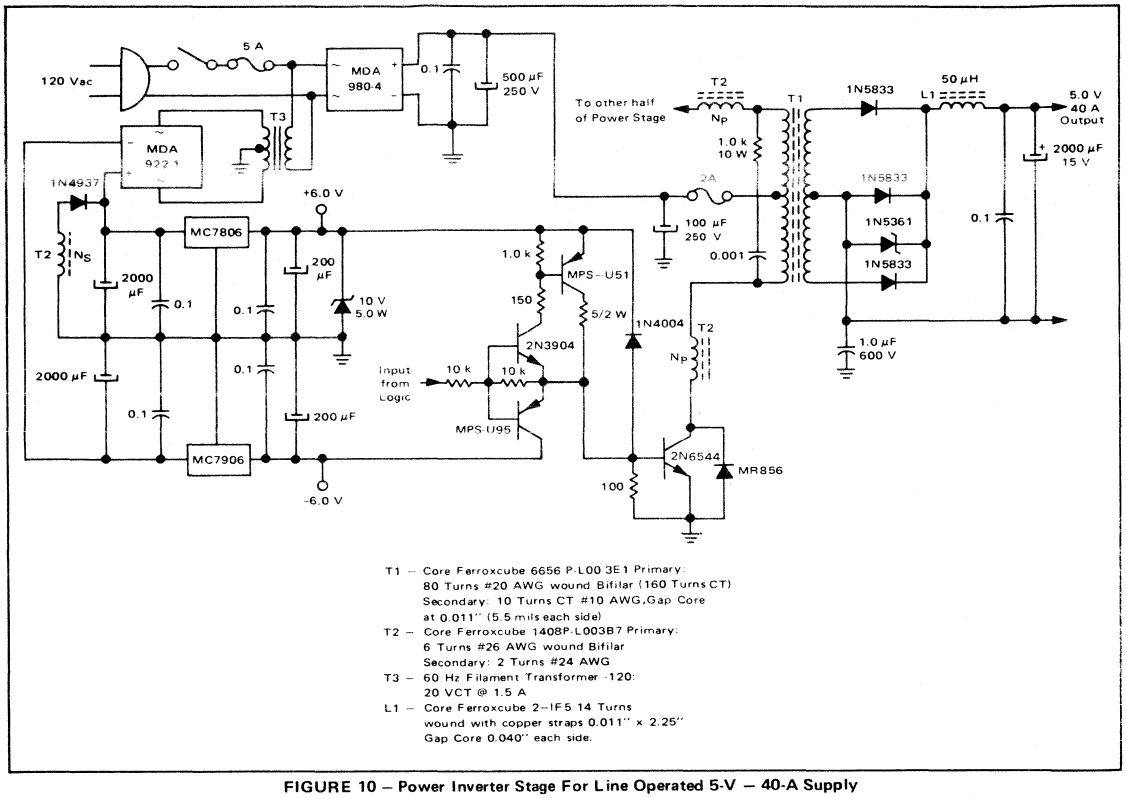
The two voltages are used with a push-pull drive stage to provide both positive and negative base drive to the inverter transistors. When the logic signal is high, the 2.0 A MPS-U51 saturates and supplies 1 A to the base of the 2N6306 inverter power transistor. When the logic is low, the 1.5 A MPS-U95 darlington operates in a current limited mode during storage time and then applies -5 V to the base to hold the inverter transistor off. Figure 11 shows this base current waveform at rated load. Storage time is under 2 μs with these fast switching Uniwatt▲ drivers and will increase slightly at lighter loads.

Power Transistors

Motorola 2N6544 power transistors were used in the inverter because they are fast and economical. These transistors have an 8 A current rating, but are specified for beta and switching speed and used here at 3 A of collector current. The switching sequence and load lines at full load of these devices (before and after shaping) are shown in Figure 12. A current spike observed during turn-on was contained using 80 μH of inductance on a common pot core in series with each collector. This improved the load line and reduced turn-on losses in

[7] This equation is from reference #3.

▲ Trademark of Motorola, Inc.



T1 – Core Ferroxcube 6656 P-L00 3E1 Primary:
80 Turns #20 AWG wound Bifilar (160 Turns CT)
Secondary: 10 Turns CT #10 AWG, Gap Core
at 0.011" (5.5 mils each side)

T2 – Core Ferroxcube 1408P-L003B7 Primary:
6 Turns #26 AWG wound Bifilar
Secondary: 2 Turns #24 AWG

T3 – 60 Hz Filament Transformer -120:
20 VCT @ 1.5 A

L1 – Core Ferroxcube 2–IF5 14 Turns
wound with copper straps 0.011" x 2.25"
Gap Core 0.040" each side.

FIGURE 10 – Power Inverter Stage For Line Operated 5-V – 40-A Supply

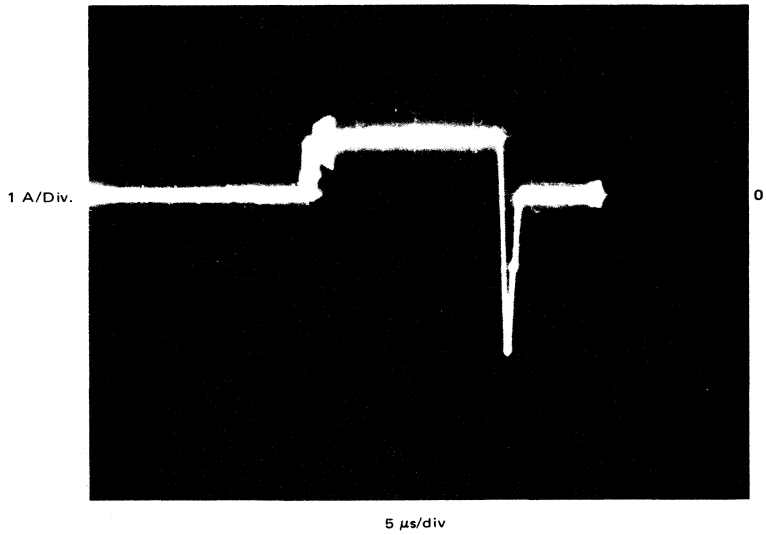
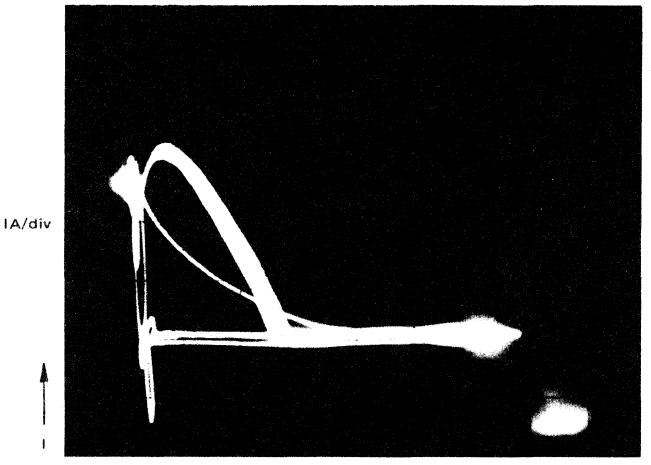
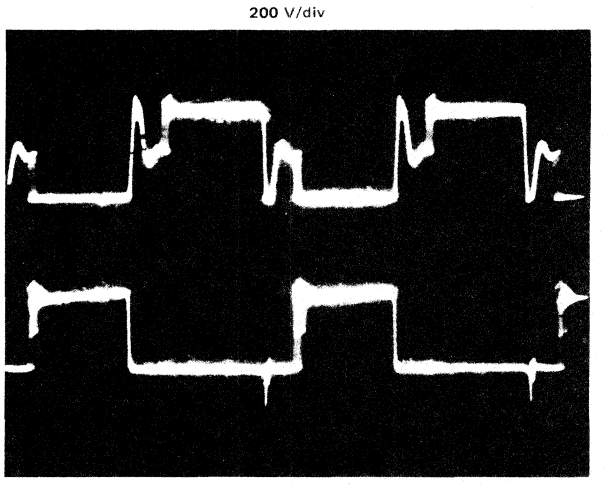
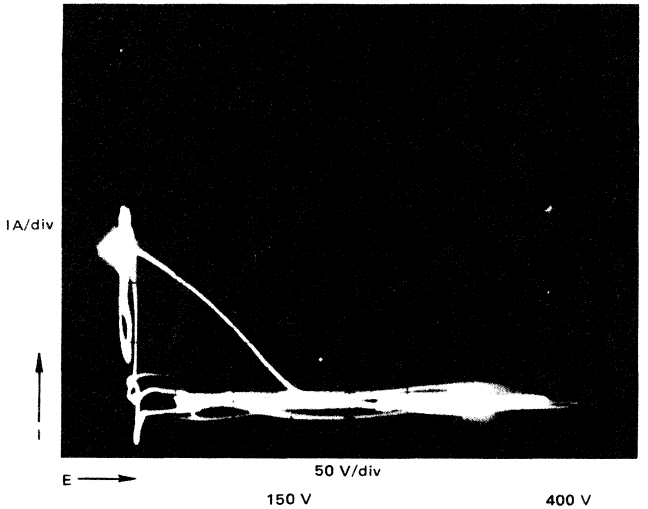


FIGURE 11 – Base Current







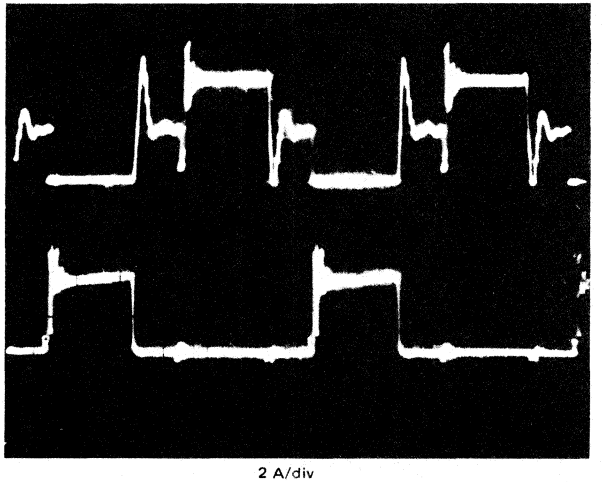


FIGURE 12 – Load Lines

the transistors without significantly affecting turn-off. Energy stored in these inductors is returned to the low voltage filter capacitor during the dead time interval (5 μs minimum) by the secondary winding on this core.[8] This technique therefore affords very efficient suppression of the current spikes with controlled voltage clamps. The resulting load line shows resistive switching during turn-off to 150 V and blocking to 400 V. The V_{CEO} and V_{CEX} ratings on this device are 300 and 650 V which are quite adequate for this application.

The inductive kick from the core can be observed as turn-off voltage spikes in Figure 12. These spikes are clamped to twice the supply by diodes across each transistor, and are "snubbed" by the standard RC network across the primary to allow the transistors to turn off before this voltage level is reached.

Transformer Saturation

The transformer, as discussed earlier, is a 2.5" ferrite pot core from Ferroxcube, hand wound with a 16-to-1 turns ratio. The collector current pulses of 2.5 A in Figure 12 therefore represent a load current of 40 A. The core was gapped empirically at 10 mils to provide about 100 mA of magnetizing current. This increases the saturation level and allows a slight imbalance in primary current pulses to exist. Such an imbalance can be created by component drifts or load changes and tends to build a dc component of flux in the core (a process known as "racheting"). This ultimately causes core saturation and destroys the power transistors.

Matched transistors (beta within 10% at 1 A) were initially used in this unit. However, subsequent field tests revealed that matched transistors are not sufficient to prevent long term transformer saturation. Based on these findings, it is now recommeded that either symmetry correction circuits or a simple over-current shutdown circuit be used for all direct coupled push-pull inverters. A suggested shutdown circuit is shown in Figure 13.

Output Rectifiers and Filter

Because efficiency is important, 50 A, 30 V barrier diodes (Motorola 1N5833) are used as the output rectifiers, although they are more expensive than fast recovery rectifiers. These diodes are fast and have low forward drops (0.5 V). However, junction temperature is limited to 100°C and for this reason, a fairly large heat sink is required (0.5°C/W) to operate safely in 70°C ambients without forced air cooling. A free wheeling diode was used but carries little current. All three diodes are protected against voltage transients (a 1 μs voltage transient can cause shorts) by a 27 V, 5 W zener placed across the free-wheeling diode. The rectifier current waveform is shown in Figure 14. The peak current is 40 A (full load) and drops to half during the dead time (each rectifier shares the filter choke current). The absence of reverse recovery spikes in this picture is an indication of the excellent high speed blocking characteristics of these parts.

The output filter elements were discussed earlier. The choke was made by winding copper strap on two "C" cores with outside dimensions of 4 x 4.5" and gapping it to prevent saturation. The capacitor is a standard 2000 μF electrolytic with a single 0.1 μF RF bypass in parallel. Worst case design of the choke allowed 2 A variation in choke current. The normal choke current variations shown in Figure 15 are only 0.8 A. With these components, the 40 kHz ripple is 25 mV peak to peak.

[8]For additional information, see references #1, 2, and 12.

[9]For additional information, see reference #11

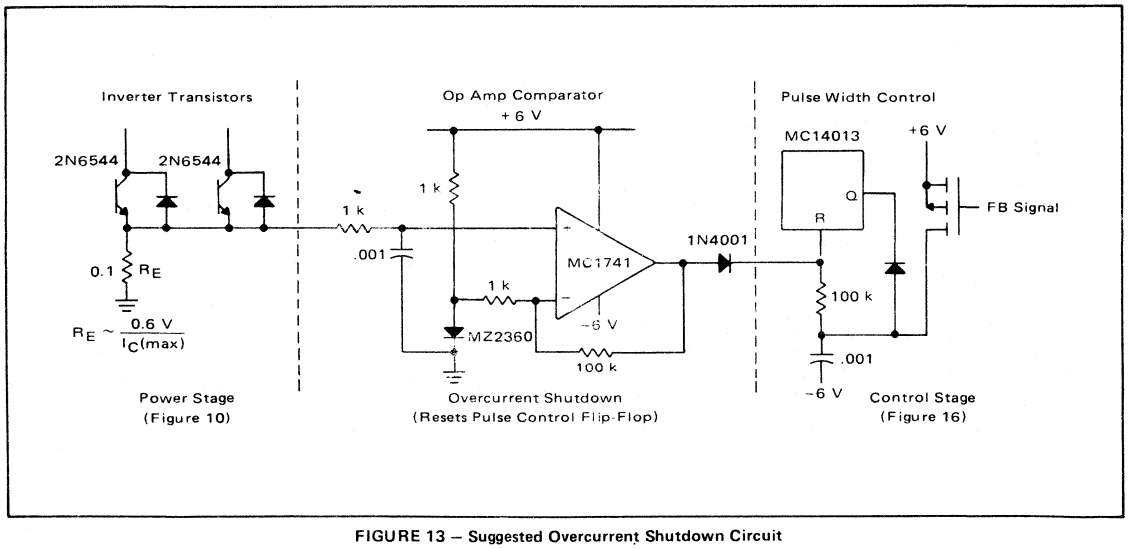


FIGURE 13 – Suggested Overcurrent Shutdown Circuit

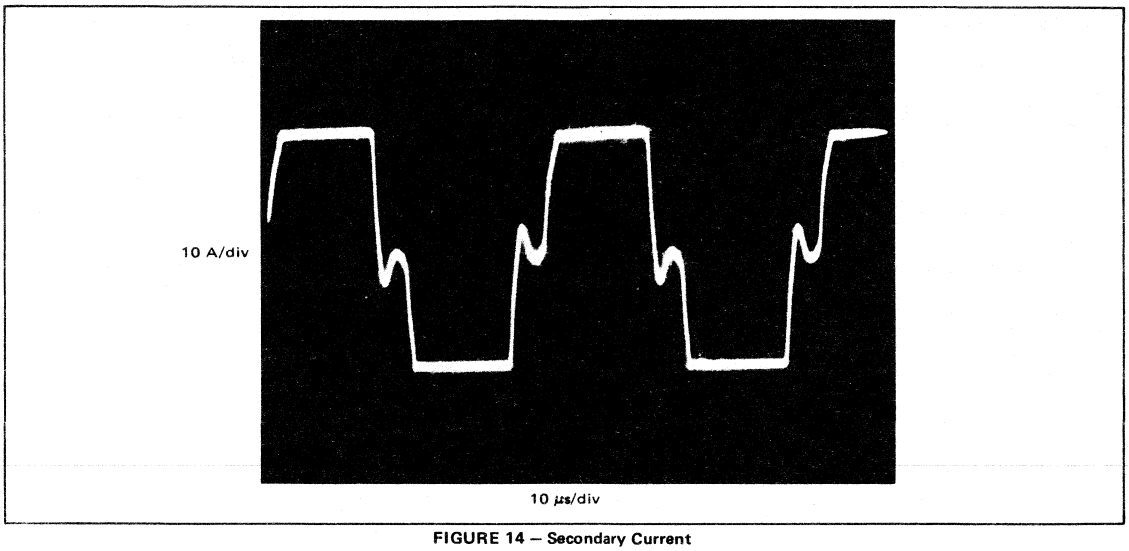


FIGURE 14 – Secondary Current

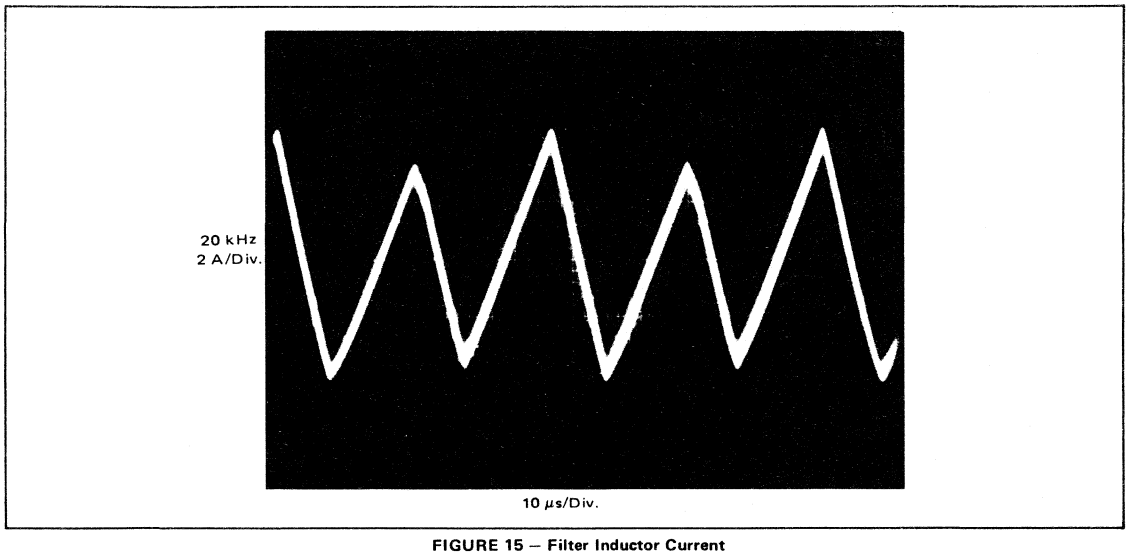


FIGURE 15 – Filter Inductor Current

CONTROL STAGE DETAILS

The basic functions of the control stage were discussed earlier in the block diagram section. The schematic of this stage is shown in Figure 16. The various circuits required for the control function include:

1. Oscillator
2. Phase splitter
3. Pulse width control
4. Gates
5. Opto isolation
6. Feedback amplifier

Functions 1 and 4 are obtained from a single CMOS package, the MC14001 quad 2-input NOR gate. A second CMOS package (the MC14013), a dual D flip-flop is used to implement functions 2 and 3. Two other dual-in-line IC packages, the 4N28 optoelectronic coupler and the MC1741 operational amplifier, contain the circuits used to implement functions 5 and 6.

The phase splitter is a flip-flop which operates in the toggle mode with $\overline{Q}$ connected to D. The pulse control flip-flop operates as a one shot and resets itself when the FET current charges the 0.001 μF timing capacitor to half

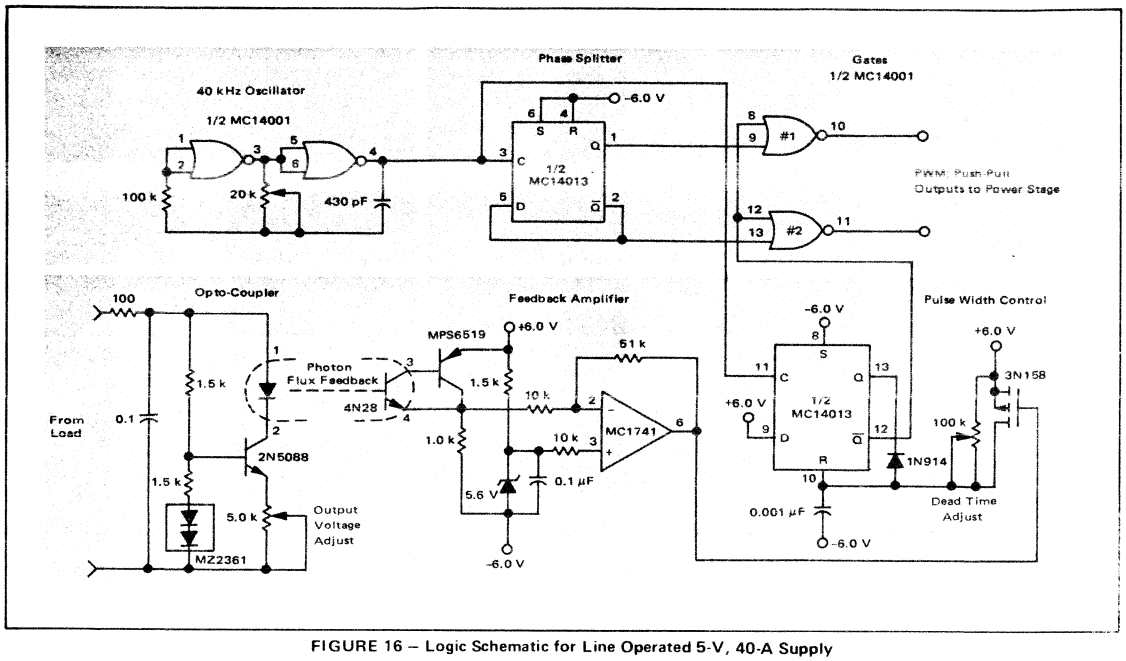


FIGURE 16 – Logic Schematic for Line Operated 5-V, 40-A Supply

the supply. The gates are enabled (high out) and turn on one of the power transistors only when both inputs are low. Since the splitter alternately causes one gate input to be low and then the other, both transistors can never be on at the same time. To further guard against simultaneous conduction and high "shoot through" currents, a resistor across the FET forces reset action in the one shot to occur in 20 μs, 5 μs before the opposite side is enabled. Because the one shot is also connected to both gates, it introduces inhibiting action even before the splitter changes state. The interaction of the stages may be easier to see in the timing diagram (Figure 17). Positive clock pulses toggle the splitter and enable the one shot (or pulse width control circuit). When the control is low and the Q output of the splitter is low, gate #1 is enabled and turns one of the inverter transistors on. On the next clock pulse, the control will go low again and the Q output of the splitter will be high ($\overline{Q}$ low). At this time, gate #2 is enabled and the remaining inverter transistor turns on.

The pulse width of the control circuit determines the output voltage and it in turn is controlled by the feedback elements in this closed loop system. The optoelectronic coupler makes use of the LED to sense output voltage changes and feed back a signal to the photo transistor and operational amplifier. The operational amplifier gain determines how good the line and load regulation will be and how much ripple reduction to expect. Too much gain will cause instability and high output ripple content. The excessive ripple is created when the pulse width control vacillates from wide to narrow pulses without ever settling on the appropriate width for the given line and load conditions. To improve stability, a low frequency filter is often added at this point (such as the RC filter shown at the LED input). The operational amplifier output voltage is fed to the gate of a P-channel MOSFET. The FET performs a voltage-to-current conversion in this design and controls the charge rate of the timing capacitor which determines the output pulse width.

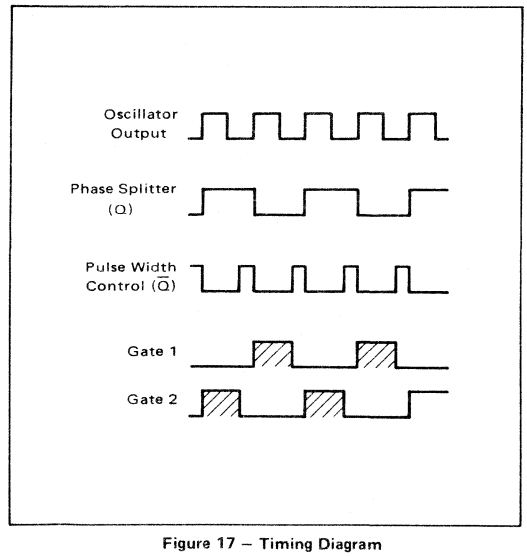


Figure 17 – Timing Diagram

Performance Data

The main features of this supply are that it is efficient and small. Some size was sacrificed in this design, in three areas specifically, to improve efficiency:

1. The barrier diode heat sink. Forced air cooling would reduce this size.
2. The inverter transformer. A large core which operates at low flux densities was used to reduce core losses.
3. The 60 Hz low voltage power transformer. A free running inverter could have been used.

Efficiency was measured with 40 A load current at 5 V. The input voltage and current waveforms are shown in Figure 18 and contain the information required to calculate input power. Assuming the input voltage is constant during current conduction:

$$P_{in} = \frac{V_{IN(peak)}}{T} \int_0^T Idt \qquad (11)$$

where P_{in} = average input power
$V_{IN(peak)}$ = peak input voltage
$\int Idt$ = area of the current pulse
T = half cycle period

with $V_{IN(peak)}$ = 165 V, T = 8.3 ms and counting 15 sq cm at 4 A and 0.2 ms per cm gives

$$P_{in} = \frac{165}{8.3\ m} (15 \times 4 \times 0.2\ m) = 240\ W$$

The efficiency therefore is

$$\eta = \frac{P_o}{P_{in}} = \frac{5\ V \times 40\ A}{240} \approx 83\% \qquad (12)$$

The total power loss in this design is about 40 W. Of this about 20 W is lost to the output rectifiers and 5 W to each IC regulator and both base resistors (another 15 W total). There was no noticeable heat rise in either the transformer or the power transistors.

This design also features line and load isolation which is made possible by the inverter transformer and optoelectronic coupler for feedback. Output voltage readings under the specified line and load variations are shown in Table III.

TABLE III – Output Voltage Readings

$V_{IN(RMS)}$	I_o	V_o
110	40	5.009
120	40	5.046
130	40	5.062
110	20	5.057
120	20	5.080
130	20	5.092

Using this data, and defining regulation as

$$\%\ Reg = \frac{\Delta V_o}{V_o} \times 100 \qquad (13)$$

gives

1. Line regulation at 40 A = 1.1% (53 mV)
2. Load Regulation at 120 V = 0.7% (34 mV)
3. Combined regulation = 1.7% (83 mV)

These figures represent the typical performance that can be obtained from this type of supply of 1% regulation before stability becomes a problem.

The ripple content of the output voltage at rated load is shown in Figure 19. In Figure 19A the 120 Hz ripple is 20 mV peak-to-peak or less than 10 mV_{RMS}. Input ripple was 20 V and with gain optimized, a 60 dB reduction was obtained. To further reduce 120 Hz ripple, the input filter capacitor would have to be increased. In Figure 19A, the 40 kHz ripple is also 20 mV peak-to-peak. In the previous filter design section, it was pointed out that this is strictly a function of the output filter elements. However, with practical high frequency limits of present components, the best designs can only reduce this num-

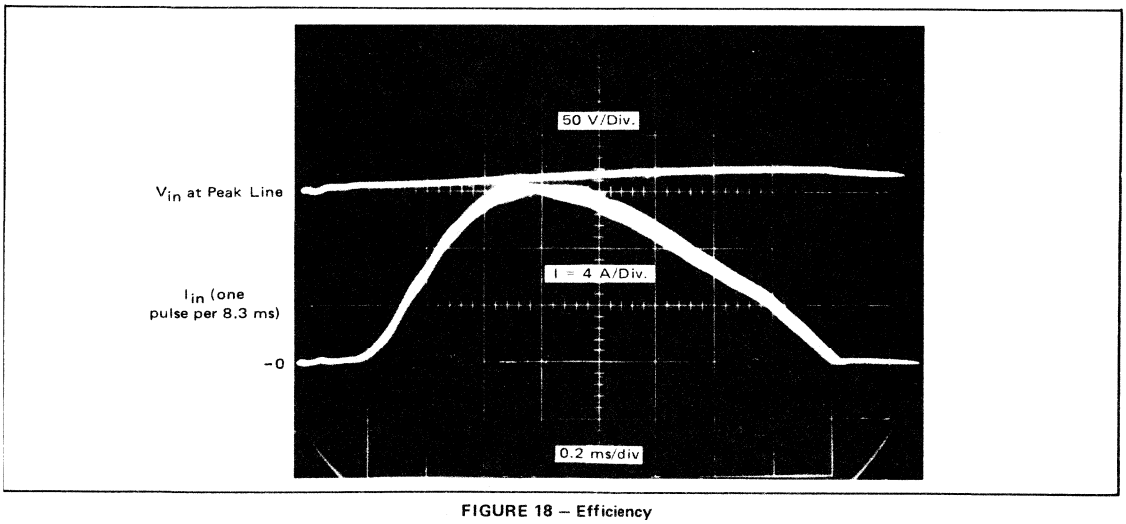


FIGURE 18 – Efficiency

ber to about 5 mV. Noise spikes, which are difficult to see in the pictures, were approximately 200 mV peak-to-peak. The spikes couple through the interwinding capacity of the filter inductor and are attenuated slightly by the 0.1 μF ceramic bypass capacitor. Further reduction would require an additional high frequency LC filter.

The overall performance of this regulator is quite good. The 10 mV ripple is more than adequate to drive standard TTL logic loads of small computers. In addition, several of these circuits could be operated from a dc bus between 140 and 200 V to supply the power requirements of a larger computer or industrial system. The 80% efficiency is exceptional. The completed supply required about 400 cubic inches and weighed about 10 pounds (see Figure 20). A further reduction in size and weight is possible with smaller heat sinks, forced air cooling and some sacrifice in efficiency by using a smaller inverter transformer and filter choke.

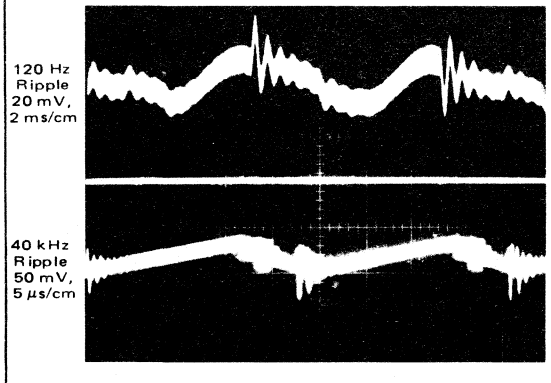


FIGURE 19 – Output Ripple

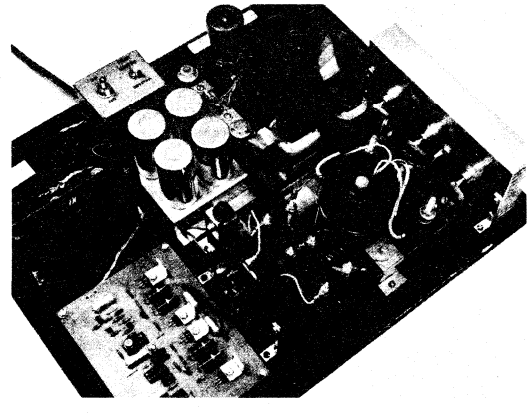


FIGURE 20 – Complete Supply

ACKNOWLEDGEMENT

The author wishes to acknowledge Paul Fletcher for the design improvements he contributed.

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AN-766
Application Note

A VARIABLE FREQUENCY CONTROL FOR 3ϕ INDUCTION MOTORS

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This application note describes a variable frequency, variable voltage drive system for three-phase induction motor controls. A survey of possible system configurations and a detailed description of a semiconverter/transistor inverter quasi-square wave drive system are included.

MOTOROLA *Semiconductor Products Inc.*

A VARIABLE FREQUENCY CONTROL FOR 3ϕ INDUCTION MOTORS

INTRODUCTION

The use of polyphase induction motors in industrial machine tools, conveyors, fans, pumps, etc. has been popular a long time due to the motors' inherent low cost, ruggedness and reliability. However, the induction motor loses some of its appeal if variable speed operation at constant torque is required. Unlike a dc motor, the induction motor's speed cannot be satisfactorily controlled by varying the excitation voltage; a variable frequency drive system must be utilized. With this method, rated output torque can be obtained over a motor speed range of greater than 30 to 1.

CONTROL SYSTEM CHARACTERISTICS

Typical speed-torque curves for an induction motor driven at different frequencies is shown in Figure 1. Note that the excitation voltage, Vac, is reduced as the drive frequency is reduced below its rated value (usually 60 Hz), maintaining a constant voltage-to-frequency ratio. This ratio keeps the motor air gap flux and magnetizing current constant. However, this V/f technique cannot be utilized for frequencies above rated drive frequency. Motor operation at higher than rated drive frequency (f_O) can be obtained if nameplate ratings for excitation voltage and output horsepower are not exceeded. This can be accomplished by keeping the excitation voltage constant at frequencies above rated f_O and loading the motor at less than or equal to rated horsepower in this region.

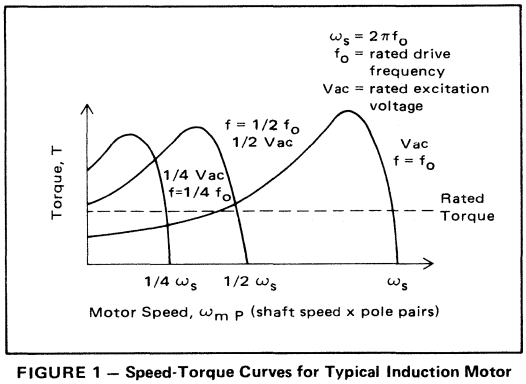


FIGURE 1 – Speed-Torque Curves for Typical Induction Motor

The desired motor operating conditions are shown in Figure 2. From approximately zero to f_O, constant V/f drive is utilized to obtain constant rated output torque. Above f_O, the excitation voltage is held constant rated output horsepower can be obtained. The upper li for the drive frequency, f1, is constrained by mc construction and is dependent on how much ine stress the rotor and motor bearings can safely han In general, the motor manufacturer must be consu for the suitability of a particular motor for variable quency drive. The following description is for a varia frequency drive system constructed for 208 V 3ϕ inc tion motors with up to 1-1/2 horsepower ratings.

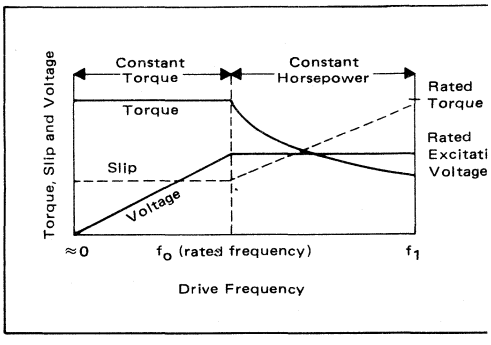


FIGURE 2 – Motor Operating Conditions

SYSTEM CONFIGURATION

In order to obtain the desired motor operation c acteristics of Figure 2, the drive system must be cap of independently controlling both the motor excita voltage and drive frequency. This is usually accomplis by utilizing a system configuration in which the 3ϕ ac voltage is transformed into an adjustable dc volt The drive system is then inverted to provide the vari frequency motor excitation.

Transforming the ac line voltage into variable dc be accomplished by either of the configurations sh in Figure 3. The first method is to full-wave rectify ac line voltage, smooth the result with a capacitor f and use a switching regulator to produce a variable output as shown in Figure 3a. This method has advantage of being highly efficient and does not req bulky filter components. Disadvantages are: it posse a poor line current form factor, much high-freque noise, and must handle power three times: 1) at the ir rectifiers, 2) the switching elements, and 3) the ou switching regulator rectifier.

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequent complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been ca fully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such informati does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

The second method, shown in Figure 3b, uses phase-ontrolled rectifiers to obtain the variable dc output oltage. This method, like the switching regulator approach, highly efficient. It has the advantages of producing a etter line current form factor and it handles the power nly once. However, it does require bulkier filter com-onents than the switching regulator method.

Once a source of variable dc voltage has been obtained, ie next system requirement is that the variable voltage e inverted into a variable frequency ac waveform for iotor excitation. This waveform should be sinusoidal, r as close to it as possible in order to minimize harmonic ontent and therefore, harmonic heating of the motor. ine-wave audio-type amplifiers have excessive dissipation; xed component filters are not usable because of the wide nge of output frequency. Therefore, a bridge type, SCR or ansistor, square-wave inverter is generally employed.

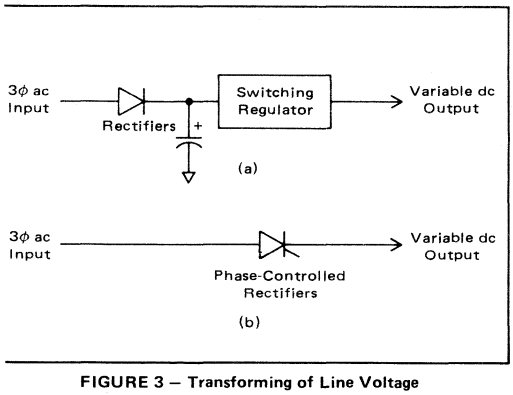


FIGURE 3 – Transforming of Line Voltage

The output waveshape of the inverter can be one of the vo forms shown in Figure 4. The waveform of Figure 4a a pulse width modulated sinusoidally weighted pulse ain. It is very low in harmonic content which results in w motor losses. However, semiconductor switching losses n be high and the circuitry required for generation of is waveform is complex.

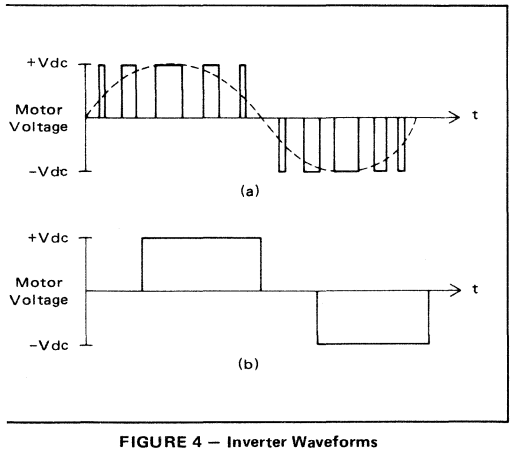


FIGURE 4 – Inverter Waveforms

An easier waveform to generate is shown in Figure 4b. This waveform, known as a quasi-square[1] wave is recognized as acceptable for motors to at least 10 horsepower, and can be readily generated by a six-transistor bridge inverter as shown in Figure 5. Also shown in Figure 5 are the transistor conduction sequence and line-to-line motor voltage waveforms.

Either of the above inverter waveform types could be used with either the switching regulator or phase-controlled rectifier scheme to obtain a system which meets the requirements for independent control of both excitation frequency and voltage[2]. For this design, the quasi-square wave inverter and phase-controlled rectifier schemes were emplcyed. The quasi-square wave inverter was chosen for its simplicity, while the phase-controlled rectifier configuration has a maximum output voltage (280 V) close to the 276 V required by the inverter for rated motor operation. (See Appendix for calculation of this voltage.)

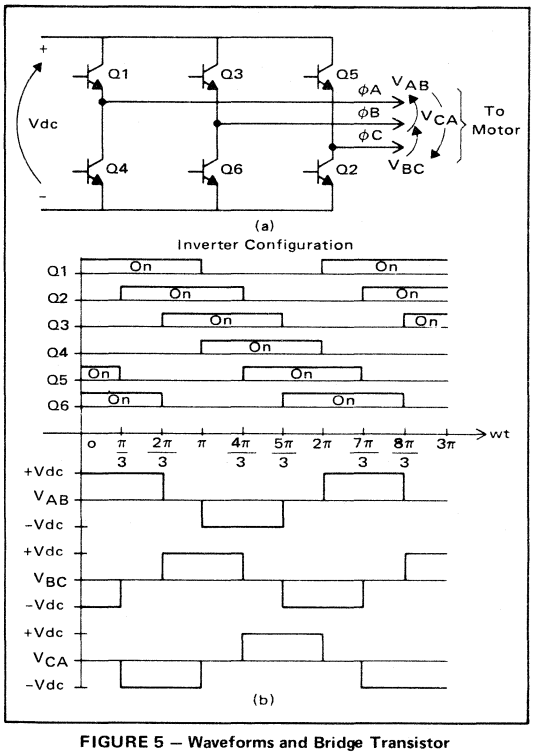


FIGURE 5 – Waveforms and Bridge Transistor Conduction Sequence

[1]Although higher in harmonic content than PWM sine weighted waveforms, the Quasi-square wave has no even or triplen harmonics. (2nd, 3rd, 4th, 6th, 9th, 10th, etc.)

[2]A method which has not been mentioned is a PWM technique in which both excitation voltage and drive frequency can be varied by use of a single inverter. However, the generation circuitry is extremely complex. For further details on this and other PWM motor control schemes, refer to "Advanced PWM Inverter Techniques," Jerry Pollack, *IEEE Transactions on Industry Applications*, Vol. IA-8, No. 2, April/March, 1972.

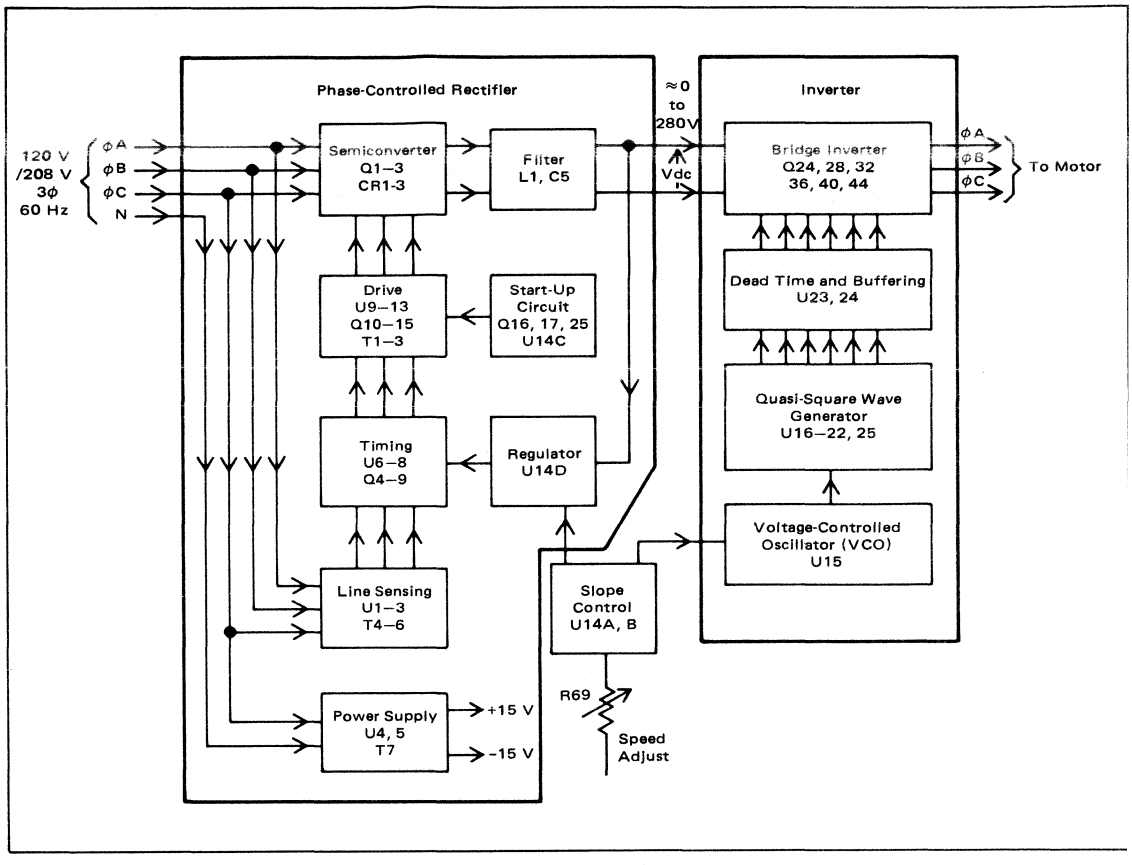


FIGURE 6 – System Block Diagram

SYSTEM BLOCK DIAGRAM

A detailed system block diagram is shown in Figure 6. Part numbers in this figure refer to those devices shown in the complete circuit schematic of Figure 7.

The phase-controlled rectifier section transforms the 3ϕ 208 V input into a variable dc output voltage. A semiconverter (3 SCRs and 3 diodes) was chosen instead of a full-converter configuration (6 SCRs) as the former method is considerably less complex and minimum output ripple is not a requirement.

Conduction angle control of the semiconverter is obtained by sensing the input line-to-line voltage zero crossings in the line sensing circuit and controllably delaying the firing command to the appropriate semiconverter SCR. This delay is $\approx$ 0 to 8.33 ms (180°) resulting in an output voltage of 280 V to $\approx$ 0 V, respectively. The firing command from the timing circuit initiates a 200 μs duration "picket-fence"[3] pulse train which is fed to the semiconverter SCR's gate for firing. The output of the semiconverter is then filtered and fed to the inverter section. The regulator circuit maintains the bus voltage Vdc, at a constant value determined by the output o the slope control circuit.

The slope control circuit controls the maximum acceleration and deceleration rates of the motor. It i the control link between the variable voltage and variabl frequency sections of the system; and is important t maintaining a constant V over f ratio.

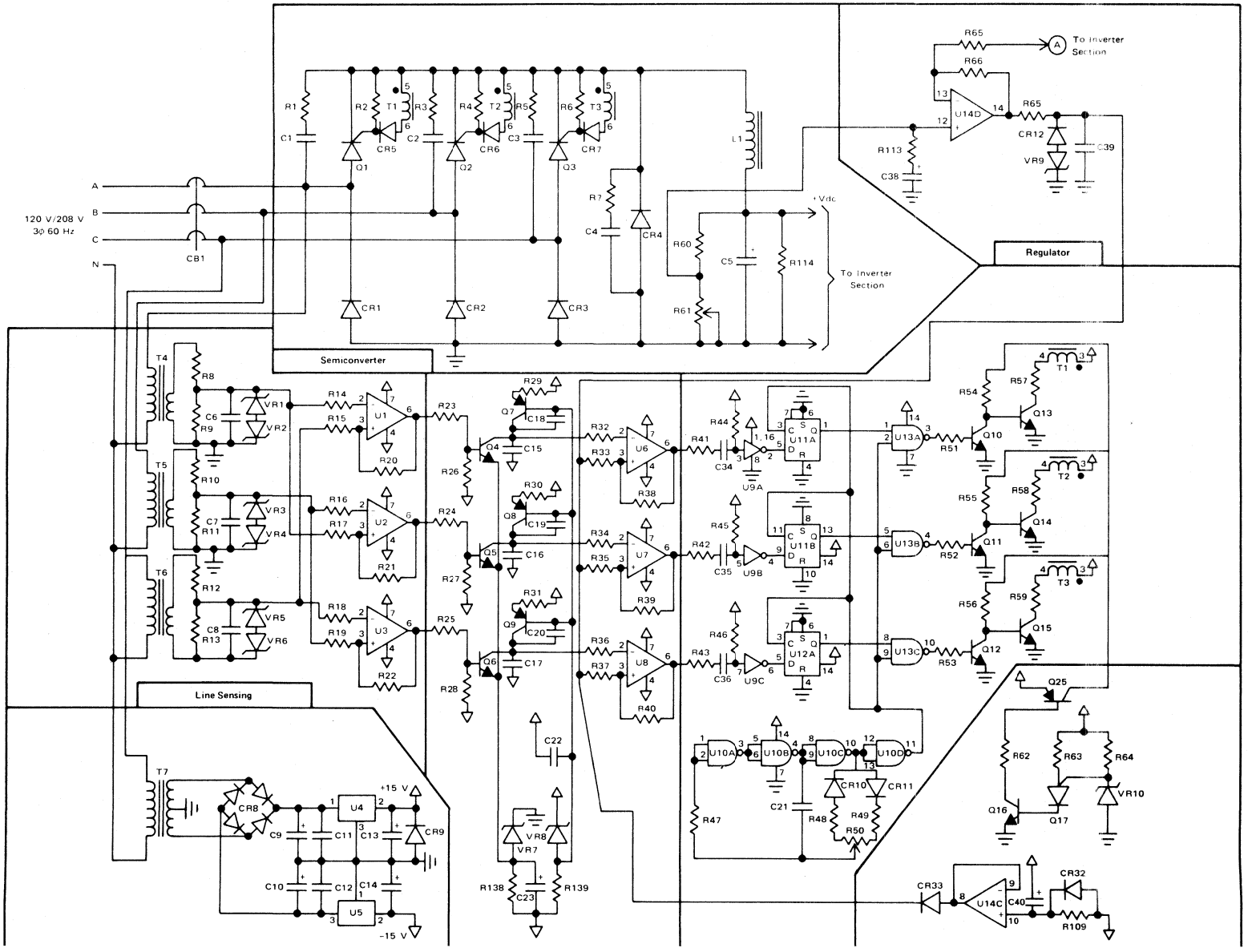
The dc bus voltage, Vdc, is inverted into quasi-squar excitation by the bridge inverter section. The driv frequency of the inverter is generated by the VCO circui which feeds the quasi-square wave generator. The output of the quasi-square wave generator determine the all important conduction sequence of the bridge inverte transistors, as shown in Figure 5b. Note that the leadin edges of these outputs are delayed approximately 30 μ by the dead time circuit in order to insure that opposin bridge legs are not on simultaneously, thereby, creating momentary but destructive short across the dc bus. Th delayed waveforms are buffered and then finally fed t the bridge inverter power circuit. The complete circui schematic is shown in Figure 7.

[3]For further information on this firing technique, see Motorola Engineering Bulletin, EB-44, "An Isolated, Picket-Fence Firing Circuit for High-Current SCRs."

PARTS LIST FOR FIGURE 7

Unless otherwise noted, all resistors are 5%, 1/4 W and capacitors are 25 W Vdc.

C1–4:	0.1 μF, 250 Vrms
C5:	2200 μF, 350 V Electrolytic
C6–8:	0.01 μF, 50 V
C9, 10:	1000 μF, 30 V Electrolytic
C11, 12, 22:	0.1 μF
C13, 14:	10 μF, 30 V Electrolytic
C15–17:	0.47 μF Matched to 2%
C18–20, 25, 37:	0.01 μF
C21:	250 pF
C23, 38:	100 μF, 25 V Electrolytic
C24:	20 μF, 25 V Electrolytic
C26:	10 μF, 25 V Electrolytic
C27, 41:	22 pF
C28–33:	270 pF
C34–36:	1 nF
C39:	0.02 μF
C40:	1 μF, 25 V Electrolytic
CB1:	15 A, 3φ Circuit Breaker
CR1–4:	MR756
CR5–7:	MR810
CR8:	MDA922-2
CR9:	1N4001
CR10–33, 38:	1N4001 or 1N914
F1–3:	15 A, 300 Vdc Fast Blow Fuse
L1:	12 mH, 20 A, 60 Hz Filter Choke
Q1–3:	2N6398
Q4–6:	MPS-A20
Q7–9:	2N3906
Q10–12, 16, 18, 34, 38, 42:	MPS5172
Q13–15:	MJE182
Q17:	2N6027
Q19–21:	2N6499
Q22, 26, 30:	2N6520
Q23, 27, 31, 35, 39, 43:	2N5657
Q24, 28, 32, 36, 40, 44:	MJ10001
Q25:	MJE170
R1–6:	220 Ω
R7:	470 Ω
R8, 10, 12:	6.2 kΩ, 1%, 1 W
R9, 11, 13:	1 kΩ, 1%, 1 W
R14–19, 62, 67, 107, 108, 111–113, 115, 116, 122, 128, 134:	1 kΩ
R20–22:	4.7 MΩ
R23–25:	4.7 kΩ
R26–28, 32–37, 41–43, 73, 78, 79, 81, 83, 85, 88, 119, 125, 131:	10 kΩ
R29–31:	4.3 kΩ, 1%
R38–40:	10 MΩ
R44–46:	200 kΩ
R47:	130 kΩ
R48:	33 kΩ
R49:	68 kΩ
R50:	50 kΩ, 1/4 W Trimpot
R51–53:	15 kΩ
R54–56:	300 Ω, 1 W
R60, 65, 66, 74–76, 86, 87, 90, 91:	100 kΩ
R61:	5 kΩ, 10 Turn Trimpot
R63:	13 kΩ
R64:	470 Ω
R68:	1.8 kΩ
R69:	1 kΩ, 1/2 W Pot
R70:	100 Ω
R71, 72:	200 kΩ, 1/4 W Trimpot
R77, 84:	47 kΩ
R80:	3.9 kΩ
R82:	4.7 kΩ
R89:	100 kΩ
R92–97:	110 kΩ
R98, 101, 104:	2 kΩ
R99, 102, 105:	2.7 kΩ
R100, 103, 106:	3.3 kΩ
R109:	1 MΩ
R110, 140:	22 kΩ
R114:	10 kΩ, 20 W
R120, 126, 132:	30 kΩ
R121, 127, 133:	200 Ω, 1 W
R137:	100 Ω, 1/4 W Trimpot
R138:	100 Ω, 1 W
R139:	5.1 kΩ
S1:	SPDT on R69
S2:	SPDT Toggle
T1-3:	Sprague 66Z930 Pulse Transformer
T4-6:	120 V Pri, 40 V Sec at 50 mA
T7:	120 V Pri, 25.2 VCT Sec at 2 A
U1-3, 6-8:	MLM301AP1
U4:	MC7815CP
U5:	MC7915CP
U9, 17, 23:	MC14049
U10, 13:	MC14011
U11, 12, 16, 18:	MC14013
U14, 15:	MC3403P
U19:	MC14510
U20:	MC14028
U21, 22:	MC14025
U24:	MC14050
U25:	MC14002
VR1-6:	Back-to-Back 1N5241, 11 V, 1/2 W
VR7:	1N5348, 11 V, 5 W
VR8:	1N5232, 5.6 V, 1/2 W
VR9:	1N4739, 9.1 V, 1 W
VR10:	1N5242, 12 V, 1/2 W
VR11, 12:	Back-to-Back 1N5239, 9.1 V, 1/2 W


120 V/208 V
3φ 60 Hz
A
B
C
N
CB1
Semiconverter
Regulator
Line Sensing
To Inverter Section
+Vdc
To Inverter Section
+15 V
-15 V

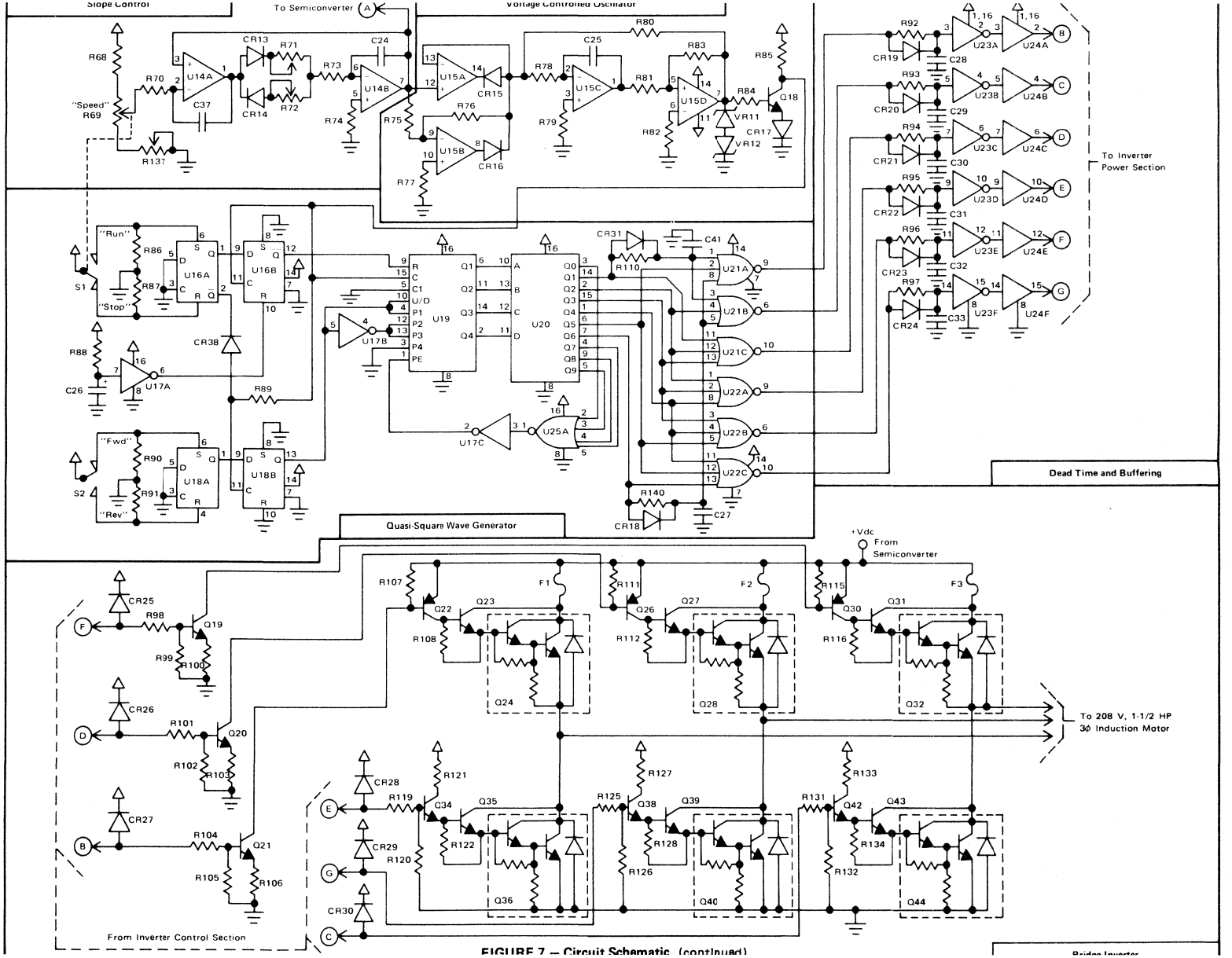


FIGURE 7 — Circuit Schematic (continued)

CIRCUIT DESCRIPTION

Line Sensing Circuit

Line-to-line voltage zero crossings are detected by first transforming down the line-to-neutral voltages with T4-6 and then comparing these voltages using U1-3.

Timing Circuit

The line-to-line zero crossing signals from U1-3 reset the ramp and pedestal timing circuits which determine the firing signal's timing, and, in turn, the semiconverter SCRs' conduction angle. For example, when $\phi A > \phi C$, (V_{CA} zero crossing) the output of U1 goes low, turning off Q4 which had been holding C15, the timing capacitor, at the pedestal voltage of -11 V. With Q4 off, the constant current source, Q7, charges C15. The voltage on C15 then linearly ramps positively. U6 compares this voltage with the control voltage from the output voltage regulator U14D. When the capacitor voltage exceeds this control voltage, the output of comparator U6 goes low, producing the firing command signal for Q1 in the semiconverter. A similar sequence is true for Q5, Q6, Q8, Q9, U7 and U8.

Drive Circuit

The firing signals from U6-8 trigger 200 μs one-shots formed by R41–46, C34–36, and U9. U11 and U12 synchronize the outputs of U9 to the clock formed by U10. This clock runs at a frequency of approximately 22 kHz and a duty cycle of 44%, which is adjusted by R50. The outputs of U11 and U12 are "anded" with the clock by U13 to produce a "picket-fence" pulse train. These pulse trains are amplified by Q10-15 and applied to the semiconverter SCRs' gates by isolation transformers T1-3.

Semiconverter and Filter Circuit

Q1-3 and CR1-3 form the semiconverter power section. R1, R3, R5, and R7, together with C1-4, form snubbers to limit the dV/dt of transient spikes appearing across Q1-3. CR4 is a free-wheeling diode which conducts lagging filter current allowing Q1-3 to commutate off. The filter is composed of L1 and C5. R114 is the filter bleeder resistor.

Regulator Circuit

Since the output voltage, Vdc, of the phase-controlled rectifier can vary with loading, especially at smaller conduction angles, closed loop control of Vdc was included. U14D compares the value of Vdc to the control voltage from the slope control circuit and adjusts the timing circuit control signal to obtain the correct value of Vdc. R61 sets the value of Vdc at a given drive frequency and is adjusted to give a Vdc of 267 V when the drive frequency is 60 Hz.

Start-Up Circuit

In order to insure that during initial power-up system circuits are fully operational, Q16, Q17, Q25 inhibit the SCR gate drive signals until the po supply voltage has reached ≈12 V. In addition, U provides a "soft start" feature, assuring an initi low, gradually increasing SCR conduction angle c this inhibit is removed.

Slope Control Circuit

The slope control circuit limits the maxir acceleration and deceleration rates of the excita voltage and drive frequency, and is composed of U and B. R71 and R72 adjust the maximum decelera and acceleration rates, respectively. R69 sets the ste state values of motor excitation voltage and freque R137 sets the minimum value of motor excitation is adjusted to produce a motor drive frequency of 2 Hz when R69 is at its minimum setting. This all the motor to operate with a 1 or 2 Hz slip freque when starting, giving maximum starting torque wi minimum of motor current.

The output of the slope control feeds the semic verter regulator and inverter VCO, thus control the bus voltage and drive frequency simultaneously.

VCO Circuit

U15 forms a linear VCO where output frequenc six times the drive frequency and is controlled by output of the slope control circuit. It has a ra from a few Hz to over 600 Hz, allowing drive frequen to 100 Hz. The output is translated and squared by Q18 to a form suitable for driving the CMOS qu square wave generator.

Quasi-Square Wave Generator

The quasi-square wave generator consists of U19 U19 is an up/down counter clocked by the V Its output is fed into U20, a BCD-to-decimal deco The outputs of U20 are coded by U21 and U22 form the drive signals for the inverter bridge, and of the form shown in Figure 5b. R140, R110, C C41, CR18 and CR31 form delay networks to elimi a race condition in the generator circuit. This form generator circuit has the advantage of possessing false output states, as opposed to some gener circuits using flip-flops.

The direction of rotation is controlled by S2, motor operation by S1. Note that S1 is interloc to R69. This prevents the motor starting at drive quencies other than that set by R137. In addit reversal of motor rotation while running is prever by CR38 and R89, which prevent U18B from b clocked. U16A and U18A debounce S1 and S2, spectively. Their outputs are synchronized with clock by U16B and U18B.

Dead Time and Buffering Circuit

The rising edges of the inverter bridge transistor base drive signals from U21 and U22 are delayed for 30 μs by CR19-24, R92-97, and C28-33. This "dead-time" insures that opposing bridge transistors are not on simultaneously because of transistor storage times. U23 and U24 buffer these signals and their outputs drive the bridge transistors.

Bridge Inverter

The inverter bridge transistors are composite multiple device PNP and NPN darlingtons. Q22-24, Q26-28 and Q30-32 form the PNP darlingtons, while Q35, Q36, Q39, Q40 and Q43, Q44 form the NPN darlingtons. Each darlington can handle up to 15 A of motor current. Q34, Q38, and Q42 drive the NPN darlingtons and Q19-21 provide a constant current drive for the PNP darlingtons. Q24, Q28, Q32, Q36, Q40 and Q44, the output transistors, are monolithic darlingtons. Constant current drive for the PNP darlingtons was necessary as the bus voltage, Vdc, can vary from a few volts to 280 V.

This quasi-complementary NPN/PNP darlington configuration was used as it does not require additional power supplies to provide drive for the upper inverter bridge transistors.

CR25-30 provide a measure of protection for the preceding CMOS circuitry in the event of transistor failures. The internal diodes of Q24, Q28, Q32, Q36, Q40 and Q44 clamp the maximum voltage across the power transistors to Vdc and provide paths for lagging and regenerative motor currents.

Snubbing and load line shaping was found to be unnecessary due to tight circuit layout, slow transistor switching times ($\cong$17 μs due to lack of turn-off drive), and the ability of the MJ10001 darlington switching transistors to safely turn-off into the 15 A, 300 V clamped inductive load.

OPERATING PRECAUTIONS

The two major operating precautions, in relation to the drive system are: (1) when the motor is decelerated, regeneration be limited so the dc bus voltage does not exceed 300 V, and (2) peak transistor currents not exceed 15 A. Regeneration is controlled by the rate of deceleration, while the acceleration rate is primarily determined by the maximum allowable transistor current.

Maximum safe acceleration rates can be increased for a given motor by increasing the current capabilities of the semiconverter and inverter. Maximum allowable deceleration rates can be increased by adding a switched resistive load to the dc bus during regeneration. This will dissipate the kinetic energy being fed back into the filter capacitor at this time.

SYSTEM PERFORMANCE

The system was tested using an induction motor with the following nameplate ratings:

Voltage	208 V
Current:	4.3 A
Frequency:	60 Hz
Pole Pairs:	2
Continuous Horsepower:	1
Continuous Torque:	3.3 lb-ft
Full Load Shaft Speed:	1750 RPM

With a slip frequency of 1.66 Hz, a constant 3.3 lb-ft of output torque could be obtained at shaft speeds from 0 to 1750 RPM; and from 1750 to 3000 RPM, a constant power output of 1 horsepower could be obtained. Peak motor current never exceeded 9 A under steady state conditions indicating that this system could be used to excite up to 1½ horsepower motors. Inverter bridge transistor and motor current waveforms are shown in Figure 8. Maximum unloaded motor acceleration to 1795 RPM and deceleration times of 2 s and 3 s, respectively, could be obtained without exceeding the 15 A transistor current limits. Cogging at low drive frequencies was not severe. System line current requirements, efficiency, etc. are given in Table 1 for full load and no load conditions.

Additional refinements to this system would be the inclusion of a resistive load that would automatically switch across the Vdc bus when regeneration occurs, automatic drive shutdown if motor current exceeds 15 A, and closed loop tachometer feedback for precise speed regulation.

TABLE 1

(f_{drive} = 60 Hz)

	No Load	Full Load
Line Voltage	208 Vrms	208 Vrms
Line Current	1.2 Arms	4.5 Arms
VA	432 VA	1.632 kVA
Current Form Factor	2.58	5.29
Watts In	225 W	825 W
Watts Out	–	746 W
Efficiency	–	90%

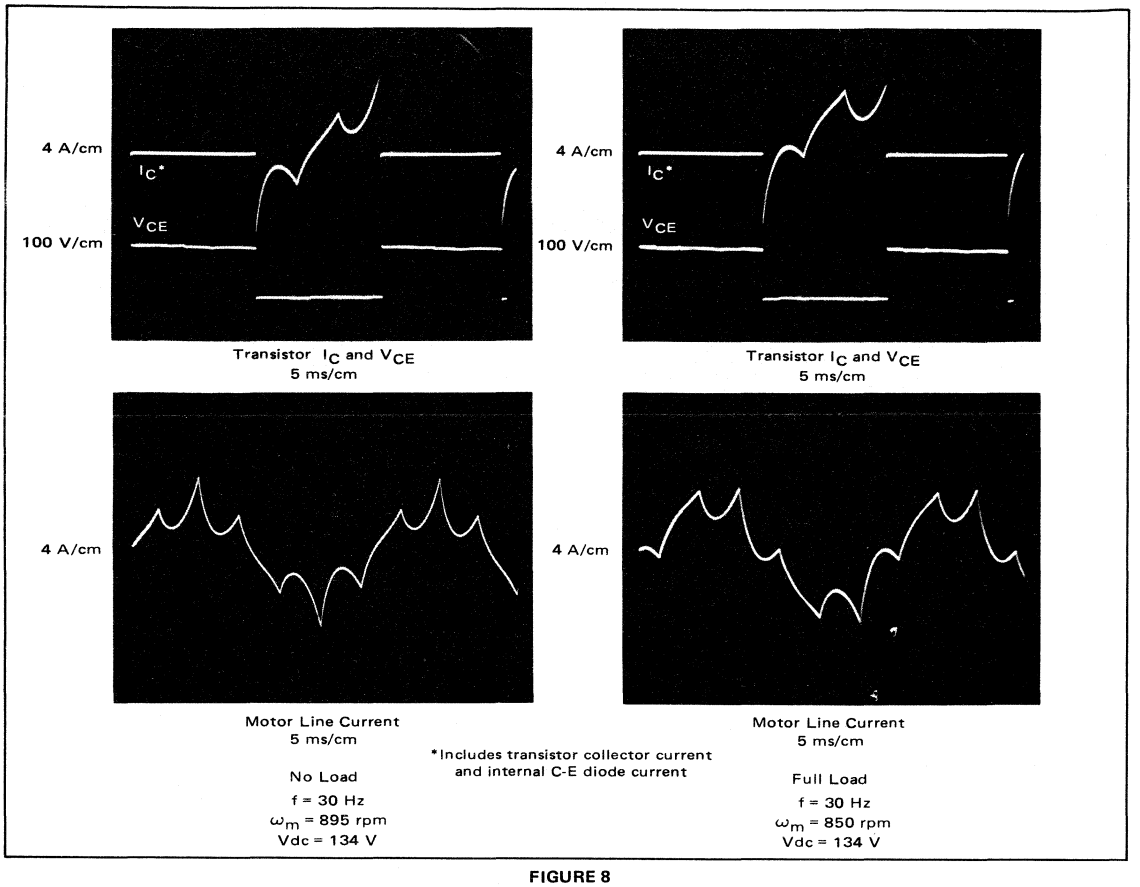


FIGURE 8

APPENDIX

Calculation of maximum value for Vdc for rated motor operation.

1. Assume that the rms value of the fundamental component of the excitation voltage should be equal to the motor name-plate operating voltage.

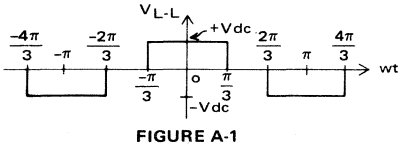


FIGURE A-1

2. The quasi-square wave line-to-line motor voltage waveform of Figure A-1 can be represented by the following Fourier expansion:

$$V_{L\text{-}L} = \sum_n a_n \cos nwt$$

where n = 1, 5, 7, 11, 13, 17, . . .

and

$$a_n = \frac{2}{\pi}\int_o^{\pi} V_{L\text{-}L} \cos nwt \, d(wt)$$

3. Solving for the peak value of the fundamental component:

$$a_o = \frac{2}{\pi}\int_0^{\pi} V_{L\text{-}L} \cos wt \, d(wt) = \frac{4\,Vdc}{\pi}\int_0^{\frac{\pi}{3}} \cos wt \, d(wt)$$

$$a_o = \frac{4\,Vdc}{\pi}\left(\frac{\sqrt{3}}{2}\right) = 1.102\,Vdc$$

4. Determine value for Vdc based on the assumption of #1 .

$$a_{o(rms)} = \frac{1.102\,Vdc}{\sqrt{2}} = 0.779\,Vdc$$

$$V_{rms} = a_{o(rms)} = 208\,V = 0.779\,Vdc$$

Solving,

$$Vdc = \frac{208\,V}{0.779} = 267\,V$$

AN-767

Application Note

A LINE OPERATED, REGULATED 5 V/50 A SWITCHING POWER SUPPLY

Prepared by:
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Geneva, Switzerland

This application note describes a regulated 220 V ac to 5 Vdc converter using high voltage switching transistors and Schottky barrier rectifiers. The control functions are all performed by integrated circuits.

MOTOROLA *Semiconductor Products Inc.*

A LINE OPERATED, REGULATED 5 V/50 A SWITCHING POWER SUPPLY

INTRODUCTION

Almost all electronic circuits require a dc voltage supply with some degree of stabilization. The voltage is normally obtained by rectifying and filtering an ac voltage. The desired stability is produced by the action of certain regulating circuits.

The most widely used regulator is the series linear regulator which is essentially a controlled voltage divider. The ratio of this divider is controlled such that the output voltage remains at a constant level for all specified changes of input voltage and load current. This type of regulator has outstanding properties as far as load and line regulation, noise and regulation response time are concerned. It is particularly suitable for those applications where linear operational amplifiers have to be supplied and noise can be a problem, or where a very high degree of stability is required. On the other hand, a lot of power is dissipated in these regulators because their efficiency is rarely higher than 50 percent. Higher efficiency, however, at the expense of slower regulation response time and higher noise levels, can be achieved by series switching regulators.

In a series switching regulator, the filtered dc input voltage is chopped by a series switching element, in general, a switching transistor. The resulting rectangular pulse train is filtered by a low pass filter, yielding a smooth dc voltage at the output of the filter. The value of this voltage is determined by the duty-cycle of the chopper and can therefore be stabilized electronically by controlling the duty-cycle, with respect to a reference voltage. This type of regulator offers noise and regulation performances that are always inferior by one order of magnitude to the corresponding linear regulators. They are therefore best suited for supplying less critical loads, like digital circuits. The losses in a series switching regulator are caused mainly by the voltage drops of the saturated switching transistor, the forward voltage drop of the freewheeling diode and the power dissipation during the commutation of the switching transistor. Efficiencies up to 85 percent can be obtained with this system.

Both types of series regulator use a transistor as the controlling element which has not only to withstand the full input voltage but also to carry the full load current. Therefore, both systems usually need a line transformer in order to produce the lowest possible input voltage to the regulator. Transformers operating at 50 or 60 Hz that have to transmit several hundred volt-amperes are heavy and bulky components and frequently prove difficult to place in equipments that have to be compact. The availability of high voltage transistors capable of carrying several amperes collector current have made it possible to design inverter-type switching regulators working directly off the line voltage without an intermediate 60 Hz transformer.

These inverter switching regulators offer noise and regulation performances similar to the series switching types and can replace them in most applications where price is not the ultimate requirement. They can be built to be more compact and light-weight, at the expense of slightly more complicated electronics, than the equivalent series switching units.

Inverter regulators use either two or four switching transistors for chopping the rectified line voltage at ultrasonic frequency (usually between 20 and 50 kHz) before applying it to a compact power transformer designed for operation at this frequency. The transformer, generally a step-down, is followed by a rectifier and a smoothing filter to obtain the dc output. The basic inverter configurations of transistors are the full bridge and its derivatives, the push-pull and the half bridge. A discussion of the properties of the last two circuits is presented in AN737 (ref. 1). The choice between these circuits depends on specific conditions such as magnitude of the line voltage, available switching devices, desired output power, etc. In brief, the full bridge is mainly used for obtaining very high output powers, above 1 kW. For medium and low output powers the half bridge and push-pull are preferred; they require two high power transistors but only two drivers, as compared to four smaller transistors and four drivers for the full bridge. The disadvantage of requiring transistors of higher power is compensated by a simpler driving circuit.

For high line voltages (typically 220 V) the half bridge is preferred to the push-pull because it requires lower voltage transistors. For low line voltages (typically 115 V) the simplicity of the driving circuit of a push-pull inverter makes it generally preferable to the half bridge, although its potential ability to draw destructive dc current through one leg of the output transformer and also sometimes the necessity of having to isolate electrically the transmission of the output voltage magnitude to the control electronics may require extra efforts to find suitable solutions.

In this note a system is described which uses a half bridge Pulse Width Modulated Inverter to generate a 5V/50A output from 220 volts ac lines.* The switching transistors,

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

*Operation from a 115 V ac line is possible if a full-wave voltage doubler is used.

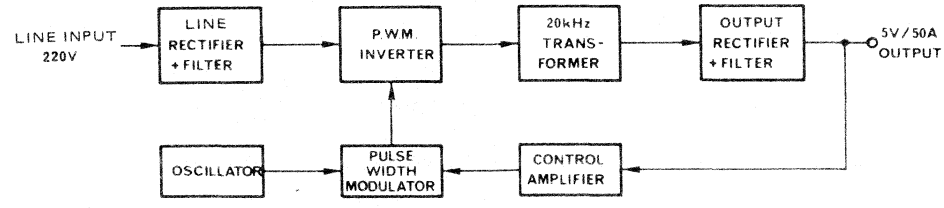


FIGURE 1 – POWER SUPPLY BLOCK DIAGRAM

operated at 20 kHz, are used to produce an ac voltage which is stepped down by a ferrite core transformer to an appropriate value. The secondary voltage of the transformer is rectified and filtered to yield the smoothed 5 Vdc output. Regulation of the output voltage is achieved by controlling the duty cycle of the switching waveforms.

DESCRIPTION OF THE SYSTEM

General

A block diagram of the complete system is shown in Fig. 1. Rectifying and filtering the line voltage yields a 310 Vdc voltage which provides the supply voltage for the dc-dc converter generating the 5 volts output.

The control circuitry consists basically of a Pulse Width Modulator, a clock oscillator and a control amplifier. The control pulses generated by the P.W.M. are at clock frequency and have a duration dictated by the control amplifier.

The input circuit

The input circuit can be seen in detail in figure 2; it consists of a rectifier and a smoothing capacitor. Nominal line voltage is 220 volts, 50–60 Hz. The minimum voltage for a full power output is 190 Vac and the maximum, for the elements selected here, is 260 Vac corresponding to 268 and 367 peak dc volts respectively. The line is rectified by an MDA 806 bridge and filtered by an electrolytic capacitor of 600 μF. This gives a ripple voltage of 15 volts peak-to-peak at full load and at nominal input voltage. The current flowing from the capacitor to the inverter under these conditions is 1.1 amps dc. The current through the rectifier bridge is 2.4 amps rms.

P.W.M. inverter

The half bridge inverter circuit shown in figure 2 consists of capacitor C_1 and C_2, transistors TR_1 and TR_2 and transformer T_1.

The capacitors C_1 and C_2 divide the dc supply voltage approximately to its mid-value (155 Vdc). These capacitors also prevent any net dc voltage being applied to the primary of T_1. Transistors TR_1 and TR_2 are alternately turned ON and OFF, producing across the primary of T_1 the stepped ac waveform indicated in the upper half of figure 3, the same waveform that appears across the switching transistors. The current in one transistor is indicated in the lower half of figure 3. At the beginning and at the end of the conduction period the collector-emitter voltage of each transistor changes ideally by half the inverter dc supply voltage (155 volts). The full dc voltage of 310 volts appears at the transistor collector only after the transistors are completely cut-off and draw no more collector current. The peak switching power which the transistors have to handle is therefore, theoretically, the product $1/2\ V_{CC} \times I_C$.

In practice the switch -off portion of the load line tends to extend up to the point $V_{CC} \cdot I_C$ due to stray inductance in the power transformer. Use of an RC snubber network in parallel with TR_2 is therefore recommended to keep the load line within the Reverse Bias Safe Operating Area of the switching devices. A practical result obtained with such a technique is illustrated in figure 4.

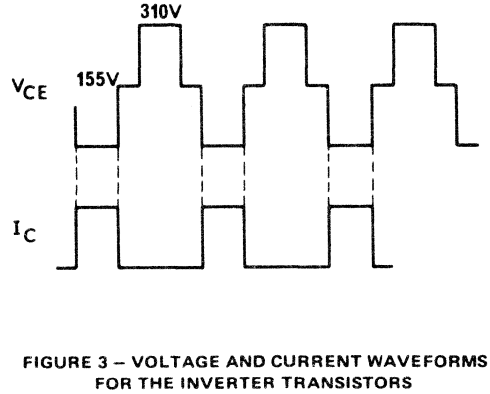


FIGURE 3 – VOLTAGE AND CURRENT WAVEFORMS FOR THE INVERTER TRANSISTORS

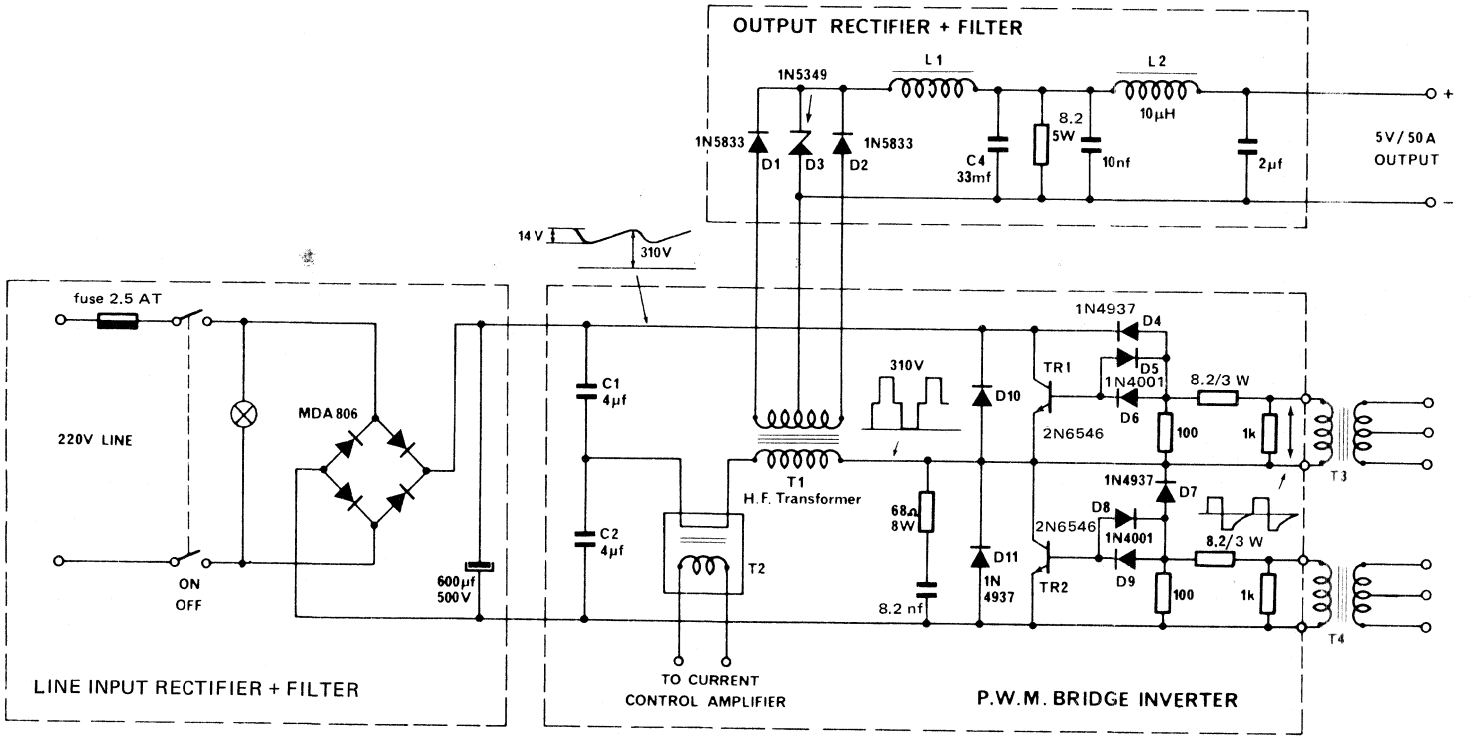
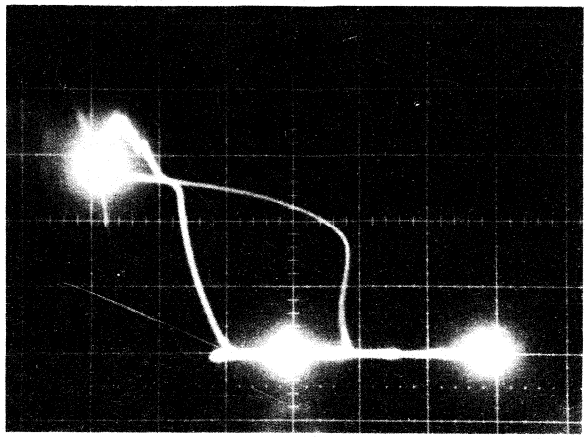


FIGURE 2 – HALF BRIDGE DC-TO-DC CONVERTER



Vertical: 1 A/Div.
Horizontal: 50 V/Div.

FIGURE 4 – LOAD LINE OF THE INVERTER TRANSISTORS AT FULL LOAD

The transistors used in the present design, 2N6546, are fast high voltage devices capable of switching currents of 8 A at 350 volts level. In order to keep the devices switching at high speed throughout the complete range from full output load to no-load, great care has to be taken in the design of the base driving circuits. Here, as illustrated in figure 2, use is made of a diode network for avoiding saturation of the transistors. The diodes D_4 up to D_9 very effectively maintain full switching speed for the transistors with any load. A fast recovery type of diode has to be selected for D_4 and D_7.

The transistor dissipation is about 20 watt for both devices together at full load. The required heatsink should have a thermal resistance of about 2.5°C/watt in order to keep the junction temperature below 120°C for a 50°C ambient temperature.

Special care is needed in the design of the ultrasonic frequency power transformer. The winding technique has to be such as to minimize the leakage inductance in order to avoid large voltage overshoots affecting transistor commutation. An interleaved structure was adopted for the transformer windings as shown in figure 5. The primary winding consists of three windings in parallel, the two halves of the secondary winding are sandwiched between the primary ones.

In addition to proper winding techniques, high frequency wiring rules must be observed in order to minimize RF interference and parasitic oscillation.

The following is the specification for transformer T_1:

Core Philips P 66/56 – 3H1
Np = 33 turns of 0.6 mm dia wire
Ns = 2 turns of 1 x 6 mm flat wire

The current transformer T_2 is used as the detector for the current control loop to limit the output at 50 A. When loaded with 10 kΩ, it provides a signal of about 0.4 V/A.

Construction data for T_2 are as follows:

T_2: Core Telmag HWR 4/5/4, single loop
Np = 1
Ns = 1000 turns of 0.2 mm dia wire

C_1 and C_2 are metallized polyester capacitors with a 20 kHz impedance of approximately 2Ω each. The ultrasonic frequency ripple across them at full load is about 5 volts pk-pk.

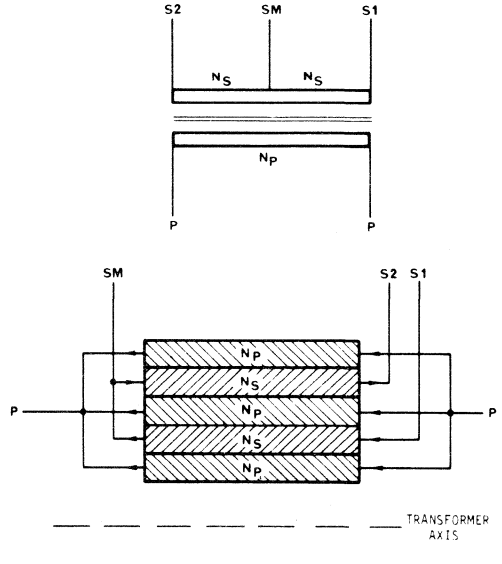


FIGURE 5 – WINDING TECHNIQUES USED FOR THE TRANSFORMER T 1

Output rectifier and filter

The voltage at the secondary of transformer T_1 has an amplitude of approximately 9 volts at nominal input voltage. This voltage is rectified by two 40A/30V Schottky rectifiers which provide a very efficient high current rectification. The thermal power dissipation of these devices at full load is approximately 20 watts each and a heat sink of at least 1.3°C/W is required to keep their junction temperature below 125°C at an ambient temperature of 50°C. Schottky diodes are very sensitive to over-voltages even in the form of short spikes; a simple zener diode D_3 protects them against spikes above 2 x V_Z and greatly increases the reliability of the system.

The output filter consists of two LC sections with following data:

L_1 Core Telmag HWR 40/24/4, double loop with a 1.5 mm airgap, 23 windings of copper sheet 55 x 0.4 mm

L_2 1 cm^2 iron core with 4 windings of copper flat wire 6 x 1 mm.

The first filter section has a series resonance frequency of about 400 Hz for greater attenuation of the ripple at the working frequency and above. The 100 Hz ripple is reduced by the regulating circuit itself, by as much as 70 dB. The second filter section attenuates the residual commutating spikes which can pass the first filter section by virtue of the winding capacitance of L_1.

A fixed preload of 8.2Ω maintains a minimum of conduction time in the switching transistors and avoids large shifts in the dc level at the junction of C_1 and C_2. Such shifts would increase the switching power in the switching devices when large loads are suddenly applied.

The control circuitry

The control circuitry is shown in figure 6; it includes all the electronic circuits necessary to produce a stabilized dc output voltage with a limited dc output current, by controlling the duty cycle of the switching power transistors TR_1, and TR_2 of the inverter. It also contains an overvoltage protection circuit and a reset circuit. Using quad operational amplifiers, the whole circuit needs only 5 IC packages and a few discrete elements, and can easily be built on a 10 x 16 cm circuit board.

Two control amplifiers provide the necessary loop gain to stabilize either the output voltage or the output current with respect to a given reference. The gain of both feedback loops can be controlled by adjusting the gain of the amplifiers. No particular frequency compensation of the loops was required for their stability.

The Pulse-Width-Modulator consists of a linear ramp generator and three voltage comparators. The linear ramp generator, employing a MC1455 and a small signal transistor, also produces the system's clock frequency. The linear ramp is separately compared to the outputs of the two control amplifiers and also to a pre-set fixed limiting voltage, by three MC3302. The outputs of these three comparators are connected together in a wired "OR" so that preference is given to the one defining the shorter pulses (i.e. the one defining the lower output voltage). Control of the output voltage is dictated by the voltage loop, up to an output current of approximately 50 A. Above 50 A the current control loop defines the pulse width and causes the output voltage to decrease. The fixed voltage provided by the Limiter defines the maximum length of the pulses and consequently guarantees that in all circumstances (particularly if the input voltage is too low) the switching transistors are both disabled for a few μs at each half cycle. This time, set by potentiometer P_1, is required for the conducting transistor to recover completely before the other transistor is driven ON.

The inverter has to be started with a low duty cycle in order to prevent a large starting pulse (in terms of volt-seconds) from driving the transformer core into saturation and possibly causing high inrush current into the switching transistors. A low duty-cycle start-up network has therefore been foreseen in combination with the Limiter. When the Reset push-button is pressed, capacitor C_5, initially discharged, causes the Limiter comparator to assume control of the duty cycle and to keep it to a very low value. C_5 is then slowly charged-up through R_5 and the duty cycle is progressively increased until control is taken up by the voltage or the current loop.

The phase splitter provides the correct routing of the pulses from the P.W.M. to the power transistors'drivers. It uses one D-flip-flop MC14013 and two gates MC14023. The pulse train can be stopped by the reset circuit; the drivers and the output power transistors are then automatically disabled.

The power transistors' drivers are self-commutating push-pull drivers providing electrically isolated signals to the power transistors by means of the transformers T_3 and T_4. Data for these transformers are as follows:

Core 3H1 18/11

Np = 2 x 60 turns of 0.25 mm dia wire

Ns = 15 turns of 0.5 mm dia wire

While a positive driving pulse is being transmitted to the bases of the power transistors, energy is stored in the core of these transformers. At the end of each pulse this energy is liberated at the secondary of T_3 and T_4 in the form of a negative 5V pulse applied across the emitter-base junction of the power transistors, resulting in fast recovery of the transistor. During development, it was found useful to include a small fuse in series with the transistors' bases to protect the driving circuits in case of accidental transistor failure.

The overvoltage detector compares the output voltage to a reference by means of a programmable unijunction transistor (PUT). If the output voltage exceeds that reference (typically 6 volts) the PUT is triggered and generates a pulse, which, amplified by an MC3302, clocks the reset circuit. An optional thyristor crowbar could easily be added to short the output of the supply so as to avoid damaging the load.

The purpose of the reset circuit, a D-flip-flop MC14013, is to stop the system's clock and disable the output drivers. It is set upon command of the overvoltage detector as well as each time the power supply is switched on, so that it

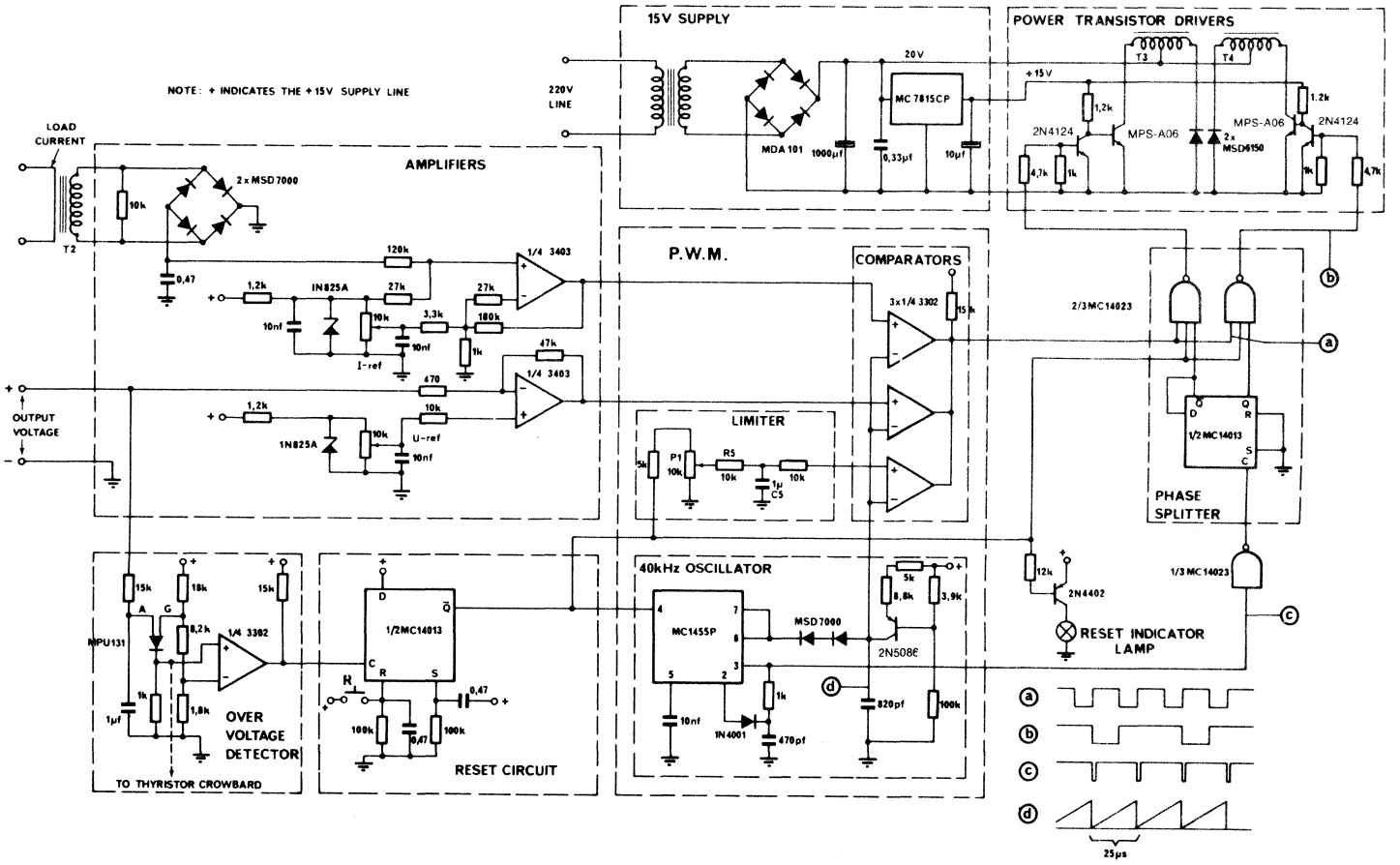


FIGURE 6 – CONTROL CIRCUITRY

insures that the correct supply voltages are present when the clock is enabled. A push button on the front panel allows the circuit to be reset for starting operation.

Performance of the power supply

The output voltage is stable to within +0.2% and -0.3%, for a line voltage variation between 190 and 260 volts and currents up to 50 A.

Output ripple has a maximum of 25 m volts rms measured with a bandwidth from 10 Hz to 10 MHz. Ripple amplitude is 60 mV peak-to-peak.

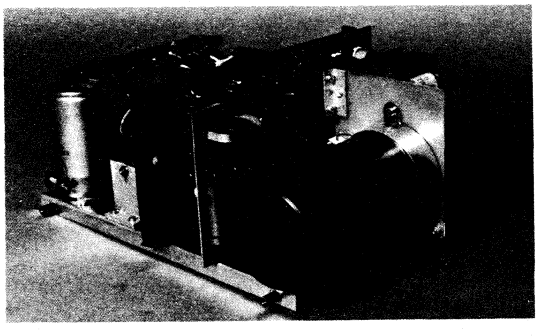
Overall efficiency of the power supply at full load is approximately 75%.

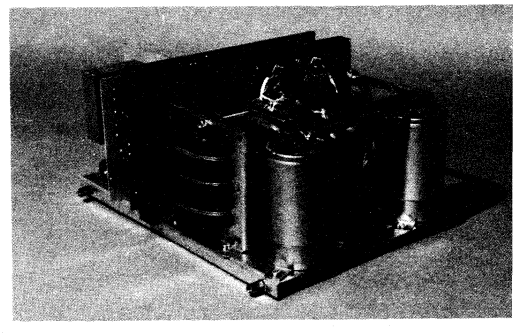
CONCLUSIONS

The design of a 5 V/50 A switching power supply working directly off the line has been illustrated. It has been shown how modern power transistors and high frequen rectifiers can be used in a high performance and yet simp design. Notable simplification of the control circuits w achieved by the use of quad operational amplifiers a quad comparators operated from the same single supp used for the CMOS logic circuits.

The magnitude of the output voltage of a power supp such as the one described here, depends on the choice the turns ratio of the output transformer and on t suitability of the output rectifier and filter. Only the parts and the gain of the voltage control amplifier wou have to be adapted to obtain a 250 watt supply havi almost any output voltage.

Ref. 1. Haver, R.J. – Switched Mode Power Supplies Highlighting a 5V, 40A Inverter Design, AN–73 Motorola Semiconductors Products Inc.





APPENDIX

Estimation of the critical value of the bridge capacitors C1, C2

C1 and C2 should be selected large enough to ensure good efficiency of the power supply, an upper critical value exists however which may lead to saturation of the power transformer T_1 if the switching transistors are not perfectly matched. A quick method for estimating this critical value is given here, it is based on a number of simplifying assumptions leading to an approximate, but worst-case result.

It is supposed that the supply is unloaded, that the resistive components in T_1 are negligible and that a difference exists between the on-time of TR1 and the on-time of TR2. This difference initially gives rise to a net dc voltage ΔV across the primary of T1. ΔV causes a current I_1 in T_1 having the form: $I_1 = \Delta V \sqrt{\frac{2C}{L}} \cdot \sin\left(\frac{t}{\sqrt{2LC}}\right)$

where C is the common value of C1 and C2 and L is the value of the primary inductance of T1.

In the worst case I_1 has to be added to the current in due to the switching square wave: $I_2 = \frac{Vdc}{4L} \cdot t_{on}$

where Vdc is the rectified line voltage and t_{on} the eq alent on-time of the power transistors.

If saturation of transformer T_1 is to be avoided, then total magnetizing current has to be lower than its satu tion current I_{sat}:

$$\Delta V \sqrt{\frac{2C}{L}} + \frac{Vdc}{4L} \cdot t_{on} < I_{sat}$$

This condition allows the determination of C for a gi set of the other parameters.

As an example, if I_{sat} = 0.3 A, L = 15 mH, Vdc = Volt, t_{on} = 20 μs and ΔV = 6 Volts due to a differe of 2 μs between the on-time of TR1 and TR2, then value of C is 8.5 μF.

MOTOROLA
Semiconductor Products Inc.

AN-785
Application Note

REVERSE BIAS SAFE OPERATING AREA

Prepared by
Bob Bailey

The rating of high voltage, high speed switching transistors for safe turn-off operations is examined. Clamped inductive turn-off measurements are used to generate a switching RBSOA—reverse bias safe operating area—which can be used in conjunction with load line analysis to assure proper transistor operation. The effects of inductance, temperature, base turn-off conditions and forward base drive on RBSOA are included in the discussion.

TRODUCTION

Construction of power transistors with increased ltage, current, and speed required for applications such switching power supplies, motor controls, and horizon- deflection has necessitated compromises in capability handle turn-off switching energy. The specification pically used to show capability in this mode has been n-clamped Es/b, which was established many years o as a figure of merit for extremely rugged, low voltage nsistors generally used in series pass applications. though modern devices can handle many thousands volt-amperes during switching intervals, in general ey have limited capability in avalanche. Therefore, to ply a non-clamped Es/b specification to the newer vices, one has to severely limit the time actually spent the transistor in avalanche, making the choice of coil, rn-off base conditions, and collector current very licate. The resulting specification has in most cases en of limited value to the circuit designer.

The use of a switching RBSOA (or just RBSOA) ɔt is proposed, similar to familiar forward-bias SOA, demonstrate capability to handle turn-off switching ergy. The circuit designer can then compare his turn-off ıd line with the RBSOA plot. Knowing his turn-off nditions and how they affect RBSOA, he can make sure ıt his design will not stress the transistor to the point degradation or failure.

JRN-OFF AND RBSOA

In switching applications, two key parameters related turn-off conditions are of interest to the circuit signer: storage time and switching losses. In many designs, storage time of pairs of devices must be either matched or greatly minimized to avoid saturation of magnetic cores; the alternative is fairly complex control circuitry. Storage time also can limit the range of regulation. Switching losses are of concern because they affect efficiency and determine required heat sinking for reliable operation. Figure 1 and 2 show switching waveforms for resistive and clamped inductive turn-off loads for a high voltage, high current Darlington. At 20 kHz, this device under these conditions would generate 13.2 watts of switching loss with a resistive load and 19 watts with an inductive load. Note that the inductive load generates much higher peak energy than the resistive load, and indeed could cause second breakdown failure if the RBSOA capability of the device is exceeded.

FIGURE 1 — Resistive Switching Turn-off Waveforms

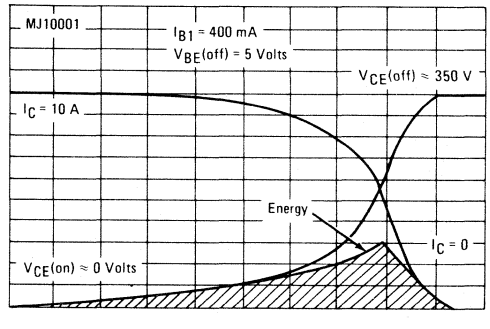
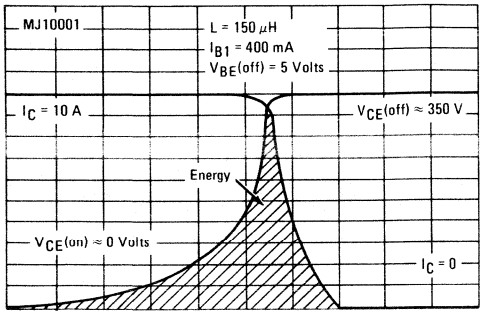


FIGURE 2 – Clamped Inductive Switching Turn-off Waveforms



Figures 3 and 4 show, respectively, t_{sv} and t_c versus base turn-off voltage for the high voltage Darlington and for a high voltage, moderate current discrete. (t_{sv} is defined as storage time from 90% I_{B1} to 10% V_{CE} and t_c as commutation time from 10% V_{CE} to 10% I_C in a clamped inductive switching circuit.) Obviously, a designer would choose $V_{BE(off)}$ to be as high as possible to minimize t_c (switching losses) and t_{sv}.

Es/b

Degradation and/or failure of a transistor in the turn-off mode can be caused by Es/b reverse-bias secondary breakdown energy. Whereas Is/b occurs with energy concentrated at the emitter periphery, Es/b is different in many ways from Is/b forward-bias secondary breakdown, since the concentration of energy on the chip is focused during turn-off to the center of the emitter. Es/b can occur below actual device avalanche, and can be

FIGURE 3 – Storage Time versus $V_{BE(off)}$

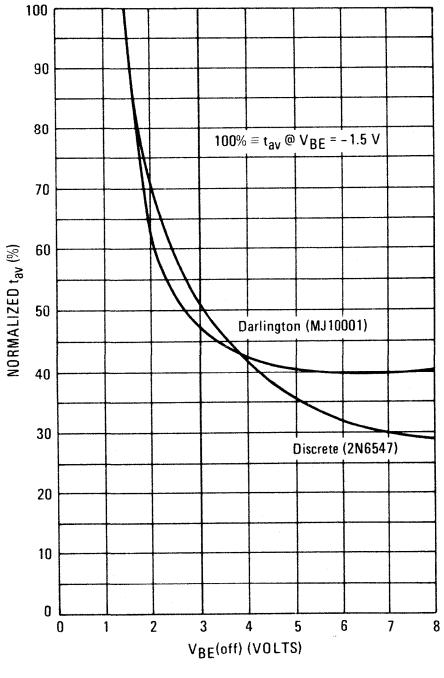
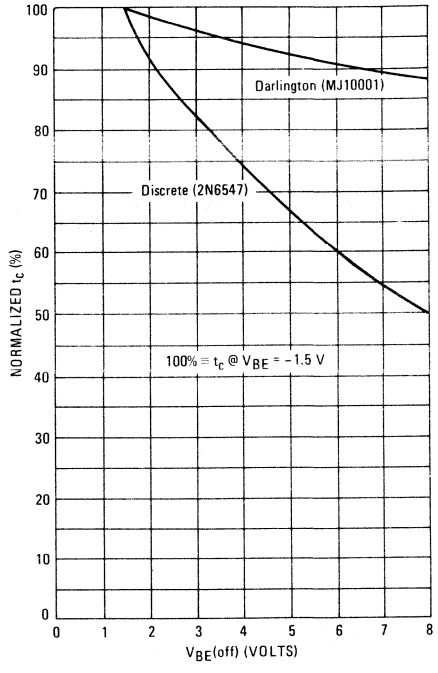


FIGURE 4 – Commutation Time versus $V_{BE(off)}$



less than Is/b for certain V-I combinations in a given device. And, as might be expected, it behaves differently from one device construction to the next.

From the earlier discussion, it seems apparent that one should use high off-bias to minimize storage time and switching losses. What does this do to second breakdown capability? Below actual device avalanche, increased off bias can improve capability, and under avalanche conditions, capability can be decreased. This has led to some confusion about how a device should be rated, and how it should be operated to achieve satisfactory reliability.

The traditional method of rating reverse-bias second breakdown has been with an unclamped inductive switching circuit, as shown in Figure 5. The energy rating is calculated as:

$$Es/b = 1/2 L_{(eff)} I_C^2$$

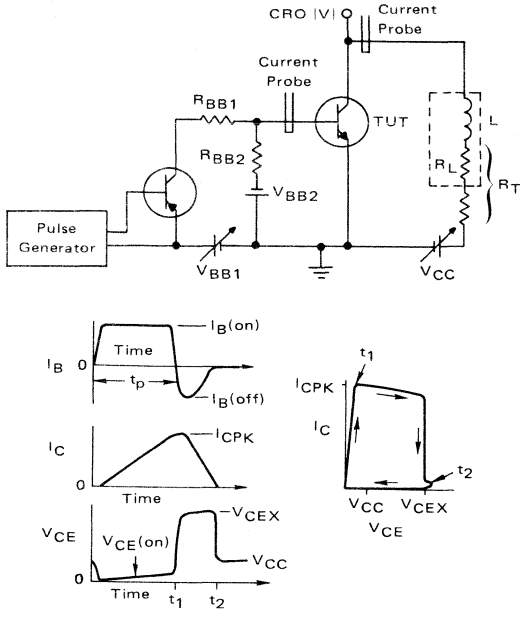
where $L_{(eff)} = \dfrac{V_{CEX}}{V_{CEX} - V_{CC}} L$.

If the inductor and collector current are high enough and if the TUT turn-off time is fast enough, the TUT will go into a collector avalanche mode, clamping the voltage at $V_{CEX(sus)}$. As stated earlier, the energy that a device can withstand in actual reverse-bias avalanche is small for high voltage, high speed transistors; therefore, reverse-bias second breakdown energy (often referred to simply as Es/b for this rating system) is many times specified with open base turn-off or with very high base impedance. This yields very high Es/b compared to hard turn-off conditions—in fact, ratings range from millijoules to joules

and indeed device capability varies by orders of magnitude depending upon conditions. In most cases, the circuit designer is interested in the hard turn-off conditions, under which unclamped Es/b seldom exceeds several millijoules.

FIGURE 5

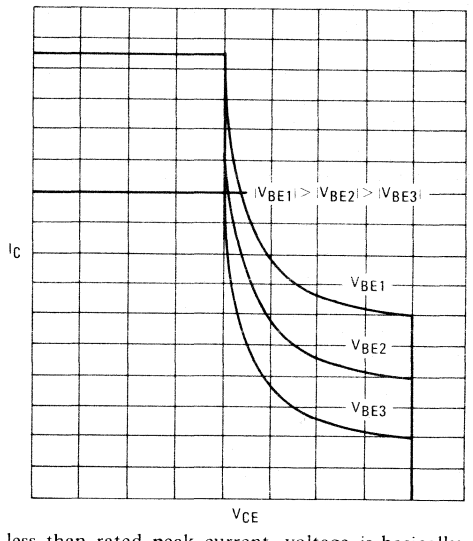
Suggested test circuit for verifying specifications of safe operating area for switching between conduction and cutoff with an unclamped inductive load, and waveforms while switching. (From JEDEC Suggested Standard No. 10, Jan. 1976)



AN ALTERNATIVE–RBSOA

Figure 6 shows a rating system–switching RBSOA–which is applicable to modern switching transistor applications. In form, it is similar to the very familiar forward-bias SOA plot. Collector current is constrained to be equal to

FIGURE 6 – Switching Reverse Biased Safe Operating Area (RBSOA)

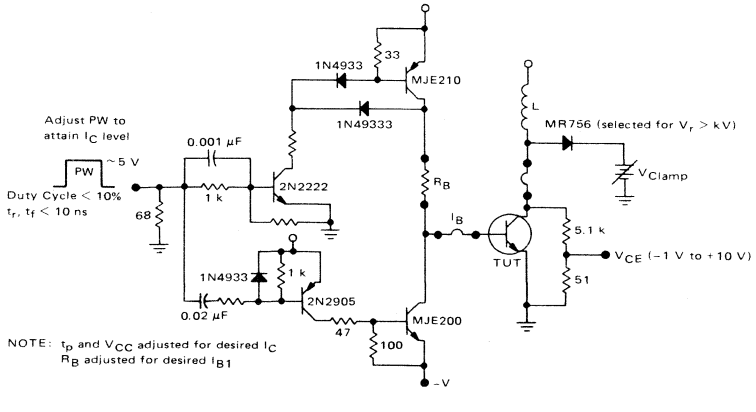


or less than rated peak current, voltage is basically constrained by maximum V_{CEX}, and the high simultaneous V-I portion is constrained by energy-handling capability. Following is a discussion of details of generating this rating, and the effect of variables such as inductance, temperature, turn-off bias, etc.

One circuit which can be used to verify switching RBSOA capability is shown in Figure 7. In this circuit, R_B and the +5 volt supply can be adjusted to set the desired I_{B1}, and V_{CC} and t_p are adjusted for desired I_C. Turn-off is accomplished via the MJE200 connected to -V. I_{B2} is determined by the TUT; if controlled I_{B2} is desired, resistance can be added to the turn-off circuit.

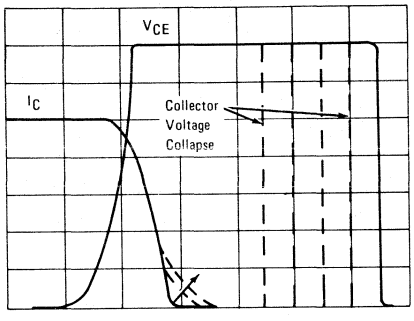
The collector circuit consists of V_{CC}, inductor L and a clamp circuit comprised of the MR756 connected to a clamping supply. To profile switching RBSOA of a device, one can either set V_{Clamp} and vary I_C, or fix I_C and vary V_{Clamp}, in each case detecting failure or onset of failure.

FIGURE 7 – Switching RBSOA Test Circuit (Clamped Inductive Testing)



Some devices "serve notice" just prior to breakdown, by exhibiting an increase of collector current near the tail end of on-time, as shown in Figure 8. If voltage or current is increased beyond this point, breakdown occurs and collector voltage collapses. This is usually destructive.

FIGURE 8 – Onset of RBSOA Failure



Switching RBSOA for a high voltage, high current discrete device is shown in Figure 9. The sharp-cornered "L"-shaped area shows the specified RBSOA for $V_{BE(off)} \leq 5$ volts per the data sheet. Actual profiled curves for a typical device are also shown for $V_{BE(off)}$ = 3 volts and 9 volts. Notice that RBSOA capability increases for increased $V_{BE(off)}$.

FIGURE 9 – High Current Discrete RBSOA

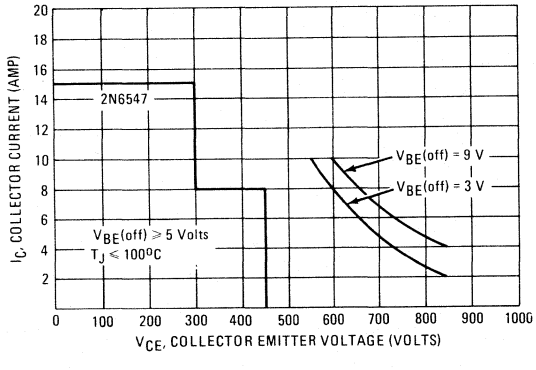


Figure 10 shows specified switching RBSOA for two high voltage, moderate current discrete devices. Below BV_{CEO}, RBSOA is not dependent on off-bias and the safe area is limited by the maximum I_C rating. Above BV_{CEO}, the collector current must be derated as shown and is very dependent upon off-bias. The higher the bias, the greater the safe area.

FIGURE 10 – Moderate Current Discrete RBSOA

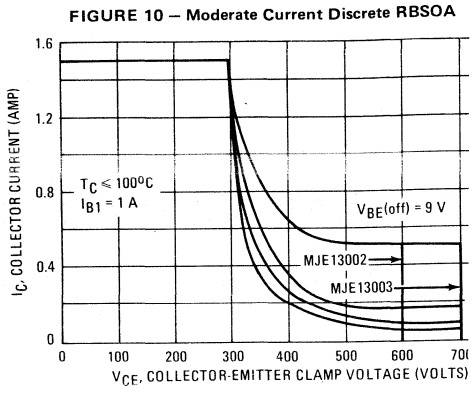
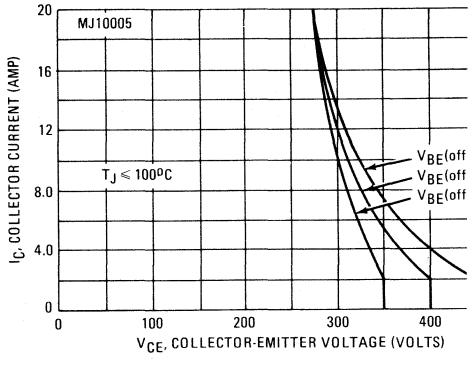


Figure 11 shows the specified RBSOA for a voltage, high current Darlington. Current is const to maximum continuous collector current. In the limited region, capability is again seen to incre $V_{BE(off)}$ is increased.

FIGURE 11 – High Current Darlington RBSOA



The fact that the shape of the specified RBSOA differs so much between devices in these exam attributable to the evolution of rating technique as ledge of device behavior has increased.

EFFECT OF VARIABLES

To understand how RBSOA applies for d operating conditions, the effect of several key v must be examined. First, what is the effect of indu and, therefore, load line? Most turn-off load line the range between pure resistance and pure indu It was noted that worst-case stress is imposed u device by pure inductive loads. Adding resista a given inductor decreases stress and is safe so lon load line is maintained within the rated RBSOA.

Tests have shown that the inductance value measurable effect on RBSOA. For very low valu collector load line "droops", as the voltage E = I

slowly, controlled by di/dt or current fall time dt
ıe device. At high inductance values, collector voltage
kly rises to V_{Clamp} at turn-off, but the stress on the
:e remains essentially unchanged as inductance is
ıer increased, since the inductive energy is transferred
he clamping circuit as soon as the device turns off.
is representative of most circuit load line clamping
ıaping techniques except, perhaps, those which turn
device back on at a given voltage such as utilization
collector-base zener. This is a special case which
bines both reverse- and forward-bias stresses, and is
within the scope of this discussion.

second very important factor is the effect of tem-
ture. Data taken to date indicates that RBSOA is
ively unaffected by temperature at high currents,
there does appear to be a definite decrease in RBSOA
increasing temperature at high voltages and low
ents. Obviously, in rating a given device, the range of
)erature over which RBSOA is guaranteed should be
ified.

$V_{BE(off)}$, having a strong effect on storage time and
:hing losses, is also important to the designer; there-
, its effect on RBSOA is of interest. For the devices
ied and reported upon, RBSOA always increased
$V_{BE(off)}$ was increased. It must be remembered,
ever, that device avalanche was purposely avoided,
is, clamped inductive rather than unclamped inductive
were run. In avalanche, a device can generally handle
: energy at lower $V_{BE(off)}$. This latter case is not
idered to be revelant since operation of a device
out the protection of either clamp diodes or snubbers
ıt recommended.

s a final note to the effect of $V_{BE(off)}$: The data
rted was restricted to $V_{BE(off)} < V_{EBO}$, that is, in
:ase was the emitter-base junction avalanched. It is
well known that turn-off switching times can be decreased by avalanching the emitter-base junction,[1,2] particularly in the case of Darlingtons without internal speed-up diodes. A form of this technique has been employed in television deflection applications with success—extending it for use in other switching applications is under consideration at present.

To complete the study of variables, the effect of I_{B1} on RBSOA was examined, and no measurable effect was noted. This included overdrive to the point of $I_{B1} = I_C$, and underdrive to the point where device saturation was just maintained.

CONCLUSION

The rating system offered—switching RBSOA—is believed to be pertinent for most switching applications, and it appears to be practical for transistor manufacturers to implement. With the assistance of this rating, the circuit designer can use one or more of several techniques to assure that his turn-off load line is constrained to be within rated RBSOA.

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MOTOROLA INC.
Semiconductor Group

AN-786
Application Note

POWER DARLINGTON LOAD LINE CONSIDERATIONS

Prepared by
Robert J. Haver

Power transistor load lines are discussed in the light of a typical application of a Switchmode(1) Darlington power transistor. Darlington advantages are reviewed and the test circuit is introduced. Load line analysis revealed a reverse bias SOA problem and just enough snubbing was used to insure reliability without unduly sacrificing efficiency.

WHY DARLINGTONS?

High voltage Darlingtons have more gain than their discrete counterparts. Forced gains required for saturation are 10 to 20 for Darlingtons and 2 to 5 for equivalent discretes. Also, they are more cost-effective than the two equivalent discrete devices they replace, and above the 5–10 A level compete directly with the cost of discretes because they require less silicon for the same current capability.

Now that several companies are producing quality high speed, high voltage Darlingtons, these devices are being used much more in Switchmode supplies. The high gain reduces drive power requirements and simplifies driver design while the slightly higher saturation voltages are insiginificant in line-operated supplies. Some designers have been hesitant to accept this Darlington revolution, but most realize that significant technological advances have been made and that their companies can now realize additional cost savings by designing with Darlingtons.

With the advent of low drift base-emitter resistors and glassivated junctions, thermal problems have been overcome and maximum operating junction temperatures of 200°C are a reality. Also, it has been shown that a hybrid speed-up diode enhances switching performance without the need for a more expensive four terminal package. Turn-off performance is now as good as discretes and turn-on is even better as evidenced by comparative dynamic $V_{CE}(sat)$ tests.

Savings result primarily because smaller base drive transformers and driver transistors can be used. Actually, forward drive is substantially less than discretes, but reverse current requirements are identical. Savings are also tied to the cost of the power device itself as indicated above.

TEST CIRCUIT OVERVIEW

To illustrate the capabilty of a typical Switchmode Darlington and demonstrate the importance of load-line analysis, Motorola's MJ10005 (400 V/20 A) was used in a series switching regulator to supply a 200 V, 10 A load. Although this type of switching supply does not provide isolation from the line, it is used quite often as a preregulator for free-running inverters or simply as a dc-dc converter. When operating off line at 220 Vac (or from 120 V with a doubler) the nominal bus voltage is 320 Vdc and at high lines, it reaches 380 Vdc. Instead of operating from the ac line, a 380 Vdc supply was used to simulate worst-case operation of the regulator. In this case, closed loop feedback was not required. Instead, the regulator was run open loop with the output pulse width controlled manually. The performance summary of this regulator is as follows:

DC Input Voltage	380 V (250 V min)
Output Voltage	200 V
Output Current	10 A
Fixed Frequency (Variable PW)	20 kHz
Output Ripple	0.4 V_{p-p}
Output Spikes	40 Watts
Efficiency (after 60 Hz conversion)	98%

(1) Trademark of Motorola Inc.

This circuit requires an input rectifier and standard control logic to become a fully regulated, line-operated Switchmode power supply. Control logic can be implemented rather easily with Motorola's new inverter control IC (MC3420) or with a quad comparator (MC3302) as shown in AN-719. However, with just the power stage itself and its open loop control circuit, the following points were demonstrated:

- Load line shaping limits inductive turn-off spikes and improves reliability.
- Switchmode Darlington provides performance and cost incentives over discretes.
- Low base drive requirement simplifies the interface design.
- Pulsed turn-off drive enhances efficiency.
- A second high frequency LC filter suppresses electrical noise.

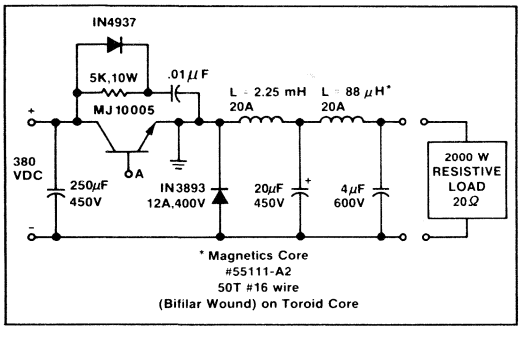

FIGURE 1 – Power Stage Schematic

TEST CIRCUIT DETAILS

The power stage schematic is shown in Figure 1. It contains the dc input voltage, the Switchmode Darlington, a snubber network, two LC filters, a fast recovery freewheeling diode, and the 2000 W resistive load. The transistor is driven from a fixed frequency, variable pulse width oscillator; and, output voltage is proportional to on time as follows:

$$V_O = (V_{in} \times t_{on})/T$$

Values for the main LC filter were chosen to keep operational current variations to 20% (2 A out of 10) and 20 kHz ripple at 1% of V_O (2 V out of 200). The approximate formulas are:

$$L = \frac{(V_{in} - V_O)}{\Delta I}\Delta t = \frac{(380 - 200)25\ \mu s}{2\ A} = 2.25\ mH$$

$$C = \frac{\Delta I \Delta t}{\Delta V} = \frac{2\ A \times 25\ \mu s}{2\ V} = 25\ \mu F$$

A laminated iron core 2 mH choke with a saturation level of 20 A and a standard 20 μF/450 V electrolytic capacitor were used. Values for the second and smaller LC filter were determined empirically. A permalloy toroid and a Mylar capacitor were used to reduce noise spikes due to the fast recovery rectifier from 25 V to 5 V. This second filter also helped reduce the 20 kHz ripple from 2 V to 0.5 V as shown in Figure 2.

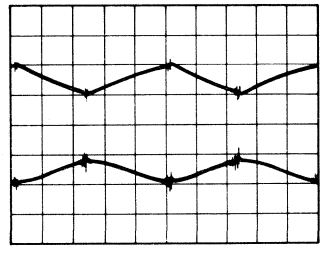

FIGURE 2 – Output Ripple (10 μs/cm)

The control stage schematic is shown in Figure 3. Here, a CMOS oscillator drives a four transistor push-pull base drive circuit. Both circuits operate between ±5 V supplies which are grounded and "float" at the emitter of the Switchmode Darlington.

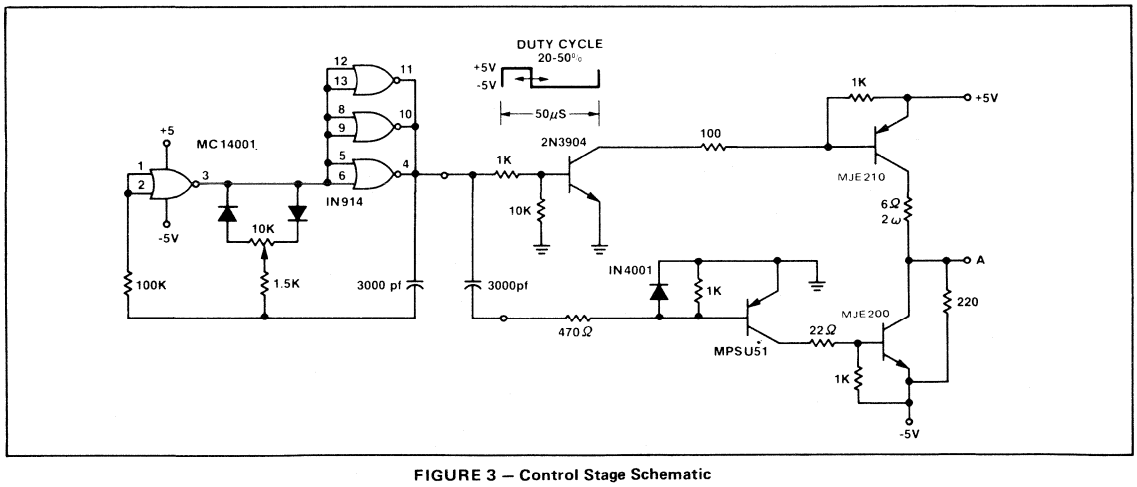

FIGURE 3 – Control Stage Schematic

Forward base drive is provided by the MJE210 and is limited to 0.5 A by the 6 Ω base resistor. To reduce storage and fall times, high voltage, low impedance off drive is recommended. For this reason, the MJE200 is directly connected to −5 V and reverse base current is limited mainly by the conductivity modulated lateral base resistance (r_B). Under these conditions, both power Darlingtons and discretes require a relatively high current driver (2 to 3 A). This drive is required for only a short time (5 μs), and should then be removed to keep from continuously drawing current through the output BE resistor (15 Ω). To accomplish this, a series RC circuit was added to the base of the predriver (MPS-U51). The results of this pulsed off drive system on I_B and V_{BE} are shown in Figure 4.

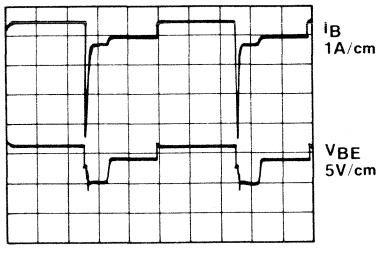

FIGURE 4 – Base Drive Waveforms (10 μs/cm)

Manual setting of the control potentiometer determines the pulse width and output voltage. When closed loop feedback is used, the control stage is usually located at the regulator output. In such a situation, the direct base drive circuits shown here must be replaced by a coupling transformer drive circuit, like those shown in Figure 5.

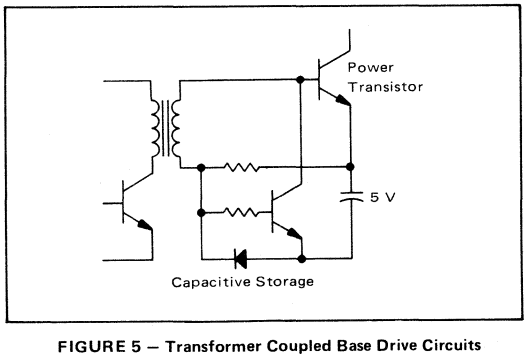

FIGURE 5 – Transformer Coupled Base Drive Circuits

To obtain good ripple rejection and input regulation, the feedback amplifiers must have high gain and adequate frequency response. To improve regulation, a second "feed-forward" loop may be added. In such a system both output and input voltages are fed to the control amplifiers. When input voltage increases, the amplifier "anticipates" that the output will increase a cycle later and compensates for this change by correcting the pulse width instantaneously. (See AN-752 for further information on this subject.)

TRANSISTOR CONSIDERATIONS

Since this is a Switchmode supply, the transistor must have a relatively low saturation voltage and fast switching speeds. It also must be able to switch reliably at high line (380 V) and have acceptable gain at the operating current level (10 A). Motorola's MJ10005 is an excellent choice for this application. It contains an internal hybrid BE diode to enhance switching performance and offers the following ratings and characteristics:

$V_{CEO}(sus)$ = 400 V at I_C = 250 mA
(Verified by clamped inductive tests)

$I_C(max)$ = 20 A, and

$V_{CE}(sat)$ = 2.0 V max at 100°C,

I_C = 10 A, and I_B = 400 mA

With the test conditions the same as specified for $V_{CE}(sat)$ and with $V_{BE}(off)$ = −5 V, typical switching times in microseconds are as follows:

Load	T_C	t_r	t_s	t_f
Resistive	25°C	0.2	0.60	0.15
Inductive	25°C	—	0.65	0.04
Inductive	100°C	—	0.85	0.10

To actually get the fast switching performance shown in Figure 6 requires both a fast device and proper base

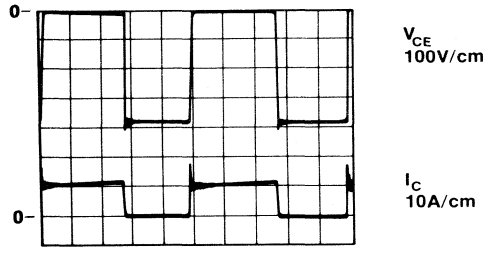

FIGURE 6 – Transistor Waveforms (10 μs/cm)

drive as discussed earlier. Although it does improve efficiency, fast switching can produce excessive noise and damaging voltage transients.

Electrical filters and magnetic shields are used to control noise. To control transients, close attention is required to mechanical layout (component placement) and lead length. The most critical loop is from the input cap to the transistor, the diode, and back. Bypass caps may be required and lead lengths should be kept short to minimize voltage spikes on the transistor.

LOAD LINE ANALYSIS

The question of how reliable the Darlington or any device is, in this application, can be addressed by checking to see how close it is operating to its SOA limits. To do this, a plot of the worst-case load line (an X-Y plot of I_C versus V_{CE}) must be obtained. In this application, the greatest switching excursions occur at high line (380 V) and rated load (10 A). A fast X-Y scope (Tektronix

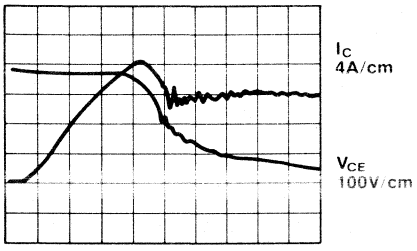

FIGURE 10 – Turn-On Waveform (50 ns/cm)

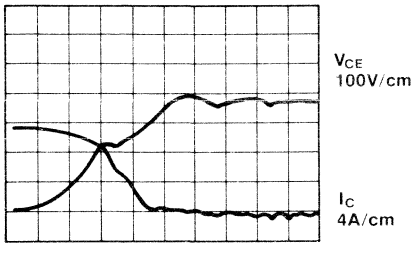

FIGURE 11 – Turn-Off Waveform (100 ns/cm)

for average current to determine base drive requirements and curve trace measurements were used to obtain transistor and diode "on" voltages which are quite difficult to measure in the circuit.

An equivalent discrete transistor, the 2N6547 (400 V, 15 A) was also operated in this circuit. In comparing the discrete and Darlington, it was noted that the base and collector "on" losses were the reverse of the Darlington, and the total was the same. The Darlington V_{sat} was higher (1.5 V versus 0.5 V), but the discrete required more base drive (2.0 A versus 0.5 A). This indicates either a Darlington or discrete could work equally well in this type of application. The final choice would have to be made by comparing switching speed and total circuit cost.

SUMMARY

The importance of load line shaping was stressed as a means of insuring reliable operation in a Switchmode power supply. The overall efficiency of 98% in this switching regulator at 100°C is exceptional. It is due primarily to the fast, high gain Darlington and to the shaping technique which minimized snubber losses. It is anticipated that demonstrated performance like this, along with cost incentives, will convince many designers to use Switchmode Darlingtons in their next design.

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3. D. Roark, "Base Drive Considerations in High Power Switching Transistors," TRW AN-120, January 1975.
4. J. Nappe and N. Wellenstein, "An 80 Watt Switching Regulator for CATV and Industrial Applications," Motorola AN-752, October 1975.

APPENDIX I

Snubber Formulas

1. To find C, estimate fall time.

$$t_f = 150\ \mu s\ @\ 25^oC,\ t_f = 300\ \mu s\ @\ 100^oC$$

$$C = \frac{I_t}{V} = \frac{10\ A \times 300\ \mu s}{380\ V} = 8\ nF$$

A 10 nF ceramic capacitor was used.

2. To find R, use a 50% discharge (0.7 τ) during the on time (20 μs)

$$R = \frac{t}{0.7\ C} = \frac{20\ \mu s}{0.7 \times 0.01\ \mu F} = 3\ k$$

A 5 k resistor was used.

3. To find P_R, use $P = E_f$ where

$$P = C\frac{(V_1^2 - V_2^2)^2}{2} f =$$

$$\frac{0.01\mu F(400^2 - 200^2)\ 20\ k}{2} = 12\ W$$

A 5 k, 20 W wire-wound resistor was used.

Circuit diagrams external to Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information in this Application Note has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

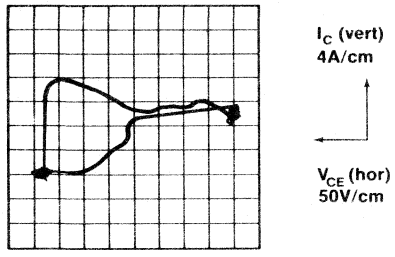


FIGURE 7 – Transistor Load Line

Model 536) was used to obtain the picture of this load line shown in Figure 7. Not all X-Y scopes will faithfully reproduce the switching loci because of limited bandwidth on the horizontal amplifier. The accuracy of the picture here was verified by checking it against the time base I_C and V_{CE} switching waveforms. Several time base scopes with an X-Y mode that have worked well for slower transistors did not work here.

Once the worst-case load line has been identified as either at high line or during power-up or power-down, the analysis is a relatively simple matter of comparing this to the published switching SOA capability of the device. (See Figure 8.) The turn-on load line should be within

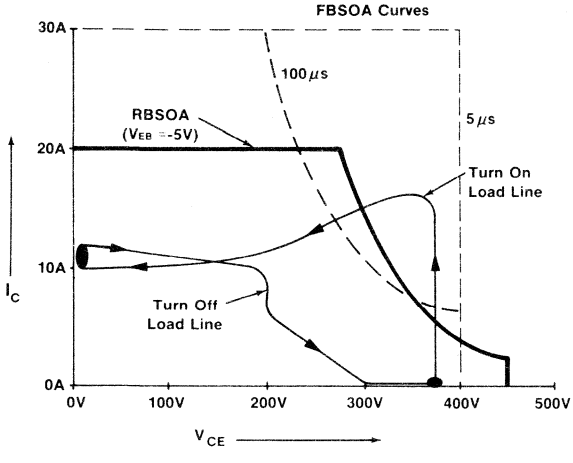


FIGURE 8 – MJ10008 Load Line Analysis Switching (10 A at 380 V)

the pulsed forward biased SOA curves (FBSOA). The turn-on load line here lasts for about 300 ns (the free-wheeling diode recovery time) and is beyond the published 100 μs FBSOA. However, more recent tests indicate this device will sustain more than 30 A at 400 V for 5 μs. The turn-on load line (16 A, 380 V) is well within this pulsed FBSOA capability.

The turn-off load line is analyzed in an identical manner and must be within the reverse bias SOA limits (RBSOA). When the circuit was originally tested without the RC snubber, this was not the case (see Figure 9).

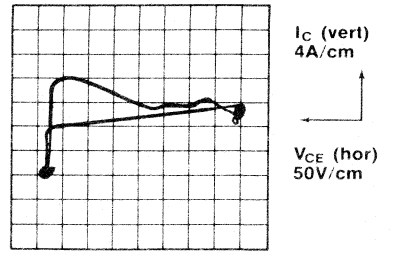


FIGURE 9 – Transistor Load Line (Without Snubber)

The 8 A, 380 V load line excursion is beyond the 5 A, 380 V point on the RBSOA curve.

In this situation, random failures of the Darlington were occurring as the input voltage was raised to 380 V. Because of this, the snubber network was required to assure reliable turn-off at high line voltages. The design formulas are shown in Appendix I. The effect of this snubber can be observed by referring to Figure 7 or 8. To improve efficiency, the resistor does not completely discharge the capacitor and does leave about 200 V on it. Therefore, the turn-off load line remains inductive to about 200 V and then becomes resistive as the capacitor absorbs the inductive energy and keeps the load line well within the RBSOA limits. The snubber does become less effective as the transistor heats and turn-off time increases. It was for this reason that these load lines were all checked at an elevated case temperature of 100°C.

EFFICIENCY

Table 1 shows a summary of power losses measured at high line and rated load (380 V, 10 A) with both the transistor and diode case at 100°C.

TABLE 1

Power Loss	Amount
SM Darlington Turn-On (due to fast recovery diode)	15 W
SM Darlington Turn-Off	4 W
Snubber Resistor	12 W
SM Darlington Saturation	7 W
Fast Recover Diode	5 W
Base Driver Power	3 W
Miscellaneous Filter Losses	2 W
Total	48 W

$$\text{Overall efficiency} = \frac{2000}{2048} \times 100 = 98\%$$

(after 60 Hz conversion)

Switching losses were obtained by integrating the area under the turn-on and turn-off waveforms shown in Figures 10 and 11. Turn-on loss is considerable, and could definitely be improved if faster fast recovery rectifiers were available. The snubber loss is determined by calculating energy transfer from the capacitor and multiplying by the frequency. Low voltage supplies were monitored

MOTOROLA
Semiconductor Products Inc.

AN-789
Application Note

CHARACTERIZING THE SCR FOR CROWBAR APPLICATIONS

Prepared by
Al Pshaenich
Senior Applications Engineer

The use of a crowbar to protect sensitive loads from power supply overvoltage is quite common and, at the first glance, the design of these crowbars seems like a straightforward relatively simple task. The crowbar SCR is selected so as to handle the overvoltage condition and a fuse is chosen at 125 to 250% of the supply's rated full-load line current. However, upon further investigation, other questions and problems are encountered.

How much overvoltage and for how long (energy) can the load take this overvoltage? Will the crowbar respond too slowly and thus not protect the load or too fast resulting in false, nuisance triggering? How much energy can the crowbar thyristor (SCR) take and will it survive until the fuse opens or the circuit breaker opens? How fast will the fuse open, and at what energy level? Can the fuse adequately differentiate between normal current levels – including surge currents – and crowbar short circuit conditions?

It is the attempt of this application note to answer these questions–to characterize the load, crowbar, and fuse and thus to match their characteristics to each other.

The type of regulator of most concern is the low voltage, series pass regulator where the filter capacitors to be crowbarred, due to 60 Hz operation, are relatively large and the charge and energy stored correspondingly large. On the other hand, switching regulators operating at about 20 kHz require smaller capacitors and thus have lower crowbar constraints.

These regulators are quite often line-operated using a high voltage, two-transistor inverter, half bridge or full bridge, driving an output step-down transformer. If a transistor were to fail, the regulator-transformed power would be less and the output voltage would drop, not rise, as is the case for the linear series regulator with a shorted pass transistor. Thus, the need for overvoltage protection of these types of switching regulators is minimized.

This premise, however, does not consider the case of the lower power series switching regulator where a shorted transistor would cause the output voltage to rise. Nor does it take into account overvoltage due to transients on the output bus or accidental power supply hookup. For these types of operations, the crowbar SCR should be considered.

How Much Overvoltage Can The Load Take?

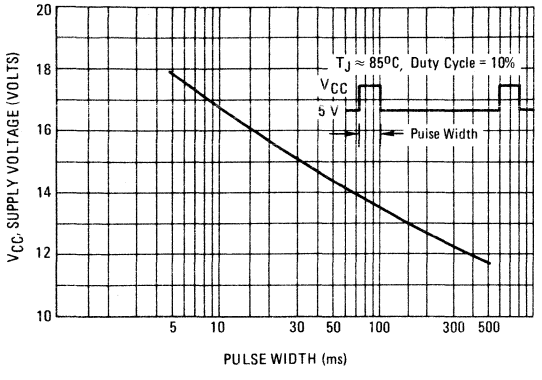
Crowbar protection is most often needed when ICs are used, particularly those requiring a critical supply voltage such as TTL or expensive LSI memories and MPUs.

If the load is 5.0 V TTL, the maximum specified continuous voltage is 7.0 V. (CMOS, with its wide power supply range of 3.0 to 18 V, is quite immune to most overvoltage conditions.) But, can the TTL sustain 8.0 V or 10 V or 15 V and, if so, for how long and for how many power cycles?

To conservatively specify the crowbar and fuse, the Safe Operating Area (SOA) of the TTL must be known. Unfortunately, this information is not readily available and has to be generated.

Using the test circuit illustrated in Appendix A, a quasi-SOA curve for a typical TTL gate was generated (Figure 1). Knowing this overvoltage-time limit, the crowbar and fuse energy ratings can be determined.

FIGURE 1 – Pulsed Supply Voltage versus Pulse Width



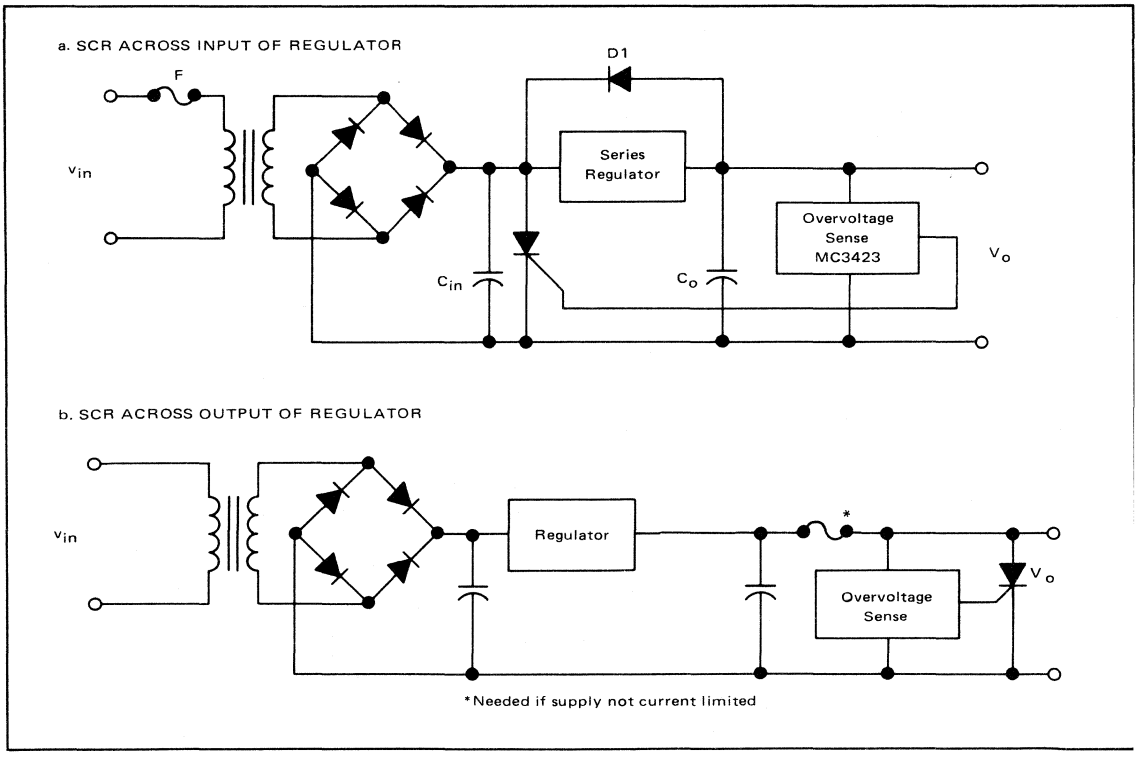
Where Is The Crowbar SCR Placed For Optimum Protection In The Series Regulator?

The two possible configurations are illustrated in Figure 2; the first case shows the crowbar SCR across the input of the regulator and the second, across the output. For both configurations, the overvoltage comparator senses the load voltage at the remote load terminals particularly when the IR drop of the supply leads can be appreciable. As long as the output voltage is less than that of the comparator reference, the crowbar SCR will be in an off state and draw no supply current. When an overvoltage condition occurs, the comparator will produce a gate trigger to the SCR, firing it, and thus clamping the regulator input, as in the first case – or output, as in the second case – to the SCRs on-state drop of about 1.0 to 1.5 V, thereby protecting the load.

Placing the crowbar across the input filter capacitors although effectively clamping the output, has several disadvantages.

1. There is a stress placed on the input rectifiers during the crowbarring short circuit time before the line fuse opens, particularly under repeated operation.
2. Under low line conditions, the minimum short circuit current can be of the same magnitude as the maximum primary line current at high line, high load making the proper fuse selection a difficult choice.

FIGURE 2 – Typical Crowbar Configurations



3. The capacitive energy to be crowbarred (input and output capacitor through rectifier D1) can be high.

When the SCR crowbar and the fuse are placed in the DC load circuit, the above problems are minimized. If crowbarring occurs due to an external transient on the line and the regulators current limiting is working properly, the SCR only has to crowbar the generally smaller output filter capacitor and sustain the limited regulator current.

If the series pass devices were to fail (short), even with current limiting or foldback disabled, the crowbarred energy would generally be less than of the previous case. This is due to the higher impedance of the shorted regulator (due to emitter sharing and current sensing resistors) relative to that of rectifier D1.

Fuse selection is much easier as a fault will now give a greater percentage increase in dc load current than when measuring transformer primary or secondary rms current.[1] The disadvantage, however, of placing the fuse in the dc load is that there is no protection for the input rectifier, capacitor, and transformer, if one of these components were to fail (short). Secondly, the one fuse must protect not only the load and regulator, but also have adequate clearing time to protect the SCR, a situation which is not always readily accomplished. The input circuitry can be protected with the addition of a primary fuse or a circuit breaker.

How Much Energy Has To Be Crowbarred?

This is dictated by the power supply filter capacitors, which are a function of output current. A survey of several linear power supply manufacturers showed the output filter capacitor size to be from about 100 to 400 microfarads per ampere with about 200 μF/A being typical. A 30 A regulator might therefore have a 6000 μF output filter capacitor.

Additionally, the usually much larger input filter capacitor will have to be dumped if the regulator were to short, although that energy to be dissipated will be dependent on the total resistance in the circuit between that capacitor and the SCR crowbar.

The charge to be crowbarred would be

$$Q = CV = IT,$$

the energy,

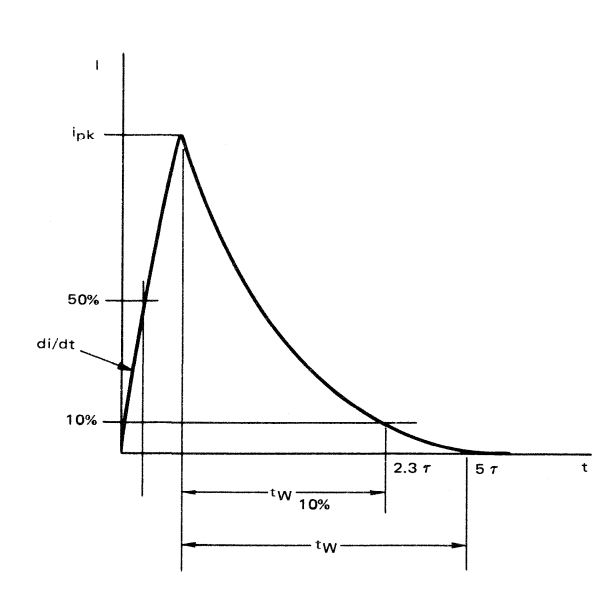
$$E = 1/2\,CV^2,$$

and the peak surge current

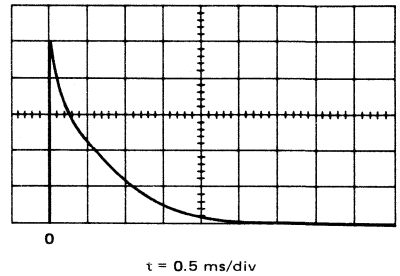
$$i_{pk} = \frac{V_C}{R_T}.$$

When the SCR crowbars the capacitor, the current waveform will be similar to that of Figure 3, with the peak surge current, i_{pk}, being a function of the total impedance in the circuit (Figure 4) and will thus be limited by the Equivalent Series Resistance (ESR) and

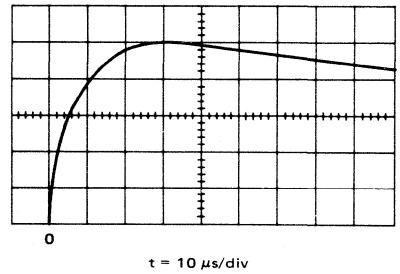
FIGURE 3 – Typical SCR Crowbar Waveform



CROWBAR CURRENT TERMS



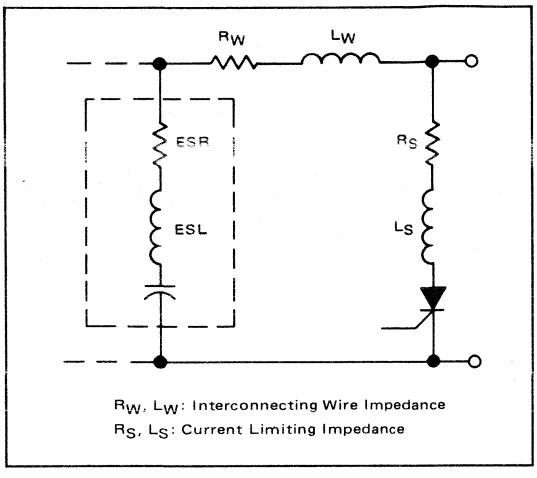
t = 0.5 ms/div



t = 10 μs/div

I = 200 A/div
MCR69
C = 22,000 μF
R_S = 0
V_C = 30 V
I_{GT} = 200 mA

FIGURE 4 – Circuit Elements Affecting SCR Surge Current



inductance (ESL) of the capacitor plus the dynamic impedance of the SCR, any external current limiting resistance, and the resistance (and inductance) of the interconnecting wires and circuit board conductors.

The ESR of computer grade capacitors, depending on the capacitor size and working voltage, might vary from 10 to 1000 milliohms (mΩ). Those used in this study were in the 25 to 50 mΩ range.

The dynamic impedance of the SCR (the slope of the on-state voltage, on-state current curve), at high currents, might be in the 10 to 20 mΩ range. As an example, from the on-state characteristics of the MCR70, 35 A rms SCR, the dynamic impedance is

$$r_d = \frac{\Delta V_F}{\Delta I_F} = \frac{(4.5 - 3.4)V}{(300 - 200)A} = \frac{1.1\ V}{100\ A} \cong 11\ m\Omega.$$

The interconnecting wire might offer an additional 5.0 mΩ (#20 solid copper wire ≅ 20 mΩ/ft) so that the total circuit resistance, without additional current limiting, might be in the 40 to 70 mΩ range. The circuit inductance was considered low enough to ignore as far as i_{pk} is concerned for this exercise, being in hundreds of nanohenry range (ESL ≅ 3 nH, L wire ≅ 500 nH/ft). However, di/dt will be affected by the inductance.

How Much Energy Can The Crowbar SCR Sustain?

There are several factors which contribute to possible SCR failures or degradation–the peak surge current, di/dt, and a measure of the device's energy capability, I^2t.

If the peak current and/or duration of the surge is large, destruction of the device due to excessive dissipation can occur. Obviously, the i_{pk} can be reduced by inserting additional impedance in the crowbar path, at an increase in dump time. However, this time, which is a measure of how long the overvoltatge is present, should be within the SOA of the load.

The energy stored in the capacitor being a constant for a particular capacitor voltage would suggest that the I^2 integral for any limiting resistance is also a constant. I reality, this is not the case as the thermal response of th device must be taken into consideration. It has bee shown[2] that the dissipation capability of a device varie as to the $\sqrt{t}$ for the first tens of milliseconds of th thermal response and, in effect, the measure of a device' energy capability would be closer to $i^2\sqrt{t}$. This effect i subsequently illustrated in the empirically derived i_p versus time derating curves being a non-linear function However, for comparison with fuses, which are rate in I^2t, the linear time base, "t", will be used.

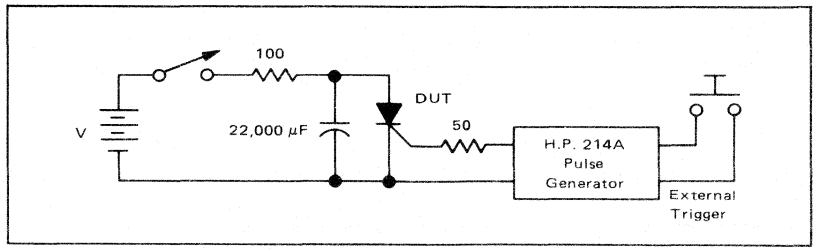
The di/dt of the current surge pulse is also a critica parameter and should not exceed the device's rating (typically about 200 A/μs for 50 A or less SCRs). Th magnitude of di/dt that the SCR can sustain is controlle by the device construction and, to some extent, the gat drive conditions. When the SCR gate region is driven on conduction across the junction starts in a small regio and progressively propagates across the total junction Anode current will initially be concentrated in this smal conducting area, causing high current densities which ca degrade and ultimately destroy the device. To minimiz this di/dt effect, the gate should be turned on hard an fast such that the area turned on is initially maximized This can be accomplished with a gate current puls approaching five times the maximum specified continuou gate current, I_{gt}, and with a fast rise time (< 1 μs). Th gate current pulse width should be greater than th propagation time; a figure of 10 μs minimum shoul satisfy most SCRs with average current ratings under 50 A or so.

The wiring inductance alone is generally large enoug to limit the di/dt. Since most SCRs are good for ove 100 A/μs, this effect is not too large a problem. How ever, if the di/dt is found excessive, it can be reduce by placing an inductance in the loop; but, again, thi increases the circuit's response time to an overvoltag and the trade-off should be considered.

Since many SCR applications are for 60 Hz line opera tion, the specified peak non-repetitive surge current I_{TSM} and circuit fusing I^2t are based on 1/2 cycle (8.3 ms conditions. For some SCRs, a derating curve based on u to 60 or 100 cycles of operation is also published. Thi rating, however, does not relate to crowbar applications To fully evaluate a crowbar system, the SCR must b characterized with the capacitor dump exponential surg current pulse.

A simple test circuit for deriving this pulse is shown i Figure 5, whereby a capacitor is charged through a limit ing resistor to the supply voltage, V, and then the charg is dumped by the SCR device under test (DUT). The SCI gate pulse can be varied in magnitude, pulse width, an rise time to produce the various I_{gt} conditions. An est mate of the crowbar energy capability of the DUT i determined by first dumping the capacitor charged to low voltage and then progressively increasing the voltag until the DUT fails. This is repeated for several devices t

FIGURE 5 – Simple Test Circuit for Crowbar SCR



stablish an average and minimum value of the failure oints cluster.

This procedure was used to test several different SCRs f which the following Table 1 describes several of the ertinent energy specifications and also the measured rowbar surge current at the point of device failure.

This one-shot destruct test was run with a gate current f five I_{GT}(max) and a 22,000 μF capacitor whose ESR roduced the exponentially decaying current pulse bout 1.5 ms wide at its 10% point. Based on an appro- riate derating, ten devices of each line were then success- ılly tested under the following conditions.

Device	V_C	i_{pk}	t
MCR68	12 V	250 A	1.5 ms
MCR69	30 V	800 A	1.5 ms
MCR70	30 V	800 A	1.5 ms

To determine the effect of gate drive on the SCRs, ıree devices from each line were characterized at non- estruct levels using three different capacitors (200, ,000, and 22,000 μF), three different capacitor voltages 10, 20, and 30 V), and three different gate drives GT(max), 5 I_{GT}(max), and a ramp I_{GT}(max) with di/dt of about 1.0 mA/μs). Due to its energy limitations, ıe MCR68 was tested with only 10 V across the larger ıpacitors.

The slow ramp, I_{GT}, was used to simulate overvoltage ınse applications where the gate trigger rise time can be ow such as with a coupling zener diode.

No difference in SCR current characteristics were ɔted with the different gate current drive conditions; the eak currents were a function of capacitor voltage and rcuit impedance, the fall times related to RTC, and the se times, t_r, and di/dt, were more circuit dependent (wiring inductance) and less device dependent (SCR turn- on time, t_{on}). Since the wiring inductance limits, t_r, the effect of various I_{GT}s was masked, resulting in virtually identical waveforms.

The derated surge current, derived from a single (or low number) pulse test, does not truly reflect what a power supply crowbar SCR might have to see over the life of the supply. Life testing over many cycles have to be performed; thus, the circuit described in Appendix B was developed. This life test fixture can simultaneously test ten SCRs under various crowbar energy and gate drive conditions.

Each of the illustrated SCRs of Figure 6a were tested with as many as four limiting resistors (0, 50, 100, and 240 mΩ) and run for 1000 cycles at a nominal energy level. If no failures occurred, the peak current was pro- gressively increased until a failure(s) resulted. Then the current was reduced by 10% and ten new devices were tested for 2000 cycles (about six hours at 350 cycles/ hour). If this test proved successful, the data was further derated by 20% and plotted as shown on log-log paper with a slope of −1/4. This theoretical slope, due to the $I^2\sqrt{t}$ one-dimensional heat-flow relationship (see Appen- dix D), closely follows the empirical results. Of parti- cular interest is that although the peak current increases with decreasing time, as expected, the I^2t actually decreases.

Figure 6b shows the effect of elevated ambient tem- perature on the peak current capability of the illustrated SCRs.

Fuse Characteristics

SCRs, like rectifiers, are generally rated in terms of average forward current, $I_T(AV)$, due to their half-wave operation. Additionally, an RMS forward current, $I_T(RMS)$, a peak forward surge current, I_{TSM}, and a

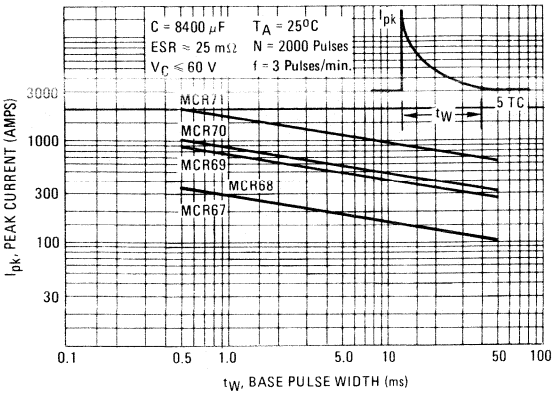
Table 1 – Specified and Measured Current Characteristics of Three SCRs

		Maximum Specified Values					Measured Crowbar Surge Current I_{pk}		
Device	Case	$I_{T(RMS)}$ (A)	$I_{T(AV)}$ (A)	I_{TSM}* (A)	i^2t (A^2sec)	I_{GT}(Max) (mA)	Min (A)	Max (A)	Ave (A)
MCR68	TO-220	12	8.0	100	40	30	380	750	480
MCR69	TO-220	25	16	300	375	30	1050	1250	1100
MCR70	TO-208	35	22	350	510	30	1100	1300	1200

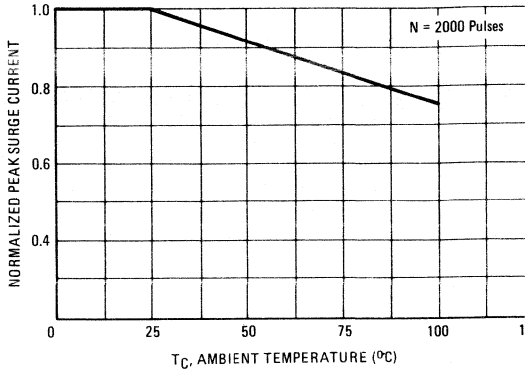
*I_{TSM} = Peak Non-Repetitive Surge Current, 1/2 cycle sine wave, 8.3 ms.
**Calculated from I_{TSM}.

FIGURE 6 — Crowbar Derating Curves

a. Peak Surge Current versus Pulse Width



b. Peak Surge Current versus Ambient Temperature



circuit-fusing energy limit, I^2t, may be shown. However, these specifications, which are based on one-half cycle 60 Hz operation, are not related to the crowbar current pulse and some means must be established to define their relationship. Also, fuses which must ultimately match the SCR and the load, are rated in RMS currents.

The crowbar energy curves are based on an exponentially decaying surge current waveform. This can be converted* to I_{RMS} by the equation

$$I_{RMS} = 0.316\ i_{pk}$$

which now allows relating the SCR to the fuse.

The logic load has its own overvoltage SOA as a function of time (Figure 1). The crowbar SCR must clamp the overvoltage within a specified time, and still be within its own energy rating; thus, the series-limiting resistance, R_S, in the crowbar path must satisfy both the load and SCR energy limitations. The overvoltage response time is set by the total limiting resistance and dumped capacitor(s) time constant. Since the SOA of the TTL used in this exercise was derived by a rectangular overvoltage pulse (in effect, over-energy), the energy equivalent of the real-world exponentially falling voltage waveform must be made. An approxmation can be made by using an equivalent rectangular pulse of 0.7 times the peak power and 0.7 times the base time.[2]

Once an overvoltage is detected and the crowbar is enabled, in addition to sustaining the peak current, the SCR must handle the regulator short-circuit current for the time it takes to open the fuse.

Thus, all three elements are tied together—the load can take just so much overvoltage (over-energy) and the crowbar SCR must repeatedly sustain for the life of the equipment an RMS equivalent current pulse that lasts for the fuse response time.

It would seem that the matching of the fuse to the SCR would be straightforward—simply ensure that the fuse RMS current rating never exceed the SCR RM current rating (Figure 7), but still be sufficient to hand steady-state and normal overload currents. The mo exact relationship would involve the energy dissipated the system $\int I^2R dt$, which on a comparative basis, can b reduced to I^2t. Thus, the "let-through" I^2t of the fu should not exceed the I^2t capability of the SCR under a operating conditions. These conditions are many, consis ing of "available fault current", power factor of the loa supply voltage, supply frequency, ambient temperatur and various fuse factors affecting the I^2t.

There has been much detailed information publishe on fuse characteristics and, rather than repeat the te which would take many pages, the reader is referred t those sources.[3,4] Instead, the fuse basics will be define and an example of matching the fuse to the SCR w be shown.

*See Appendix C for derivation.

FIGURE 7 — Time-Current Characteristic Curves of a Crowbar SCR and a Fuse

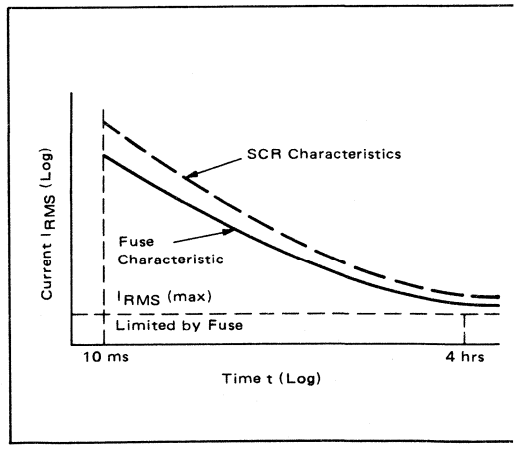
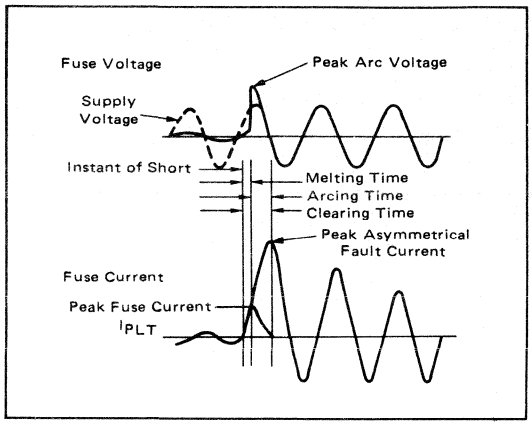


FIGURE 8 – Typical Fuse Timing Waveforms During Short Circuit



In addition to interrupting high current, the fuse should limit the current, thermal energy, and overvoltage due to the high current. Figure 8 illustrates the condition of the fuse at the moment the over-current starts. The peak let-through current can be assumed triangular in shape for a first-order approximation, lasting for the clearing time of the fuse. This time consists of the melting or pre-arcing time and the arcing time. The melting time is an inverse function of over-current and, at the time that the fuse element is opened, an arc will be formed causing the peak arc voltage. This arc voltage is both fuse and circuit dependent and under certain conditions can exceed the peak line voltage, a condition the user should ensure does not overstress the electronics.

The available short-circuit current is the maximum current the circuit is capable of delivering and is generally limited by the input transformer copper loss and reactance when the crowbar SCR is placed at the input to the regulator or the regulator current limiting when placed at the output. For a fuse to safely protect the circuit, it should limit the peak let-through current and clear the fault in a short time, usually less than 10 ms.

Fuse manufacturers publish several curves for characterizing their products. The current-time plot, which describes current versus melting time (minimum time being 10 ms), is used in general industrial applications, but is not adequate for protecting semiconductors where the clearing time must be in the subcycle range. Where protection is required for normal multicycle overloads, this curve is useful.

Two other useful curves, the total clearing I^2t characteristic and the peak let-through current I_{PLT} characteristic, are illustrated in Figures 9 and 10, respectively. Some vendors also show total clearing time curves (overlayed on Figure 9 as dotted lines) which then allows direct comparison with the SCR energy limits. When this clearing time information is not shown, then the designer should determine the I_{PLT} and I^2t from the respective curves and then solve for the clearing time from the approximate equation relating these two parameters. Assuming a triangular waveform[5] for I_{PLT}, the total clearing time, t_c, would then approximately be

$$t_c \approx \frac{3\,I^2t}{I_{PLT}{}^2}.$$

Once t_c of the fuse is known, the comparison with the SCR can readily be made. As long as the I^2t of the fuse is less than the I^2t of the SCR, the SCR is protected. It should be pointed out that these calculations are predicated on a known value of available fault current. By inspection of Figure 10, it can be seen that I_{PLT} can vary greatly with available fault current, which could have a marked effect on the degree of protection. Also, the illustrated curves are for particular operating condi-

FIGURE 9 – Maximum Clearing I^2t Characteristics for 10 to 20 A Fuses

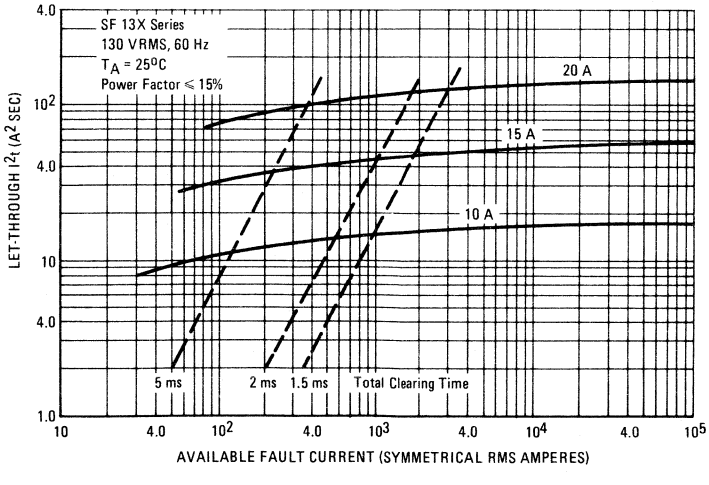
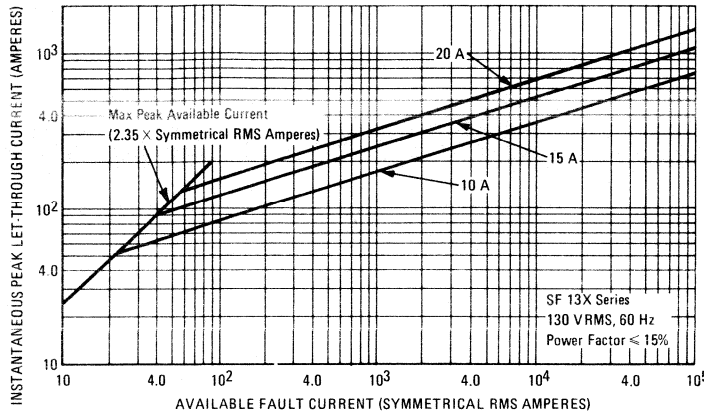


FIGURE 10 – Peak Let-Through Current versus Fault Current for 10 to 20 A Fuses



tions; the curves will vary somewhat with applied voltage and frequency, initial loading, load power factor, and ambient temperature. Therefore, the reader is referred to the manufacturer's data sheet in those cases where extrapolation will be required for other operating conditions. The final proof is obtained by testing the fuse in the actual circuit under worst-case conditions.

Crowbar Example

To illustrate the proper matching of the crowbar SCR to the load and the fuse, consider the following example. A 50 A TTL load, powered by a 60 A current limited series regulator, has to be protected from transients on the supply bus by crowbarring the regulator output. The output filter capacitor of 10,000 μF (200 μF/A) contributes most of the energy to be crowbarred (the input capacitor is current limited by the regulator). The transients can reach 18 V for periods of 100 ms.

Referring to Figure 1, it is seen that this transient exceeds the empirically derived SOA. To ensure safe operation, the overvoltage transient must be crowbarred within 5.0 ms. Since the TTL SOA is based on a rectangular power pulse even though plotted in terms of voltage, the equivalent crowbarred energy pulse should also be derived. Thus, the exponentially decaying voltage waveform should be multiplied by the exponentially decaying current to result in an energy waveform proportional to e^{-2x}. The rectangular equivalent will have to be determined and then compared with the TTL SOA. However, for simplicity, by using the crowbarred exponential waveform, a conservative rating will result.

To protect the SCR, a fuse must be chosen that will open before the SCR's I^2t is exceeded, the current being the regulator limiting current which will also be the available fault current to the fuse.

The fuse could be eliminated by using a 60 A SCR, but the cost versus convenience trade-off of not replacing the fuse is not warranted for this example. A second fuse or circuit breaker will protect the rectifiers and regulator for internal faults (shorts), but its selection, which based on the respective energy limits of those componen is not part of this exercise.

If a crowbar discharge time of 3.0 ms were chose it would not only be within the rectangular pulsed SO but also be well within the derived equivalent rectangul model of the exponential waveform. It would also requi about 1.3 time constants for the overvoltage to dec from 18 V to 5.0 V; thus, the RC time constant wou be 3.0 ms/1.3 or 2.3 ms.

The limiting resistance, R_S would simply be

$$R_S = \frac{2.3\ \text{ms}}{10{,}000\ \mu\text{F}} = 0.23\ \Omega \cong 0.2\ \Omega.$$

Since the capacitor quickly charges up to the overvolta V_{CC1} of 18 V, the peak capacitor discharge curre would be

$$I_{pk} = \frac{V_{CC1}}{R_S} = \frac{18\ \text{V}}{0.2\ \Omega} = 90\ \text{A}.$$

The RMS current equivalent for this exponentia decaying pulse would be

$$I_{RMS} = 0.316\ I_{pk} = 0.316(90) = 28.4\ \text{A RMS}.$$

Now referring to the SCR peak current energy curv (Figure 6), it is seen that the MCR68 can sustain 210 peak for a base time of 3.0 ms. This 12 A SCR must als sustain the 60 A regulator limited current for the tim required to open the fuse. The MCR68 has a specifie peak forward surge current rating of 100 A (1/2 cycl sine wave, 60 Hz, non-repetitive) and a circuit fusi rating of 40 A^2 s.

The non-repetitive rating implies that the device ca sustain 100 occurrences of this 1/2 cycle surge over th life of the device; the SCR crowbar surge current curv were based on 2000 cycles.

For the 3.0 ms time frame, the $I_1{}^2t_1$ for the expone

tial waveform is

$$I_1^2t_1 = (28.4\ A)^2(3.0\ ms) = 2.4\ A^2\ s$$

Assuming that the fuse will open within 6.0 ms, the approximate energy that the SCR must sustain would be 60 A for an additional 3.0 ms. By superposition, this would amount to

$$I_2^2t_2 = (60\ A)^2(6\ ms) = 21.6\ A^2\ s$$

which, when added to the exponential energy, would result in 24 A^2

The MCR68 has a 40 A^2 sec rating based on a 1/2 cycle of 8.3 ms. Due to the one-dimensional heat flow in the device, the energy capability is not linearly related to time, but varies as to the $\sqrt{t}$. Therefore, with a 6.0 ms 1/2-cycle sine wave, the 40 A^2t rating would now decrease to approximately (see Appendix D for derivation):

$$I_2^2t_2 = I_1^2t_1\left(\frac{t_2}{t_1}\right)^{1/2}$$

$$= 40\ A^2\ s\ \left(\frac{6.0\ ms}{8.3\ ms}\right)^{1/2}$$

$$= 34\ A^2\ s$$

Although the 1/2 cycle extrapolated rating is greater than the actual crowbar energy, it is only characterized for 100 cycles of operation.

To ensure 2000 cycles of operation, at a somewhat higher cost, the 25 A MCR69 could be chosen. Its exponential peak current capability, at 3.0 ms, is about 560 A and has a specified I_{TSM} of 300 A for 8.3 ms. The I^2t rating is not specified, but can be calculated from the equation

$$I^2t = \frac{(I_{TSM})^2}{2}\,t = \frac{(300\ A)^2}{2}(8.3\ ms) = 375\ A^2\ s$$

Extrapolating to 6.0 ms results in about 318 A^2 s, an I^2t rating much greater than the circuit 24 A^2 s value.

The circuit designer can then make the cost/performance trade-offs.

All of these ratings are predicated on the fuse opening within 6.0 ms.

With an available fault current of 60 A, Figure 9 shows that a 10 A (SF13X series) fuse will have a let-through I^2t of about 10 A^2 s and a total clearing time of about 6.0 ms, satisfying the SCR requirements, that is,

$$I^2t\ \text{fuse} < I^2t\ \text{SCR}$$

$$t_c \leqslant 6.0\ ms.$$

Figure 10 illustrates that for the same conditions, instantaneous peak let-through current of about 70 A would result. For fuse manufacturers that don't show the clearing time information, the approximate time can be calculated from the triangular model, as follows

$$t_c = \frac{3\ I^2t}{I_{PLT}^2} = \frac{3(10)}{(70)^2} = 6.1\ ms.$$

The fuse is now matched to the SCR which is matched to the logic load. Other types of loads can be similarly matched, if the load energy charactersitics are known.

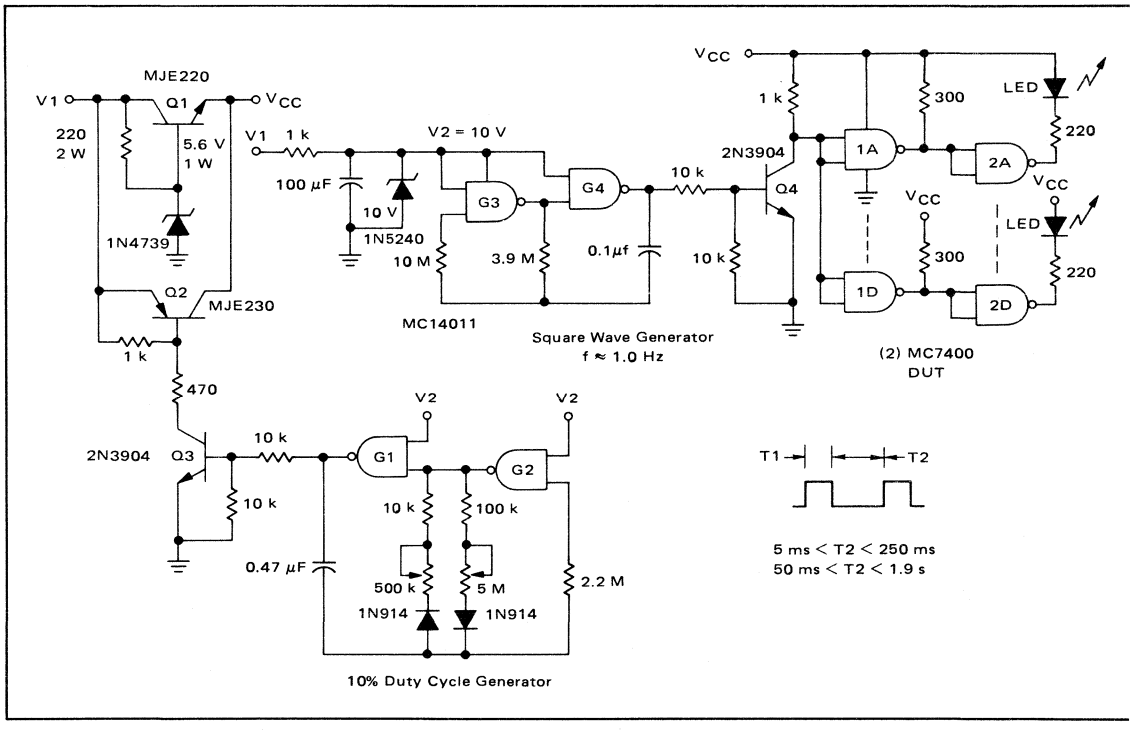
Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.

APPENDIX A

TTL SOA Test Circuit

Using the illustrated test circuit, the two TTL packages (quad, 2-input NAND gates) to be tested were powered by the simple, series regulator that is periodically shorted by the clamp transistor, Q2, at 10% duty cycle rate. By varying the input to the regulator V1 and the clamp pulse width, various power levels can be supplied to the TTL load. Thus, as an example, V_{CC} could be at 5 V for 90 ms and 10 V for 10 ms, simulating a transient on the bus or a possibly shorted power supply pass transistor for tha duration. These energy levels are progressively increase until the gate (or gates) fail, as detected by the statu of the output LEDs, the voltage and current waveform and the device case temperature. The results of thi quasi-SOA test are shown in Figure 1; the V_{CC}-puls width curve is a 20% derated one from a series of faile device cluster points.

TTL SOA Test Circuit



APPENDIX B

CR Crowbar Life Testing

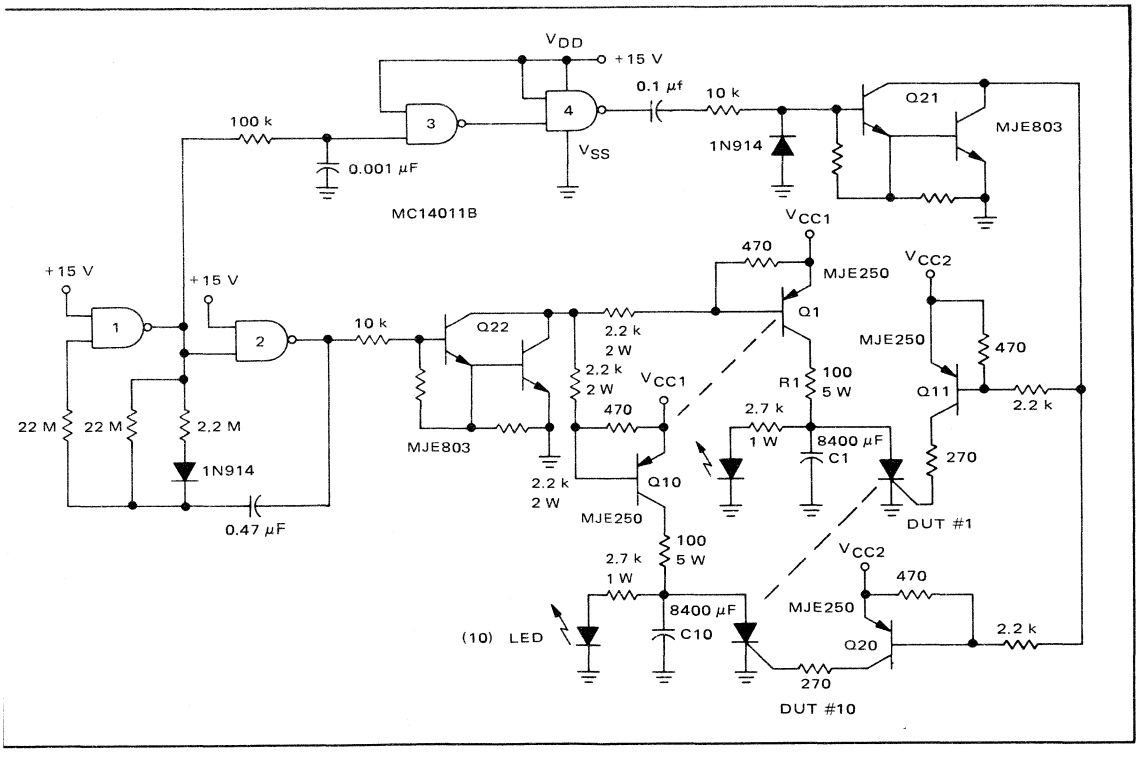
This crowbar life test fixture can simultaneously test en SCRs under various crowbar energy and gate drive onditions and works as follows.

The CMOS Astable M.V. (Gates 1 and 2) generate n asymmetric Gate 2 output of about ten seconds high, ne second low. This pulse is amplified by Darlington)22 to turn on the capacitor charging transistors Q1–Q10 or the ten seconds. The capacitors for crowbarring are hus charged in about four seconds to whatever power upply voltage to which V_{CC1} is set. The charging transis- ors are then turned off for one second and the SCRs are ired by an approximately 100 μs delayed trigger derived rom Gates 3 and 4. The R-C network on Gate 3 input ntegrates the complementary pulse from Gate 1, resulting n the delay, thus insuring non-coincident firing of the test ircuit. The shaped pulse out of Gate 4 is differentiated nd the positive-going pulse is amplified by Q21 and the ollowing ten SCR gate drivers (Q11–Q20) to form he approximate 2.0 ms wide, 1.0 μs rise time, SCR gate riggers, I_{GT}. I_{GT} is set by the collector resistors of the respective gate drivers and the supply voltage, V_{CC2}; thus, for $I_{GT} \approx 100$ mA, $V_{CC2} \approx 30$ V, etc.

The LEDs across the storage capacitors show the state of the voltage on the capacitors and help determine whether the circuit is functioning properly. The timing sequence would be an off LED for the one-second capacitor dump period followed by an increasingly brighter LED during the capacitor charge time. Monitoring the current of V_{CC1} will also indicate proper operation.

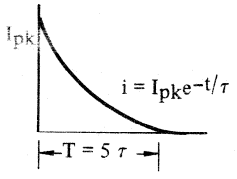
The fixture's maximum energy limits are set by the working voltage of the capacitors and breakdown voltage of the transistors. For this illustration, the 60 V, 8400 μF capacitors (ESR $\approx$ 20 mΩ) produced a peak current of about 2500 A lasting for about 0.5 ms when V_{CC1} equals 60 V. Other energy values (lower i_{pk}, greater t_w) can be obtained by placing a current limiting resistor between the positive side of the capacitor and the crowbar SCR anode, which is the method by which the curves of Figure 6 were derived.

Ten Position SCR Crowbar Life Test Fixture



APPENDIX C

Derivation of the RMS Current of an Exponentially Decaying Current Waveform



$$I_{RMS} = \sqrt{\frac{1}{T}\int_0^T i^2(t)\,dt}$$

$$= \left[\frac{1}{T}\int_0^T (I_{pk}e^{-t/\tau})^2\,dt\right]^{1/2}$$

$$= \left[\frac{I_{pk}^2}{T}\frac{e^{-2t/\tau}}{(-2/\tau)}\Bigg|_0^T\right]^{1/2}$$

$$= \left[\frac{I_{pk}^2}{T}\left(\frac{-\tau}{2}\right)(e^{-2T/\tau} - e^0)\right]^{1/2},$$

where $T = 5\ \tau$,

$$= \left[-\frac{I_{pk}^2}{10}(e^{-10} - 1)\right]^{1/2}$$

$$I_{RMS} = \frac{I_{pk}}{\sqrt{10}} = 0.316\ I_{pk}.$$

APPENDIX D

Derivation of I^2t for Various Times

Thermal Equation $\Delta t = Z(\theta)P_D$

where $Z(\theta) = r(t)R_{\theta JC}$

and $r(t) = K\sqrt{t}$.

Therefore, for the same Δt,

$$\Delta t = K\sqrt{t_1}\,R_{\theta JC}P_{D_1} = K\sqrt{t_2}\,R_{\theta JC}P_{D_2},$$

$$\frac{P_{D_1}}{P_{D_2}} = \sqrt{\frac{t_2}{t_1}} = \frac{I_1^2R}{I_2^2R},$$

$$\frac{I_1^2}{I_2^2} = \sqrt{\frac{t_2}{t_1}}.$$

Multiplying both sides by (t_1/t_2),

$$\frac{I_1^2t_1}{I_2^2t_2} = \left(\frac{t_2}{t_1}\right)^{1/2}\frac{t_1}{t_2} = \left(\frac{t_1}{t_2}\right)^{1/2},$$

$$I_1^2t_1 = I_2^2t_2\sqrt{\frac{t_1}{t_2}}.$$

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AN-803
Application Note

THE EFFECT OF EMITTER-BASE AVALANCHING ON HIGH-VOLTAGE POWER SWITICHING TRANSISTORS

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Senior Applications Engineer

Reverse biasing the base of a power transistor during turn-off decreases its turn-off switching losses. This application note investigates the effect of increasing the bias into avalanche on the life, switching speeds and inductive turn-off stresses on several types of high-voltage switching power transistors.

With the advent of a new generation of high-voltage, high-speed silicon power switching transistors, applications of greater than 20kHz operation are readily achievable. To obtain these bandwidths, certain circuit techniques have been developed to reduce the switching times and thus switching losses, the major dissipative effect in high frequency applications. Of the two switching times, turn-off time (t_{off}) is greater than turn-on time (t_{on}) and its reduction is of greater importance. The usual techniques described in the literature to minimize t_{off} are to reverse bias the emitter-base junction and allow a low impedance path for depleting or "sweeping out" the stored charge in the collector-base region. The result can be a great reduction in storage time (t_s) and also a substantial reduction in fall time (t_f). Minimizing storage time is of importance in pulse width modulation circuits such as switching regulators where regulation limits can require defined pulse width variations. Also, in switching applications requiring two or more transistors, (½ bridges, full bridges, push-pull inverters, etc.), low t_s (and many times matched t_s) is required to prevent transformer biasing. Since the turn-off switching losses are proportional to fall time, its need for reduction is apparent.

In addition to effecting turn-off times, reverse biasing the emitter-base also effects the RBSOA (Reverse Bias Safe Operating Area) capability of a transistor when switching clamped inductive loads. Depending on the process type and the current levels involved, this capability can increase with increasing off biases.

"Reverse bias" can be derived by applying a reverse voltage to the base through a low impedance source, resulting in a negative base current I_{B2} flowing, or through a reverse constant current source. Some transistor manufacturers specify turn-off switching times with a specified reverse voltage $V_{BE\ (off)}$, others with a reverse current I_{B2}. Either method can simulate the "real world" as some applications use a base-emitter clamp (to a negative supply for NPN transistors) to reduce turn-off times and others use a voltage source through a base-limiting resistor, as in transformer coupled circuits. $V_{BE(off)}$ is generally specified at $-5.0V$, however, for some devices, RBSOA can be derived with off biases up to the specified maximum emitter-base voltage rating of $-9.0V$. I_{B2} is usually selected at some multiple of I_{B1} (the forward base current), be it I_{B1} or two or four I_{B1}, etc. By increasing the off bias, even faster turn-off times can be obtained.

The question arises as to how much reverse bias can be applied to the device before adverse effects, if any, occur. Most power devices have maximum emitter-base voltage rating V_{EBO} of from 5 to 9V, implying that these ratings should not be exceeded. Some of the literature state that the emitter-base junction can be reversed biased into avalanche without degrading the device, but this premise is not supported with any documentation or test results.

Other literature states not to avalanche as this could possibly cause degradation of the device over a long period of time, particularly in a reduction of gain. Yet in some applications, notably TV horizontal deflection circuits, avalanching of the emitter-base is commonplace, although this is the result of generating a controlled storage time and not as a planned design.

It is the intent of this article to clarify this question by life testing a number of devices under emitter-base

avalanche conditions and determine if any detrimental effects occur.

Five different high-voltage "switchmode" devices were tested, three discretes and two darlingtons, encompassing two different but similar processes — triple diffused and epi-collector double diffused.

The parameters measured are h_{FE}, collector-emitter breakdown voltage $V_{CEO(sus)}$, emitter-base breakdown voltage (BV_{EBO}) and collector cutoff currents (I_{CEO} and I_{CBO}), and emitter cut-off current (I_{EBO}).

Additionally, turn-off times for resistive and inductive loads and RBSOA curves as a function of off-bias are shown, allowing circuit design optimization. And finally, seven base drive circuits which can avalanche the device under test (D.U.T.) are described with their cost/performance trade-offs.

LIFE TEST

All of the five product lines were life tested in the test circuit of Figure 1 using a resistive 10 ohm load. Additionally, an inductive load life test was performed using the 2N6250. The fixture consists of a CMOS oscillator (G_1 and G_2) clocking a CMOS decade counter whose outputs sequentially address the ten drivers and devices under test (D.U.T.). Thus, each D.U.T. is pulsed at a 10% duty cycle for approximately 30 μs, the period of the oscillator frequency (33kHz). Base currents I_{B1} were as listed in the following Table 1 to drive the 5A collector current and off bias was set large enough to ensure E-B avalanching. The resulting I_{B2} pulse was about 10μs wide at its base (as determined by the R_1C_1 differentiating circuit); thus the devices were avalanched for about a 3% duty cycle.

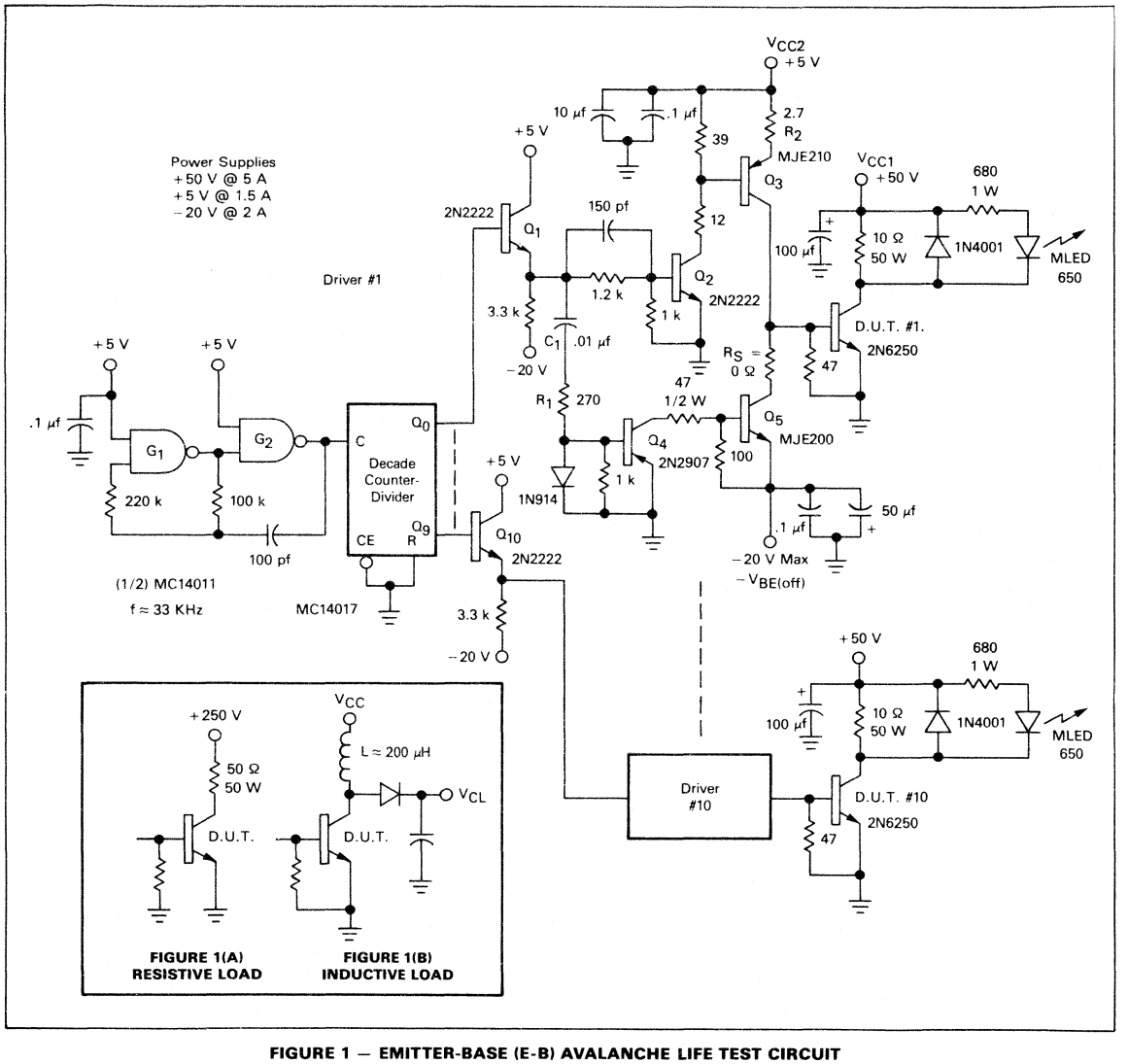


FIGURE 1 — EMITTER-BASE (E-B) AVALANCHE LIFE TEST CIRCUIT

Eight of the ten devices were emitter-base (E-B) avalanched with the listed reverse bias; the two remaining transistors were not biased and were used as a parameter standard. Additionally, another transistor was used as a measurement standard, never being powered, but always remeasured when the test devices were measured. This ensured measurement repeatability. For all tests, h_{FE} (and the other parameters) were remeasured after 1 day, 1 week, 3 weeks, 6 weeks, etc.

As expected, for the discrete devices, the greatest reduction in h_{FE} occurred at low collector currents with high-current h_{FE} having minimal change (Figures 2A, B&C). About 50% of this change occurred within the first 24-hour test period. In general, the two non-avalanched devices also had a proportional reduction in h_{FE} after life testing indicating a transistor "burn-in" period. Any reduction in h_{FE} beyond the life test periods of from 500 hours to 1160 hours respectively can be assumed to be due to "aging" since the non-avalanche devices also had reduced h_{FE}.

Measurement repeatability on the one standard, non-powered device was within 1 to 4% for the five product lines. After all these corrections were factored in, the approximate overall reduction of h_{FE} as a function of collector current is illustrated in Table 2. Note that the discrete devices have a relatively large reduction in h_{FE} at 10mA — about 15 to 25% — and a small change, if any, beyond 1A. The Darlingtons, on the other hand, showed a minimal change in h_{FE} (Figures 2D & E) with the two respective non-avalanche units showing similar reductions in h_{FE}. Thus, any change in the illustrated h_{FE} is the result of the differences between the avalanched and non-avalanched devices and will only be as accurate as the respective measurements. With the limited sample size (two) of the non-avalanched units, there can be some question as to the accuracy of the "modified" h_{FE}. However, based on the life testing of these five high-voltage double and triple diffused power transistors where burn-in and aging effects were noted, it could be concluded that no appreciable change in medium- and high-current h_{FE} will occur when the devices are emitter-base avalanched.

The other parameters measured proved even more consistent. Collector emitter breakdown voltages, $V_{CEO(sus)}$, were measured prior to testing and remained within about ± 5V after testing, any change being attributed to measurement accuracy. Similarly, the emitter-base breakdown voltage (BV_{EBO}) showed no degradation being within ± 0.1V of the initial reading. No drastic changes in cut-off currents, I_{CBO} and I_{EBO}, were noted, varying at the most by ± 20% from the typical value of about 1μA.

E-B AVALANCHE LIFE TEST CONDITIONS

TABLE 1

D.U.T.	TYPE	Spec I_C (A)	Spec V_{EB} (V)	Spec $V_{CEO(sus)}$ (V)	$V_{BE(off)}$ (V)	I_{B1} (A)	$I_{B2(pk)}$ (A)	Hours
2N6250	NPN	15	6	275	−20	1	7	1130
2N6545	H.V.	8	9	400	−15	1	6	530
2N6547	Discrete	15	9	400	−12	1	6	1570
MJ10011	Darlington Horiz. Defl.	8	5	700	−12	0.25	5	1160
MJ10001	Darlington H.V.	8	8	400	−14	0.25	4	500

% REDUCTION IN h_{FE} DUE TO E-B AVALANCHING

TABLE 2

I_C / D.U.T.	10 mA	100 mA	500 mA	1 A	3 A	4 A	5 A	8 A	10 A	15 A
2N6250	−25	−5	—	−1	0	—	0	—	0	—
2N6545	−20	−20	—	−5	0	—	0	0	—	—
2N6547	−15	−10	—	−3	0	—	0	—	0	0
MJ10011	—	0	0	0	—	0	—	0	—	—
MJ10001	—	0	—	0	0	—	0	0	—	—

FIGURE 2(A) —
CHANGE OF h_{FE} DUE TO E-B AVALANCHING.
AVERAGE OF 8 DEVICES TESTED FOR 1130 HRS.

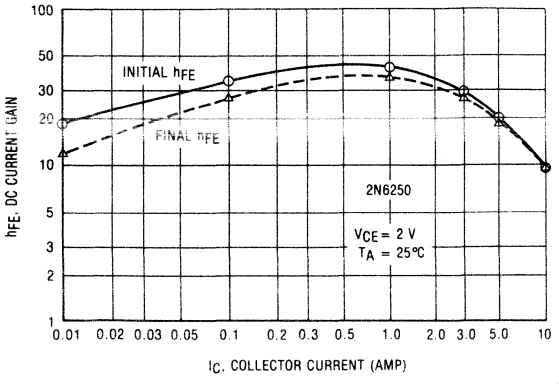


FIGURE 2(B) —
CHANGE OF h_{FE} DUE TO E-B AVALANCHING.
AVERAGE OF 8 DEVICES TESTED FOR 530 HRS.

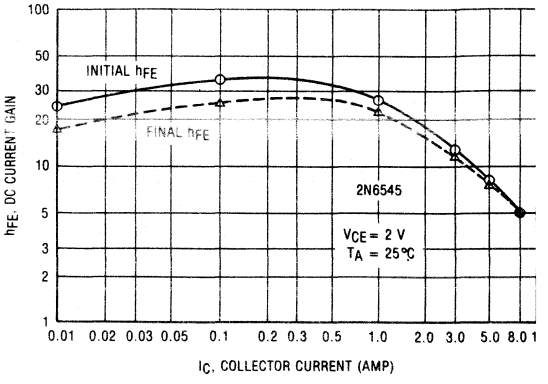


FIGURE 2(C) —
CHANGE OF h_{FE} DUE TO E-B AVALANCHING.
AVERAGE OF 8 DEVICES TESTED FOR 1570 HRS.

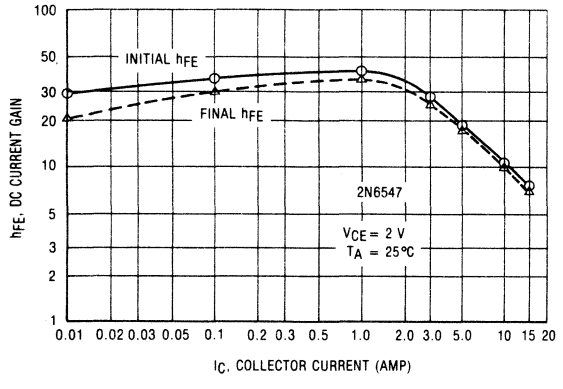


FIGURE 2(D) —
CHANGE OF h_{FE} DUE TO E-B AVALANCHING.
AVERAGE OF 8 DEVICES TESTED FOR 1160 HRS.

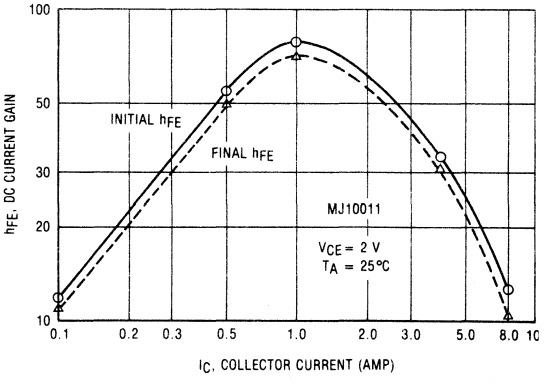
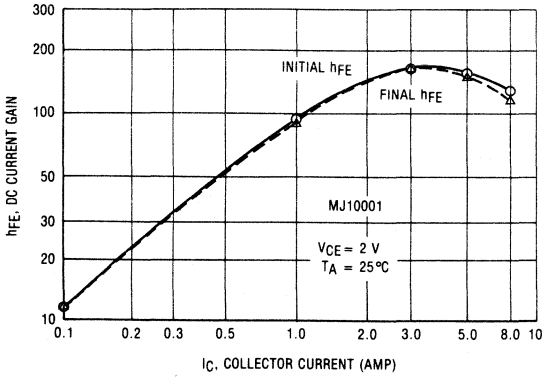


FIGURE 2(E) —
CHANGE OF h_{FE} DUE TO E-B AVALANCHING.
AVERAGE OF 8 DEVICES TESTED FOR 500 HRS.



RBSOA TEST

In addition to performing life tests with a resistive load, a 330 hour clamped inductive load life test was performed on 10 samples of the 2N6250 to determine if avalanching had any effect on this type of load. The test circuit was similar to the resistive load life test circuit (Figure 1) with the load now being a 100μH inductor collector current was ramped up to 5A pk) clamped by a fast recovery rectifier to a 250V supply. Five pairs of drivers were driven by a 5-stage counter resulting in a 10% duty cycle operation. As in the previous test, two of the D.U.T.'s (standard) had zero volts off-bias and of the remaining eight devices, three had $V_{BE(off)}$ of −5.0V and five were run well into avalanche with $V_{BE(off)}$ of −20V. RBSOA characterization was performed before and after the life test to see what effect off-bias had on the turn-off energy capability. This test was performed with off-biases of −5V, −15V and −20V. Additionally, three non-life test devices were similarly characterized for RBSOA and two devices were not tested at all but simply used as an h_{FE} measurement/aging standard. Using the same normalized h_{FE} correction as previously, it was found that h_{FE} degraded similar to the resistive load case, i.e., greater low current h_{FE} degradation which was proportional to off-bias, as follows:

I_C / $V_{BE(off)}$	Δ h_{FE}		
	100mA	5A	10A
0 V	0	0	0
−5 V	−3%	0	0
−20 V	−20%	0	0

There also was no change in collector leakage current I_{ES} and collector-emitter sustaining voltage $V_{CEO(sus)}$ within measurement repeatability limits but the change in collector-emitter breakdown voltage (at 100μA) showed some increase after life test. For this small sample size, BV_{CEO} increased after life testing by about 4V, 10V and 50V at $V_{BE(off)}$ of 0V, −5V and −20V respectively.

RBSOA after life testing showed little change; if anything, it increased slightly for the $V_{BE(off)}$ conditions of −15V and −20V.

It should be pointed out that the typical RBSOA capability of the 2N6250 was measured at only one collector current (5A) with the aforementioned off-bias voltages. A detailed RBSOA curve or family of curves would be performed at various collector currents with various off-biases to fully characterize the device. These type of curves are illustrated in Figures 3(A) and (B) for the "Switchmode" transistor 2N6545, Figure 3(A) showing the $V_{BE(off)}$ being the variable and 3(B), I_{B2} the variable. Note that at high collector-emitter voltages, the RBSOA capability increases with off-biases and at high collector currents, it decreases. This is due to switching speed/loss predominating over current crowding (hot spot) effects at high voltage whereas at high current, the opposite results. For this device, using $V_{BE(off)}$ as the variable, the large increase in RBSOA capability at high voltage, nominal currents is readily observable. Both figures were derived with one D.U.T. using a 200μH inductor in a non-destruct RBSOA fixture, a circuit that detects the advent of second breakdown and quickly turns off the power to the D.U.T.

FIGURE 3(A) – TYPICAL CLAMPED INDUCTIVE LOAD REVERSE BIAS SAFE OPERATING AREA (RBSOA) AS A FUNCTION OF REVERSE BIAS VOLTAGE ($V_{BE(off)}$) FOR THE 2N6545

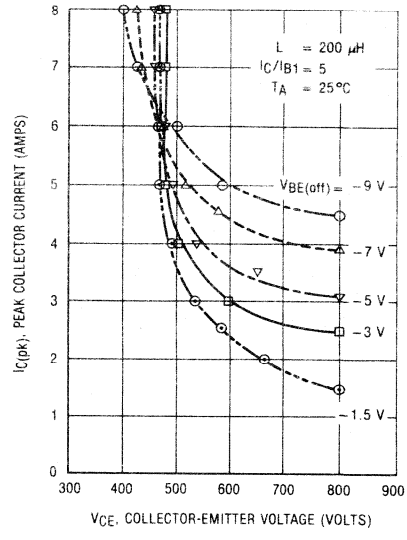
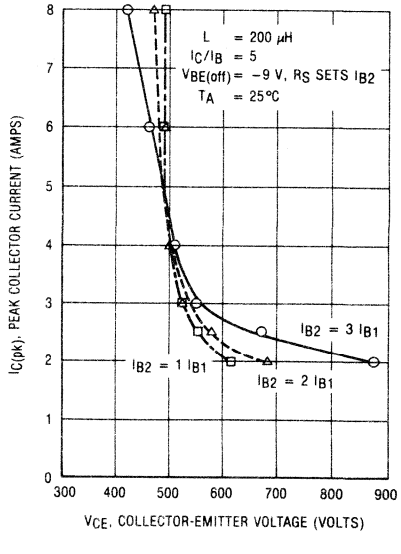


FIGURE 3(B) – TYPICAL CLAMPED INDUCTIVE LOAD REVERSE BIAS SAFE OPERATING AREA (RBSOA) AS A FUNCTION OF REVERSE BASE CURRENT (I_{B2}) FOR THE 2N6545



TURN-OFF TEST, TRANSISTOR CLAMP SERIES SWITCH

Thus far, the effect of $V_{BE(off)}$ including avalanching has been illustrated through life testing and RBSOA characterizing. The initial purpose of this excercise was to show the effect of off-bias on turn-off switching times. This switching evaluation was performed in detail with a circuit identical to one stage of the ten stage life test circuit (Figure 1). Instead of using an input drive pulse derived from the decade counter and emitter follower Q1, a pulse generator was used at the Q1 output node; its specs are: pulse amplitude of 5V, width of about 25μs, duty cycle of about 2% and switching times of about 10ns max. Turn-off switching tests were performed with a resistive load and a clamped inductive load using three 2N6250's as the D.U.T.'s. (These same three devices were also used in subsequently described test circuits). For most of the tests, the collector current was set for 5A and I_{B1} for 1A; the resistive load used a 50Ω, 50W resistor with V_{CC1} of 250V and the inductive load used a 200μH inductor ramping up to 5A pk while clamped to a 250V supply.

This circuit is described as a "transistor clamp series switch" since it uses transistor Q_5 (as a D.U.T. base clamp) to provide the low impedance path for sweeping out the stored charge and a series transistor switch Q_4 to drive Q_5. The negative supply to the clamp emitter (Q_5) furnishes the reverse bias voltage $V_{BE(off)}$ and/or reverse current I_{B2}. This current is dictated by the stored charge in the D.U.T., its base spreading resistance, the series resistance and h_{FE} of Q_5.

Upon application of a positive pulse (25μs wide in this case to simulate 20kHz operation), NPN transistor switch Q_2 is turned on, supplying base drive for the PNP constant current switch Q_3. Transistor Q_3 is operated in this mode to prevent device saturation and thus reduce its own storage time. The emitter resistor R_2 sets the emitter current, and hence, the forward base current for the D.U.T., to about 1.0A. As the applied pulse switches to ground, the R_1, C_1 network produces a negative going, differentiated pulse derived from the trailing edge of the positive pulse. This pulse, about 10μs at its base, supplies base current for PNP transistor Q_4, turning it on. Thus, Q_4 is on for only the 10μs following the turn on pulse and its peak power handling capability can be relatively high. Base current (as much as 400mA when $V_{BE(off)}$ equals 20V) is then provided to Q_5, initiating the I_{B2} current pulse. The base current and voltage waveforms are illustrated in Figure 4 for four conditions of reverse bias, $V_{BE(off)}$ equals 0V, −5V, approximately −15V (avalanche) and −20V. Note that when the bias exceeds avalanche, the I_{B2} waveform becomes somewhat rectangular, the energy (area under the curve) increases and thus the total device dissipation, and junction temperature, increases. As an example, when operating at a 10% duty cycle (as was the case for the life test fixture), with a $V_{BE(off)}$ of −20V and an I_{B2} of 7A, the emitter base dissipation would be approximately:

$$P_{D(E\text{-}B)} = V_{BE(off)}\ I_{B2}\ D.C.$$
$$= 20\ (7)\ (10\mu s/300\mu s)$$
$$= 4.7W$$

Using the published thermal resistance of 1.0°C/W, the rise in junction temperature due to this increase dissipation would be:

$$\Delta t = t_j - t_c = R_{\theta JC}\ P_D = 1.0°C/W\ (4.7W)$$
$$= 4.7°C$$

This calculated temperature rise of about 5°C agree with the measured temperature of about 6°C for the av alanched devices.

A limited life test of 200 hours was also performe using an inductive load where the I_{B2} duty cycle wa increased to about 20%. The results, as expected, wa an increase in case temperature and the decrease in low current h_{FE} was of the same magnitude as prior examples Thus, when operating at higher E-B duty cycles, th increased dissipation due to emitter-base avalanchin should be considered in regard to total device dissipation

The effect of reverse bias and I_{B2} current limitin resistance on switching times t_s and t_f is illustrated i Figures 5(a) through (e), 6, 7(a) & (b) and 8(a) & (b) Figure 5 defines the turn-off switching times of th 2N6250 with a resistive load and collector current of 5A Figure 6 shows t_f versus I_B with I_C equal to 2.5A an Figure 7 shows the inductive load conditions. The re sistive load switching times for another transistor type the 2N6547, is illustrated in Figure 8. For all resistiv curves, the current limiting resistor R_S is varied from to 8.2 ohms. Figure 5(a) depicts the reduction of storag time t_s as a function of reverse bias and clamp circu resistance, Figure 5(b) shows the relationship of revers bias voltage and the resulting reverse base current I_B and Figure 5(c) the change of t_s versus I_{B2}. Note that th I_{B2} − t_s curve is derived from the conditions of Figur 5(a) and is completely independent of R_s as I_{B2} dictate the storage time for this circuit. As could be expected the lowest storage time occurs for maximum I_{B2}, whic in this case is limited by h_{FE} of the clamp transistor Q_5 maximum $V_{BE(off)}$ and minimum clamp circuit imped ance. It is also of interest that there is relatively littl decrease in t_s beyond about −9V of back bias (Figur 5(a)), 0.9μs compared to 0.7μs at −15V when R_S equal zero. As a relative measurement, t_s was about 16.5μ and 1.7μs with biases of 0V and −5V respectively.

Fall-time t_f curves as a function of $V_{BE(off)}$ and I_{B2} ar shown in Figures 5(d) and 5(e) respectively. Of particul interest is that fall-time does initially decrease with ir creasing bias voltage $V_{BE(off)}$ but actually starts to ir crease (under low clamp resistance conditions) beyon a particular bias. When R_S equals zero ohms, the valle point was about −9V (relative to where the device av alanched at about −14V). This phenomena is more pro nounced when viewing t_s versus I_{B2} (Figure 5(e)); th valley point occurs at about I_{B2} equals −5A peak.

The collector current was 5A for this test.

When the collector current was reduced to 2.5A (Fig ure 6), the valley point was around an I_{B2} of about 3A And thirdly, this condition is also observable in Figur 7(b), the inductive fall-time test and Figure 8(a), th 2N6547 resistive test.

This increase in collector current fall-time at the poir where the reverse base current is approximately equa to the peak collector current is attributed to the emitte having no further influence on the collector curren When I_{B2} equals I_C, I_E is zero, transistor action ceas and t_f is now governed by the reverse recovery proce of the collector-base junction.

Also of interest is that the fall-time is minimized when ıiven by a more ideal current source as shown by the ırves of Figures 5(e), 6 & 8(a). Note that for the same $_2$, t_f is less for increasing series resistance R_S. Obously, $V_{BE(off)}$ must be increased accordingly to maiin this current.

Storage time is related to a carrier recombination pro:ss and is a measure of the minority carrier lifetime in e base and collector regions[3]; thus, it should be in:pendent of the type of load (inductive or resistive) for e same bias conditions (I_{B1}, I_{B2}, I_C). This is illustrated the t_s versus I_{B2} curves of the resistive and inductive ads (Figures 5(c) and 7(a)) being approximately equal.

Collector current fall-time for the inductive load proved to be somewhat faster than for the resistive load (Figures 5(e) & 7(b)) for comparable operating conditions (V_{CC} = 250V, R_L = 50Ω, I_C = 5A for the resistive load relative to V_{CL} = 250V, $I_{C(pk)}$ = 5A for the inductive load). This is due to the difference in the transistor effective base widths for the two circuits. For the resistive load line case, the average collector-emitter voltage ($V_{CE(ave)} \approx V_{CC/2}$ for CI A) is lower than the inductive load line which swings out to V_{Clamp} and thus the depletion layer is narrower, the base width is wider resulting in slower t_{fi}.

2N6250

CONDITIONS: I_{B1} = 1.0 A, I_C = 5.0 A, V_{CC} = 250 V, R_L = 50 Ω, R_S = 0 Ω

(CIRCUIT OF FIG. 1A)

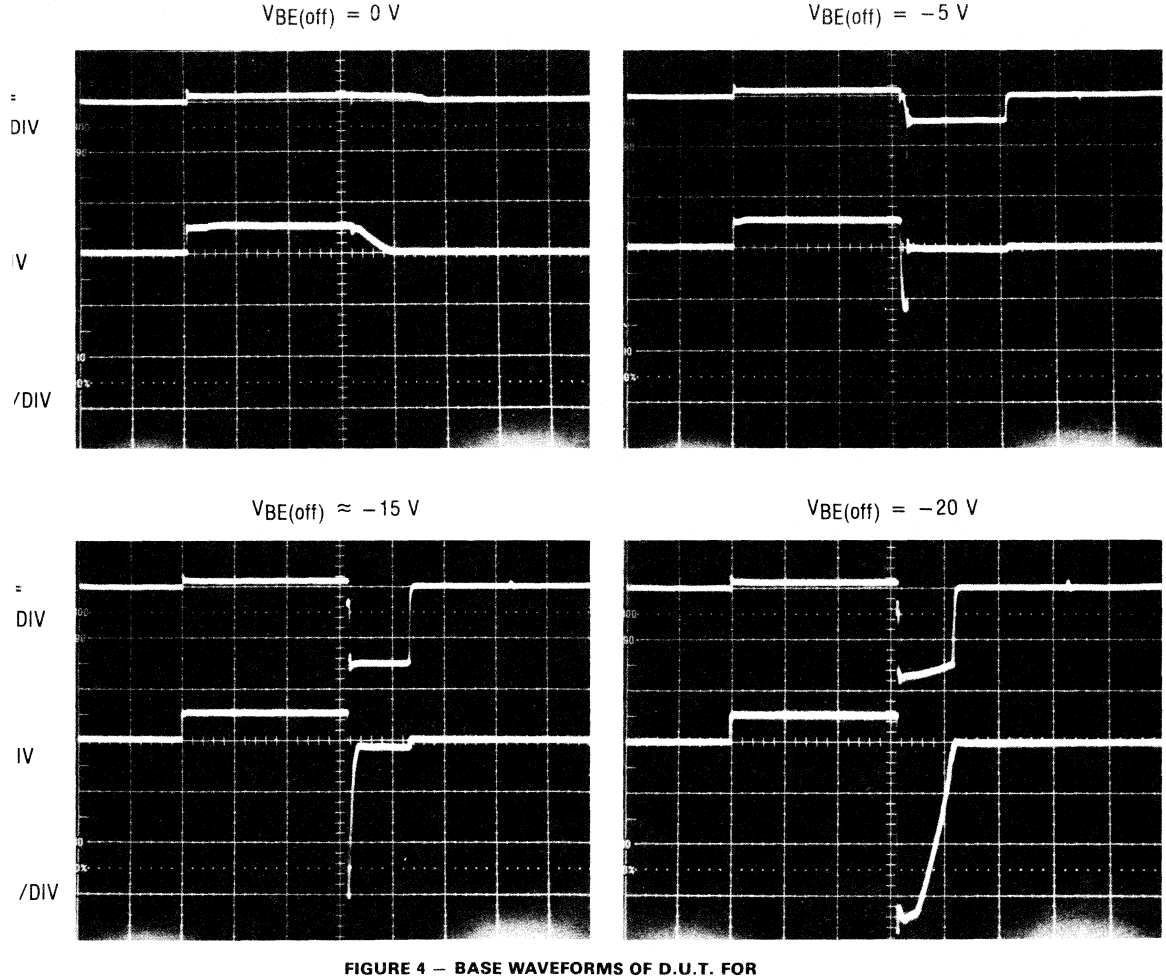


FIGURE 4 — BASE WAVEFORMS OF D.U.T. FOR VARIOUS REVERSE BIASES

FIGURE 5(A) — STORAGE TIME OF THE 2N6250 WITH VARIABLE REVERSE BIAS VOLTAGE. RESISTIVE LOAD

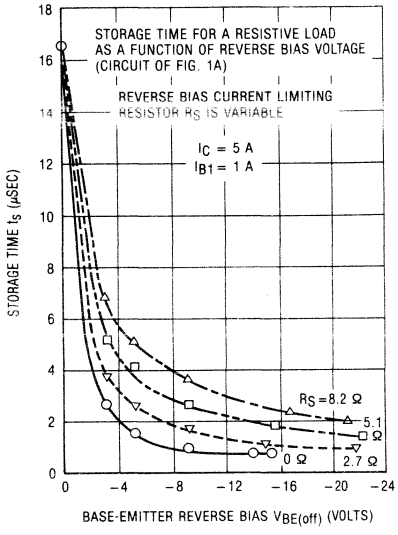


FIGURE 5(B) — BASE INPUT CHARACTERISTICS FOR THE 2N6250

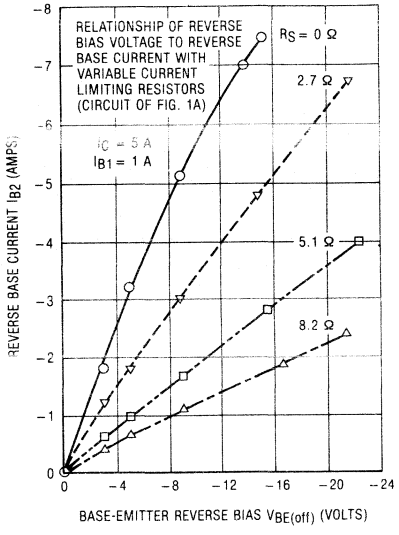


FIGURE 5(C) — STORAGE TIME OF THE 2N6250 WITH VARIABLE REVERSE BASE CURRENT. RESISTIVE LOAD

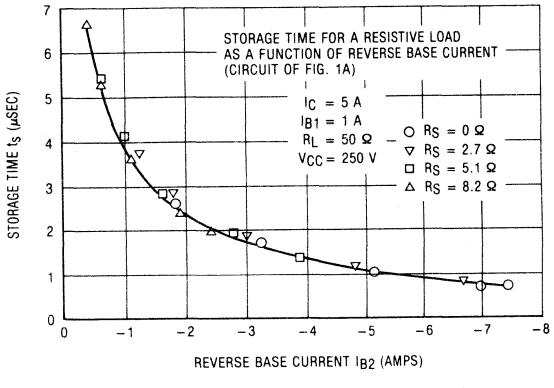


FIGURE 5(D) — FALL TIME OF THE 2N6250 WITH VARIABLE REVERSE BIAS VOLTAGE. RESISTIVE LOAD

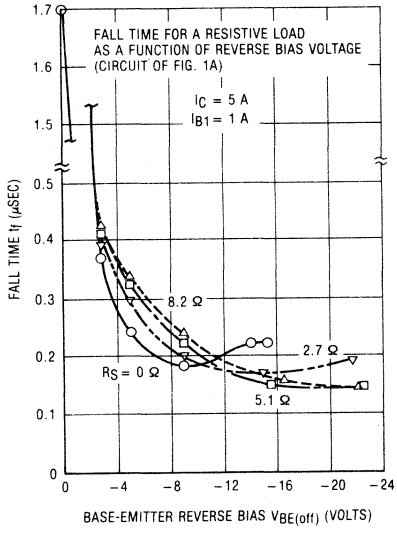


FIGURE 5(E) — FALL TIME OF THE 2N6250 WITH VARIABLE REVERSE BASE CURRENT. RESISTIVE LOAD

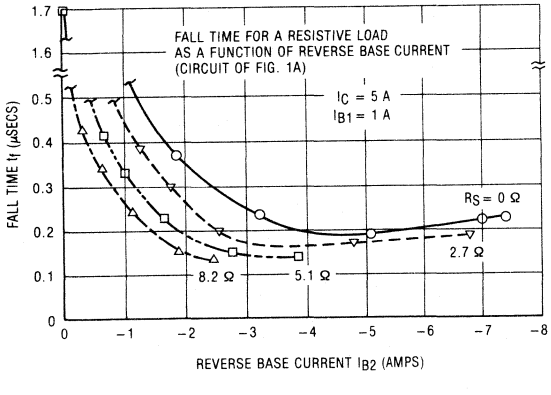


FIGURE 6 — FALL TIME OF THE 2N6250 WITH VARIABLE REVERSE BASE CURRENT AND LOWER COLLECTOR CURRENT

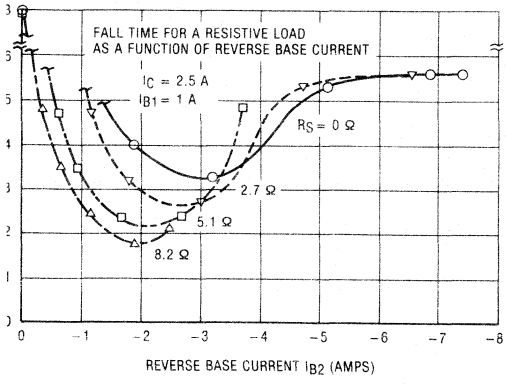


FIGURE 7(B) — FALL TIME OF THE 2N6250 WITH VARIABLE REVERSE BASE CURRENT. INDUCTIVE LOAD

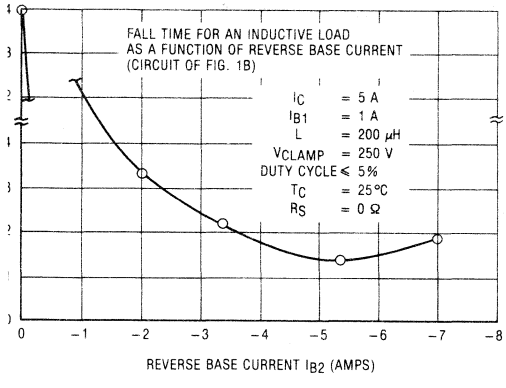
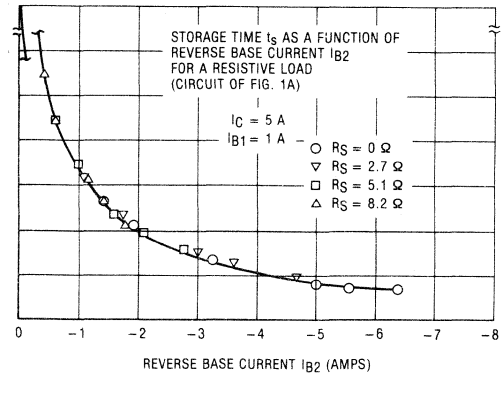


FIGURE 8(B) — 2N6547 STORAGE TIMES



NCLUSIONS

fter the completion of the characterization of switch-
e transistors with off biases, including E-B ava-
ning, the following conclusions can be noted.

Storage time can be greatly reduced with increasing off bias.

FIGURE 7(A) — STORAGE TIME OF THE 2N6250 WITH VARIABLE REVERSE BASE CURRENT. INDUCTIVE LOAD

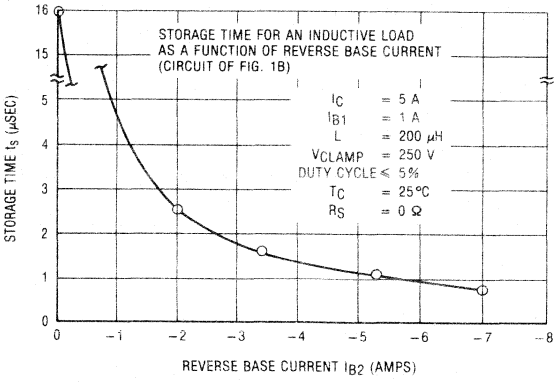
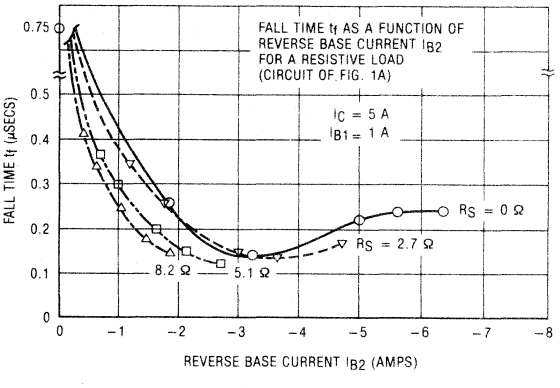


FIGURE 8(A) — 2N6547 FALL TIMES



2. Collector current fall-time decreases with increasing off-bias until transistor action ceases ($I_{B2} \approx I_C$) and increases thereafter.
3. Base circuit impedance effects turn-off time; for the same off bias voltage, t_s increases with increasing R_s (I_{B2} decreases) and t_f can be minimized with a constant current drive for the same I_{B2} (higher R_S & $V_{BE(off)}$).
4. E-B avalanching causes a reduction in low-current h_{FE} and that the degree of h_{FE} degradation is proportional to the amount of off bias;
5. E-B power dissipation during avalanching should be considered in the total power capability of the device;
6. E-B avalanching does not change the RBSOA capability;
7. RBSOA capability increases at the high voltage, nominal current portion of the curve with increasing bias.

Knowing these effects of reverse biasing, the designer can now optimize his base drive circuit to minimize t_f, if that is his requirement, or decrease t_s or increase RBSOA. If the drive circuit avalanches the emitter-base junction, the long-term results are now known (low current h_{FE} degradation) and adequate design precautions taken.

EMITTER-BASE AVALANCHE TEST CIRCUITS

The extreme case in reverse biasing the emitter-base is to avalanche the power transistor. A number of circuits capable of performing this function, if so required, have been investigated with the following illustrated seven (including the one previously described) offering the best performance — cost trade-offs.

Some of the circuits have been shown in one form or another elsewhere, others are variation on a theme — biases scaled up to insure avalanching, timing generation simplified, etc. Most of the circuits use a single power supply for the low-level drive circuits, relying on capacitive or inductive storage techniques for generating the reverse bias for emitter-base avalanching. In two variations, due to practical limitations on component size, cost and timing considerations, E-B avalanching is not achieved. The most practical and effective circuit requires an additional negative power supply, which may not always be readily available in the system.

To standardize the results of the seven circuits, all circuits had the same collector load current of 5.0A (R_L = 50Ω, V_{CC} = 250V) and the same base drive current I_{B1} of 1.0A. Additionally, the same three devices under tests (D.U.T.) were used in all circuits with the resultant turn-off times being the average of the three D.U.T.'s. All circuits were designed for low duty cycle operation, typically 2%. To operate at higher duty cycles, the component power ratings would have to be scaled up accordingly.

The following circuits, not necessarily in order of the best or most economical performance, illustrate some E-B avalanching techniques.

TRANSISTOR CLAMP, SHUNT SWITCH

This circuit, as illustrated in Figure 9, is similar to tl previously described one in that it also uses a clan transistor Q_4 across the D.U.T. for E-B avalanchin However, in this example, the clamp transistor is co trolled by its own clamp, transistor Q_3 operating as shunt switch. Avalanche timing is set by the R_1, network acting in conjunction with Q_3 as a half mon stable multivibrator. Normally, when the positive goi input pulse is not present, Q_3 is conducting, cutting-c Q_4 and no back bias is applied to the D.U.T. Under t conditions of $V_{BE(off)}$ of −20V with R_2 equal to 390 the collector current for Q_3 would be approximate 50mA; (for low-duty cycle operation, R_2 would dissip about 1W).

When a positive pulse is applied to the circuit, NF transistor Q_1 is turned on and supplies base current the Baker clamped (diodes D_1 and D_2) PNP switch Q turning it on. Transistor Q_2, being non-saturated and th not contributing appreciable storage time to the circu supplies base current of 1.0A (as set by R_3) to the D.U.

At the trailing edge of the applied positive pulse, tra sistor Q_3 will turn-off and remain off while capacitor charges through R_1. The current flowing through R_2 now diverted as base current for Q_4, turning it on. F the conditions shown with $V_{BE(off)}$ of −20V, an a proximate 3μs avalanche pulse is formed causing a rap transistion from I_{B1} to I_{B2} (less than 50ns from I_{B1} 1.0A to I_{B2} = −1.0A).

Since there is a limited base current drive for Q_4 only 50mA due to the power rating of R_2, only abo 3.3A of I_{B2} resulted (relative to about 7.4A for the p vious circuit). This produced in the D.U.T. turn-off tin of 1.5μs and 0.13μs respectively for t_s and t_f.

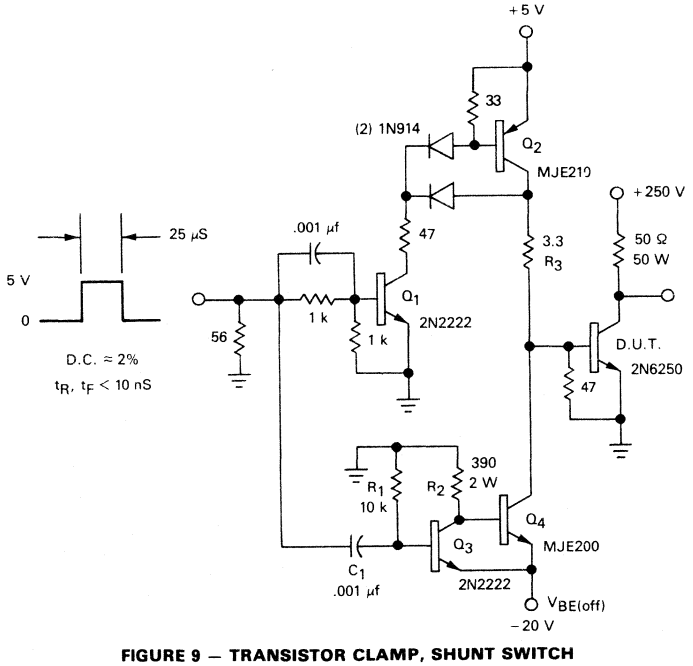


FIGURE 9 — TRANSISTOR CLAMP, SHUNT SWITCH E-B AVALANCHE CIRCUIT

'OTEM POLE DRIVE (TTL)

When only a single power supply is available, then ıe totem-pole circuit of Figures 10(a) and (b) can be sed to generate the reverse bias voltage. For this TTL onfigured driver, two approaches were used to produce ıe $V_{BE(off)}$, an RC network in the base of the D.U.T. Figure 10(a)) and a zener in the emitter of the D.U.T. Figure 10(b)). Activation is started by applying a posi- ive pulse to the base of transistor Q_1 turning it on and lamping Q_2 off. Base current is then supplied through $_1$ to transistor Q_3 (acting as an emitter-follower), turn- ng it on. This stage supplies the 1.0A base current, as et by resistors R_2 and R_3, to the D.U.T.. When the nitiate pulse is removed, transistor Q_1 turn off, Q_2 turns n which activates the clamp transistor Q_4. Concurrent vith this action Q_3 is turned off by the clamping of Q_2, emoving base drive to the D.U.T.. For the circuit of igure 10(a), the capacitor C_1 is initially charged to the oltage drop across R_3 — approximately 15V — and vhen Q_4 is energized, the clamping of the positive side f the capacitor to ground will cause a reverse bias to he D.U.T.. The amount of bias is dependent on the harge on C_1. As an example, when C_1 is 1.0μf, a bias f about −14V resulted. The time for this capacitor to ecover, however, was about 100μs, which would be too ong for 20kHz operation. A more practical recovery ime of 30μs was achieved when C_1 was 0.33μf. This, owever, resulted in lower $V_{BE(off)}$ (about −8V), and longer turn-off times (1.4μs relative to 1.1μs). The other extreme is when C_1 was zero — the resulting t_s was about 16μs.

Similar results were obtained when a 15V zener was used as a coupling element in place of R_3.

The second approach of using a 15V zener in the emitter of the D.U.T. to produce the back bias also resulted in comparable turn-off times, with t_f being slightly faster — about 0.2μs relative to 0.3μs for the first example. This zener, however, must be large enough to sustain the emitter current under load conditions and secondly, the output will now swing down to the zener voltage plus saturation voltage. The high-power (and high cost) zener can be alternatively implemented with a power transistor and low-power zener, as shown in Figure 10 (c).

Transistors Q_3 and Q_4 (MJE200) are relatively fast (f_t (min) = 65 MHz) but have V_{CEO} rating of only 25V maximum; thus V_{CE} should not exceed this value. After allowing for all voltage drops, this then puts a limit on how much reverse bias can be applied. The dropping resistor R_1, or the zener, are therefore designed for 15V rather than 20V used in the other illustrated examples. On a comparative basis, the resulting turn-off times should be slightly longer for the 15V bias condition.

Diodes D_1 and D_2 are Baker clamp diodes for transistor Q_4. Diode D_3 insures that Q_3 is turned off when Q_2 saturates by compensating for the voltage drop of D_2.

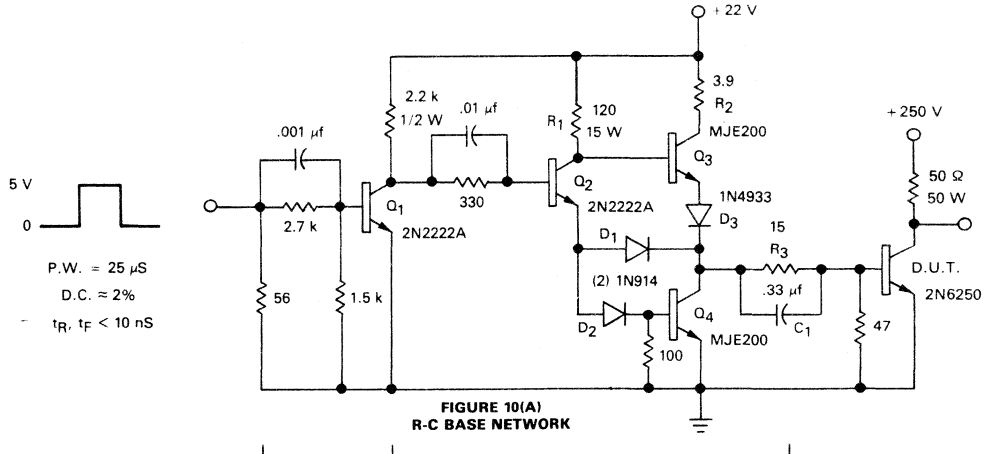


FIGURE 10(A)
R-C BASE NETWORK

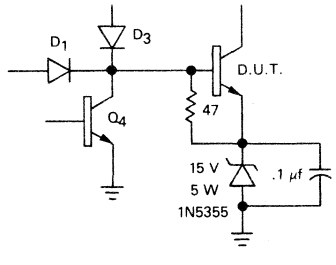


FIGURE 10(B)
ZENER IN EMITTER
HIGH POWER

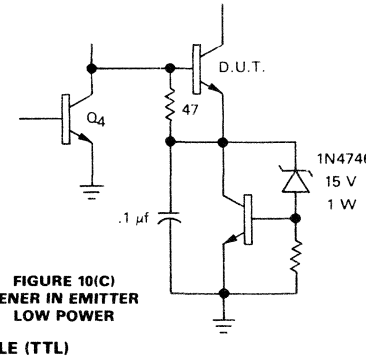


FIGURE 10(C)
ZENER IN EMITTER
LOW POWER

FIGURE 10 — TOTEM-POLE (TTL)
DRIVE E-B AVALANCHE CIRCUIT

TOTEM-POLE DRIVE (HTL)

The circuit of Figure 11 is basically a power scaled up version of the output stage of a High Threshold Logic (HTL) gate and is quite similar to the previously described TTL version. For this example, higher voltage, but lower bandwidth, driver transistors are used, the MJE180 (V_{CEO} (max) = 40V, f_t (min) = 50 MHz). In the absence of a turn-on pulse, transistor Q_1 is conducting, clamping off Q_2 and the D.U.T.. When a negative pulse is applied to the input, Q_1 turns off and Q_2 turns on by means of the base current through R_1. This resistor is designed to supply adequate base current to insure Q_2 saturation and thus must be able to sustain the power dissipated when Q_1 is on (approximately 7.5W for low-duty cycle operation). Transistor Q_2 then supplies the 1.0A I_{B1} to the D.U.T., limited by R_2 and R_3. The voltage drop across R_3 (approximately 22V) produces the reverse bias by means of the switched (when Q_1 turns on) charged capacitor C_1. For values of C_1 of 1.0μf and 0.33μf, peak reverse biases of about −14V and −4V resulted which produced storage times of about 1.8 and 1.9μs respectively. Fall times read 0.18 and 0.50μs respectively with the capacitor recovery times being about 70μs and 15μs respectively. These times are slower than the TTL version and are attributed to the lower base current to the clamp transistor Q_1, being about 11mA for this version relative to about 200mA for the other. This produced about a −3A I_{B2} relative to about −8A. Switching characteristics for this circuit as well as all the other examples are summarized in Table 3.

TRANSFORMER ISOLATED E-B AVALANCHE DRIVE CIRCUIT

A circuit that generates its own isolated reverse bias voltage by using a pulse transformer is illustrated in Figure 12. When a 10V positive pulse is applied to the input, transistor Q_1 is turned on, generating an approximate 35V pulse on the 1:1 transformer primary. This, in turn, induces a 35V secondary pulse which initially creates an I_{B1} to the D.U.T. through the parallel combination of R_1 and the uncharged capacitor C_1 and its limiting resistor R_2. As the capacitor charges up in the R_2, C_1 time constant (4μs) to about 33V, I_{B1} decays to its steady state value of 1.0A. Upon turn-off, I_{B1} ceases and C_1 starts to discharge through R_1, R_3, B-E junction of Q_2 and D_2, turning on Q_2. The remaining charge on C_1 is then switched across the E-B of the D.U.T., a alanching this junction. The result is a peak I_{B2} of abo −6A which produces a t_s and t_f of about 1.1μs ar 0.33μs respectively. Diode D_1 blocks the discharge pa of C_1 and D_2 prevents E-B avalanching of Q_2 while is charging up. A voltage scaled down version of th circuit was also tested resulting in lower capacitor vol age, reverse bias voltage and I_{B2} with somewhat high turn-off times.

SPEED-UP INDUCTOR

Speed-up circuits using capacitors are well know What is not common knowledge, but has been publishe in several sources, is a technique using a shunt induct across the E-B of the D.U.T., as shown in Figure 1 When a constant current pulse is applied to the base the D.U.T., initially, all of the current is base curre (since the inductor requires a finite time to charge u and the transistor is turned on hard. As the pulse tim progresses, the inductor current ramps up and the ba current is proportionally reduced; thus, the transistor not driven as hard into saturation. When the applie current pulse is removed, the energy stored in the i ductor can induce a voltage pulse (e = L di/dt), wi proper design, to avalanche the E-B of the D.U.T.. Th resulting I_{B2} that flows will be the difference betwe the applied current (1.0A) and the base current at th end of the pulse; i.e., $I_{B2} = I_{IN} - I_{B1\ t2}$. The base curre at this time should be large enough to still ensure sat ration of the device. The end result is a reduction of tur off time due to the lower base drive and the avalanchin of the D.U.T.. With the component values shown, f two cases of I_{B2} of 0.5A and 0.8A (pulse widths of abo 15μs and 26μs), storage times of about 3.6μs and 1.8μ respectively resulted. The fall times were respectivel 0.28μs and 0.18μs. As can be expected, the results we better with larger I_{B2}, but it must be recalled that th base current, at the end of the pulse time, is reduce When I_{B2} is 0.8A, I_{B1} is only 0.2A, resulting in a force gain of 25 (5.0/0.2). For the 2N6250, the typical h_{FE} about 20 making this condition extremely marginal.

Although very simple in design, the circuit perfo mance is therefore highly dependent on applied puls width and the resulting $I_{B1\ t2}$ and I_{B2}.

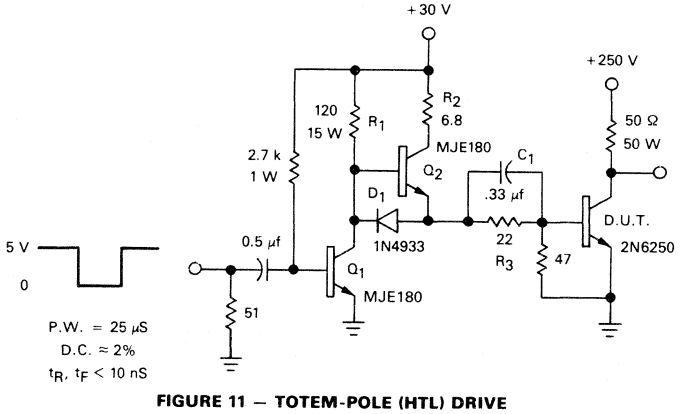
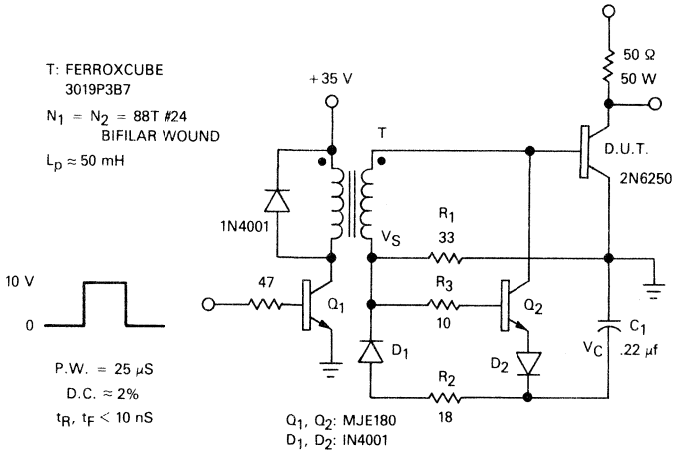
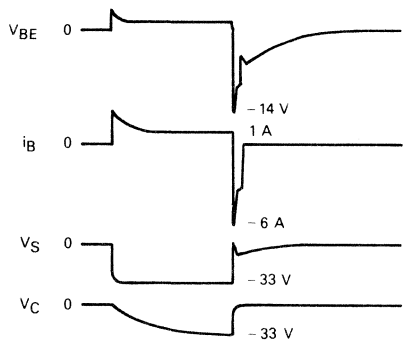


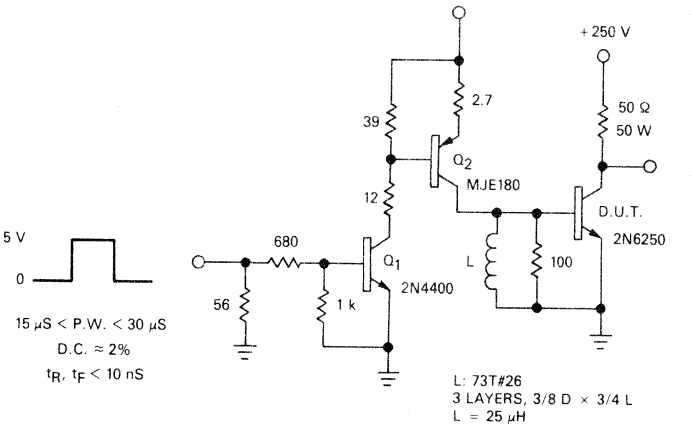
FIGURE 11 – TOTEM-POLE (HTL) DRIVE E-B AVALANCHE CIRCUIT

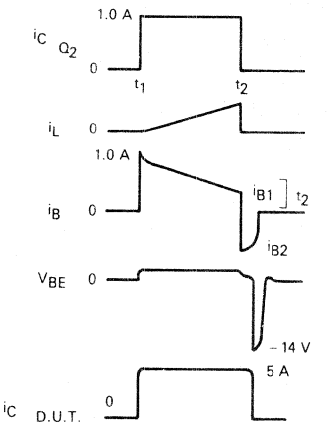




CIRCUIT WAVEFORMS

FIGURE 12 — TRANSFORMER ISOLATED E-B AVALANCHE DRIVE CIRCUIT





CIRCUIT WAVEFORMS

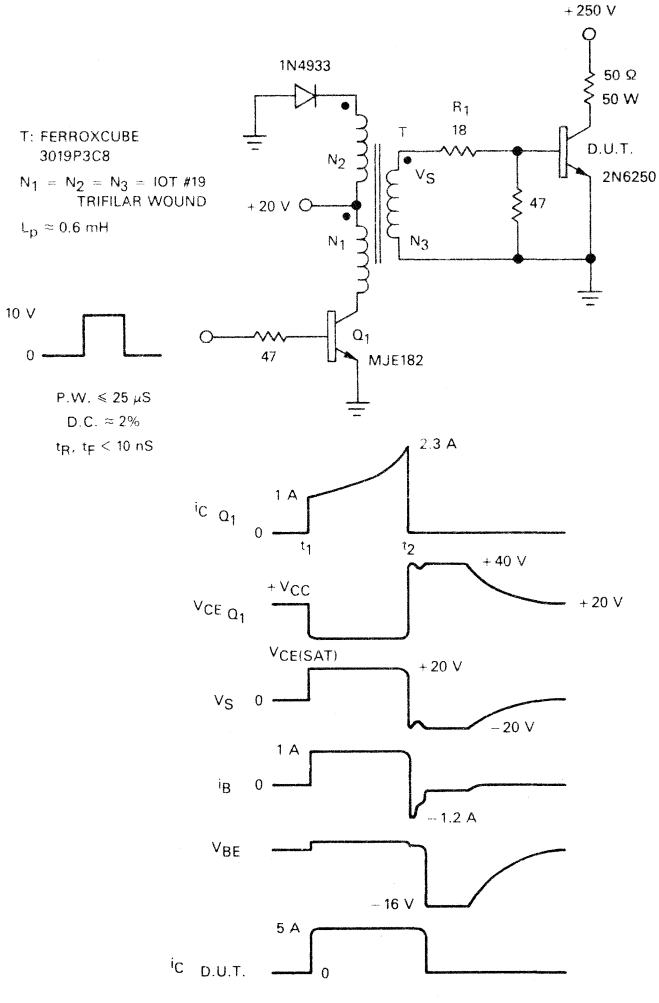
FIGURE 13 — SPEED-UP INDUCTOR E-B AVALANCHE CIRCUIT

SINGLE-ENDED, PUSH-PULL DRIVE

Flyback converter techniques can be used to generate the required avalanche voltage, as shown in Figure 14. This quasi push-pull drive circuit uses a trifilar wound transformer whose primary inductance is selected as a compromise between small pulse-droop and relatively high magnetizing current. It is this magnetizing current that supplies the avalanche I_{B2}.

Upon application of a 25μs wide, positive pulse, transistor Q1 turns on. The initial collector (primary I_p) current flowing will be dictated by the secondary load reflected to the primary, thus I_C is about 1.0A (V_{CC}/R_1). Because of the low primary inductance of about 0.6mH, the magnetizing current will start to ramp-up, storing that energy in the core.

During this time interval, the secondary, or base current I_{B1}, will also be 1.0A. At the end of the input pulse the stored energy will be transferred to the secondary as I_{B2} and any excess above this value, as dictated by the secondary circuit, will flow through N_2 into the power supply. The collector voltage will rise to twice V_{CC} due to the collapsing magnetic field inducing a like voltage in the second half of the primary, center-tapped transformer N_2. This transformed voltage will appear at the secondary causing the required negative going reverse bias. To insure non-saturation of the transformer, the various parameters (L, V_{CC}, I_c, P. W.) must be judiciously chosen.



CIRCUIT WAVEFORMS

FIGURE 14 — SINGLE-ENDED, PUSH-PULL E-B AVALANCHE DRIVE CIRCUIT

COMPARISON OF E-B AVALANCHE CIRCUITS

Table 3 summarizes the results of the turn-off tests on the seven avalanche circuits and their relative costs. With the exception of the two circuit variations with small speed-up capacitors (0.33μf), all other circuits were avalanched as noted by the $-V_{BE(pk)}$ readings. The effect of storage times from the resulting I_{B2} is also illustrated — irrespective of the circuit, t_s tends to decrease with increasing I_{B2}.

Although all of the circuits do not have comparable power gain, pricing is based on normalized gain and is accomplished by adding the cost of an emitter-follower to the input of the two examples with lower power gain. Costing estimates are based on component quantity buys of 250-999 and do not include assembly costs. The cost of the required negative power supply for the two Transistor Clamp examples are not factored in this exercise. Discounting this supply, on a cost/performance basis, the Transistor Clamp, Series Switch results in the best of the illustrated E-B avalanche circuits.

The author wishes to acknowledge Zane Romaniuk for his contribution in preparing this article.

TABLE 3 — COMPARISON OF E-B AVALANCHE DRIVE CIRCUITS

Circuit		Power Supplies	Conditions		$-i_{B2(pk)}$ (A)	$-V_{BE(pk)}$ (V)	t_s (μS)	t_f (μS)	Remarks	Normal. Cost
Transistor Clamp, Series Switch		+5 V, −20 V	R_S = 0		7.4	≈ 14	0.80	0.22	Requires Negative Power Supply	1.0
Transistor Clamp, Shunt Switch		+5 V −20 V	R_S = 0		3.3	≈ 14	1.5	0.13	Requires — P.S.	1.0
Totem-Pole Drive, TTL	R//C in Base	+25 V	R_3 = 18	C_1 = 1 μf	8.0	≈ 14	0.77	0.30	$t_{rr_{C_1}}$ ≈ 100 μS	1.5
				C_1 = .33 μf	7.5	≈ 8	0.88	0.50	$t_{rr_{C_1}}$ ≈ 30 μS	1.4
	Zener in Emitter		D.C. ≤ 2%		8.0	≈ 14	0.84	0.23	15 V Zener 5 W = $1.50	2.0
Totem-Pole Drive, HTL		+30 V	R_3 = 22	C_1 = 1 μf	3.2	≈ 14	1.83	0.18	$t_{rr_{C_1}}$ ≈ 70 μS	1.1
				C_1 = .33 μf	3.1	4.0	1.92	0.50	$t_{rr_{C_1}}$ ≈ 15 μS	1.0
Transformer Isolated E-B Avalanche Drive		+35 V	—		6.0	≈ 14	1.1	0.33	Emitter Follower Added to Cost	1.8
Speed-Up Inductor		+5 V	P.W. = 15 μS		0.5	≈ 14	3.6	0.28	L = 25 μH i_{B2} α P.W., L $\frac{I_{B1}}{t_2}$ = 0.5A	0.8
			P.W. = 26 μS		0.8	≈ 14	1.8	0.18	L = 25 μH i_{B2} α P.W., L $\frac{I_{B1}}{t_2}$ = 0.2A	
Single-Ended, Push-Pull		+20 V	L_p ≈ 0.6 mH		1.2	≈ 14	3.8	0.18	E.F. Added to Cost	1.5

REFERENCES:

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2) Bailey, R.: Reverse Bias Safe Operating Area, AN-785 Motorola Semiconductor Products Inc.
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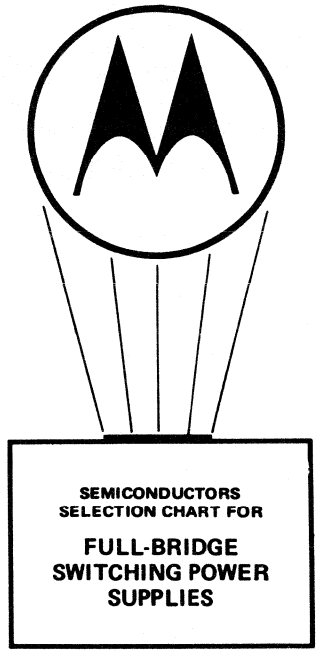
APPLICATION IDEA FROM MOTOROLA

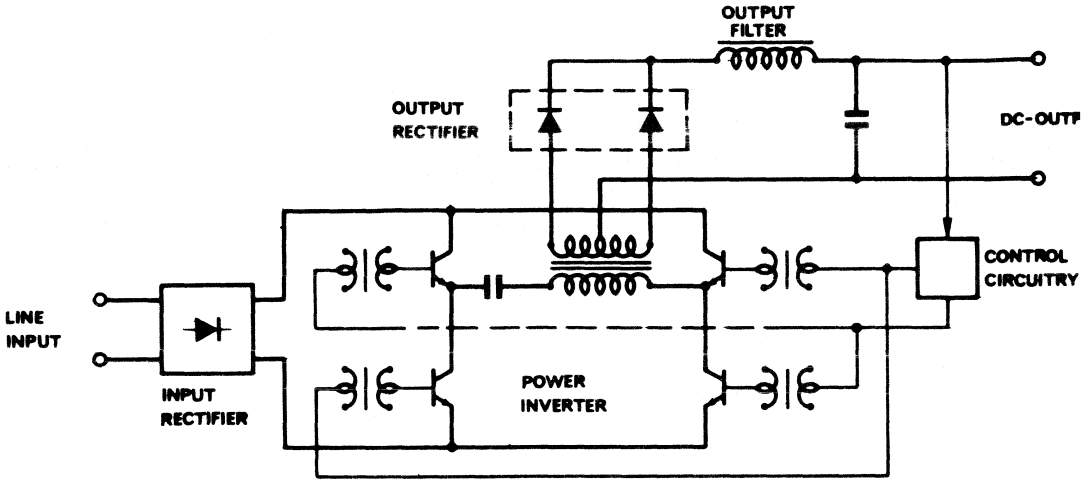


The implementation of switching power supplies by the non-specialist is becoming increasingly easy due to the availability of power devices and control IC's especially developed for this purpose by the semiconductor manufacturer.

This short note is meant to help in the preliminary selection of the devices required for the implementation of a full-bridge configuration supply in the range from 500 to 1000 watts.

Transistor data in the selection table are calculated as follows:

- Input line variation: Vin +10%, −20%
- Converter efficiency: $\eta = 80\%$
- Output regulation by duty cycle (δ) variation: $\delta_{max} = 0.8$
- Max. transistor working current: $I_W = \dfrac{Pout}{\eta \cdot \delta_{max} \cdot Vin_{min} \cdot \sqrt{2}}$
- Nominal transistor collector current: $I_C = 2 \cdot I_W$ to $3 \cdot I_W$
- Max. transistor working voltage: $V_{CEW} = Vin_{max} \cdot \sqrt{2}$
- Nominal transistor collector-emitter voltage: $V_{CEV} \geq 1.2 \cdot V_{CEW}$
- Working frequency: f = 20 to 40 kHz



BASIC FULL-BRIDGE CONFIGURATION

SEMICONDUCTORS SELECTION CHART

Output Power	500 W			750 W			1000 W			
Input Line Voltage V_{in}	120	220 240	380	120	220 240	380	120	220 240	380	V
Transistor Requirements:										
Max. Working Current, I_w	5.7	3.1	1.8	8.6	4.7	2.7	11.5	6.25	3.6	A
Max. Working Voltage, V_{CEW}	190	380	600	190	380	600	190	380	600	V
Recommended Transistor Types:										
Plastic (TO-220)	MJE13008	MJE13006 MJE13008	MJE13005	MJE13008	MJE13006 MJE13008	MJE13005 MJE13007		MJE13008	MJE13007 MJE13009	
Metal (TO-3)	2N6546	2N6544 2N6306	2N6543 2N6545 2N6308	2N6546	2N6306 2N6544 2N6546	2N6545 2N6308	2N6546	2N6546	2N6545 2N6308 2N6547	
Darlingtons (TO-3)	MJ10006 MJ10004	MJ10006/7		MJ10004	MJ10007		MJ10004	MJ10005 MJ10007 MJ10008/9[1]		
Input Rectifiers:										
Max. Working current, I_{DC}	4.6	2.5	1.5	7.0	3.8	2.2	9.25	5	3	A
Recommended types:	MDA970-5 BYW24	BYW26	MDA210	BYW24 BYW64	BYW26	BYW79	BYW24 BYW64	BYW26	BYW79	
Recommended Control Circuits:	MC3420 Inverter Control Circuit MC3423 Over-Voltage Detector Linear Amplifiers: DUAL: MC3458; QUAD: MC3403, MLM324, LM348, MLM2902									
Output Rectifiers:										
Recommended tzpes for output voltages of: 5V	MBR6020*			MBR7520*			MBR7520/30*			
10V	MBR4035/40 MBR6035/45			MBR7535/40			MBR7535/40			
20V	1N3900			1N3911			MR861/71			
50V	1N3891			1N3891/1N3901			1N3901			
100V	MR824			MR824/1N3883/1N3893			1N3893			

[1] To be introduced 3rd Quarter 1977

* More than one device per leg, matched

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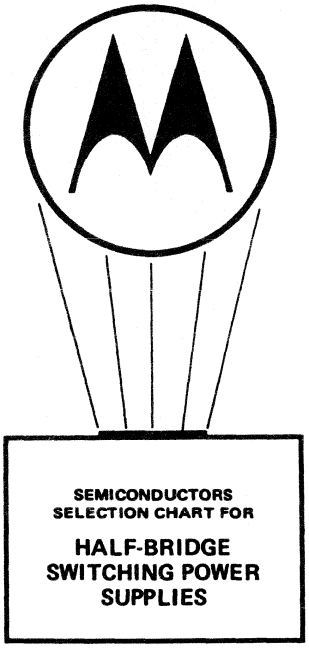
APPLICATION IDEA FROM MOTOROLA

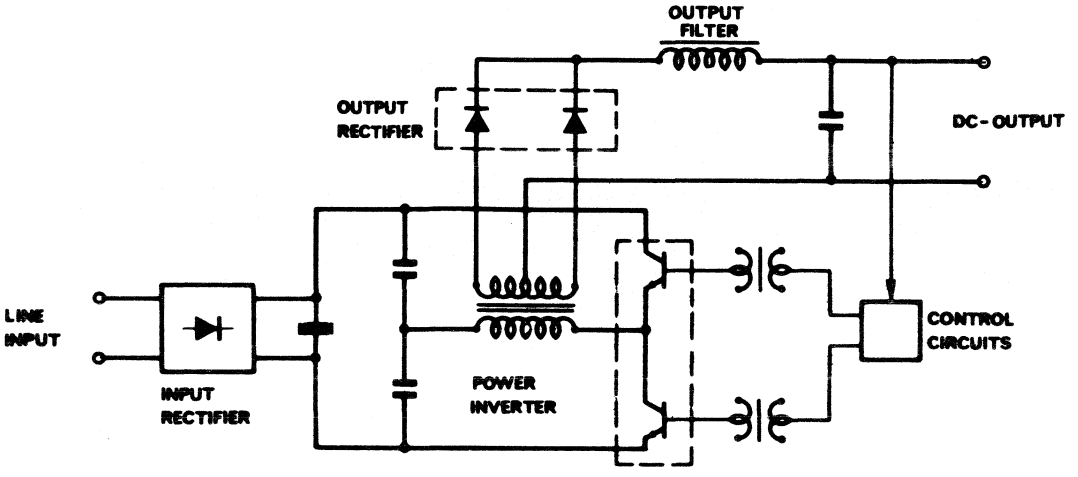


The implementation of switching power supplies by the non-specialist is becoming increasingly easy due to the availability of power devices and control IC's especially developed for this purpose by the semiconductor manufacturer.

This short note is meant to help in the preliminary selection of the devices required for the implementation of a half-bridge configuration supply in the range from 100 to 500 watts.

Transistor data in the selection table are calculated as follows:

- Input line variation: Vin +10%, −20%
- Converter efficiency: $\eta = 80\%$
- Output regulation by duty cycle (δ) variation: $\delta_{max} = 0.8$
- Max. transistor working current: $I_W = \dfrac{2\ Pout}{\eta \cdot \delta_{max} \cdot Vin_{min} \cdot \sqrt{2}}$
- Nominal transistor collector current: $I_C = 2 \cdot I_W$ to $3 \cdot I_W$
- Max. transistor working voltage: $V_{CEW} = Vin_{max} \cdot \sqrt{2}$
- Nominal transistor collector-emitter voltage: $V_{CEV} \geq 1.2 \cdot V_{CEW}$
- Working frequency: f = 20 to 40 kHz



BASIC HALF-BRIDGE CONFIGURATION

SEMICONDUCTORS SELECTION CHART

Output Power	100 W			250 W			500 W			
Input Line Voltage: V_{in}	120	220 240	380	120	220 240	380	120	220 240	380	V
Transistor Requirements:										
Max. Working Current, I_W	2.3	1.25	0.75	5.7	3.1	1.8	11.5	6.25	3.6	A
Max. Working Voltage, V_{CEW}	190	380	680	190	380	680	190	380	680	V
Recommended Types:										
Plastic (TO-220, TO-126)	MJE13004 MJE13006	MJE13004	MJE13003 MJE13005	MJE13008	MJE13006 MJE13008	MJE13005		MJE13008	MJE13007 MJE13009	
Metal (TO-3, TO-66)	2N6233/34 2N6542	2N6542 2N4240	2N6543	2N6546	2N6544 2N6306	2N6543 2N6545 2N6308	2N6546	2N6546	2N6545 2N6547 2N6308	
Darlingtons (TO-3)	MJ10006	MJ10006/7		MJ10004 MJ10006	MJ10006/7		MJ10004	MJ10005 MJ10007 MJ10008/9[1]		
Input rectifiers:										
Max Working Current, I_{DC}	0.9	0.5	0.3	2.3	1.25	0.75	4.6	2.5	1.5	
Recommended Types:	MDA204 MDA970-5	MDA206	MDA210	MDA970-5	MDA806	MDA210	MDA970-5 MDA804 MDA1204 MDA980-5	MDA806	BYW79	
Recommended Control Circuits:	MC3420 Inverter Control Circuit MC3423 Over-Voltage Detector Linear Amplifiers: DUAL: MC3458; QUAD: MC3403, MLM324, LM348, MLM2902									
Output Rectifiers:										
Recommended types for output voltages of: 5V	MBR1530			MBR4030/MBR6030			MBR7530			
10V	MBR1535/40			MBR2535/40 MBR3535/45			MBR8035/40			
20V	MR821/1N3880/1N3890			1N3890			1N3900			
50V	MR832/MR852/MR912			MR822/1N3881			1N3891			
100V	MR836/MR916/1N4936			MR834/MR804/MR854/MR914			MR824			

[1] To be introduced 3rd quarter 197-

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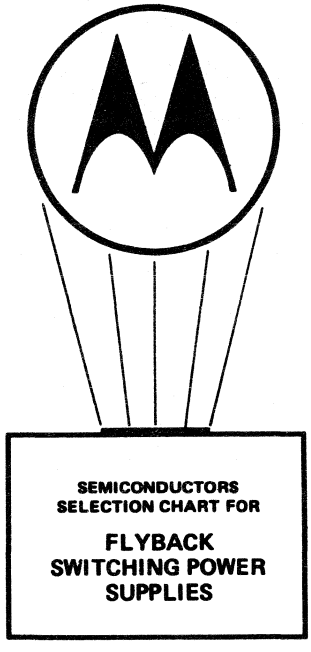
APPLICATION IDEA FROM MOTOROLA

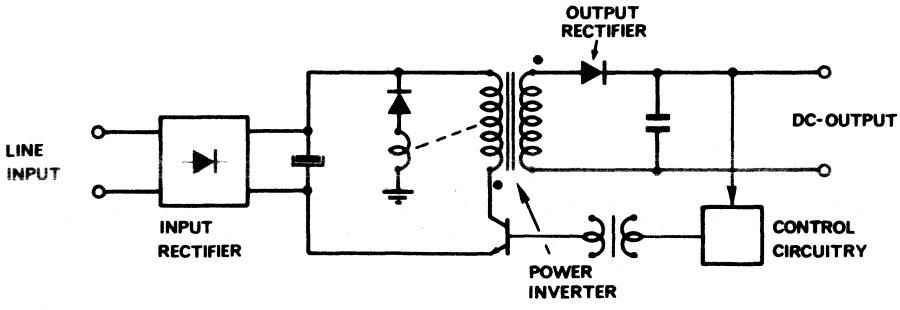


The implementation of switching power supplies by the non-specialist is becoming increasingly easy due to the availability of power devices and control IC's especially developed for this purpose by the semiconductor manufacturer.

This short note is meant to help in the preliminary selection of the devices required for the implementation of a flyback configuration supply in the range from 100 to 250 watts.

Transistor data in the selection table are calculated as follows:

- Input line variation: Vin +10%, −20%
- Converter efficiency: $\eta = 80\%$
- Output regulation by duty cycle (δ) variation: $\delta_{max} = 0.5$
- Max. transistor working current: $I_W = \dfrac{(2.5 \text{ to } 4) \cdot Pout}{\eta \cdot Vin_{min} \cdot \sqrt{2}}$
- Nominal transistor collector current: $I_C = 2 \cdot I_W$ to $3 \cdot I_W$
- Max. transistor working voltage: $V_{CEW} \approx 2 \cdot Vin_{max} \cdot \sqrt{2}$
- Nominal transistor collector-emitter voltage: $V_{CEV} \geq 1.2 \cdot V_{CEW}$
- Working frequency: f = 20 to 40 kHz



BASIC FLYBACK CONFIGURATION

SEMICONDUCTORS SELECTION CHART

Output Power	100 W		175 W		250 W		
Input Line Voltage: V_{in}	120	220 240	120	220 240	120	220 240	V V
Transistor Requirements:							
Max. Working Current, I_W	2.3–3.7	1.25–2	4–6.5	2.2–3.5	5.8–9.3	3.1–5	A
Max. Working Voltage, V_{CEW}	380	750	380	750	380	750	V
Recommended Types							
Plastic (TO-220)	MJE13004 MJE13006		MJE13006 MJE13008		MJE13008		
Metal (TO-3)	2N6542 2N6544	2N6543 2N6545	2N6544 2N6546	2N6543 2N6545	2N6546	2N6545 2N6547	
Darlingtons (TO-3)	MJ10007		MJ10007 MJ10005		MJ10005 MJ10008/9[1]		
Input Rectifiers:							
Max. Working Current, I_{DC}	0.9	0.5	1.6	0.9	2.3	1.25	A
Recommended Types:	MDA204 MDA970-5	MDA206	MDA970-5		MDA970-5 BYW24		
Recommended Control Circuits	MC3380 Astable multivibrator MC3423 Over-Voltage Detector Linear Amplifiers: DUAL: MC3458; QUAD: MC3403, MLM324, LM348, MLM2902						
Output Rectifiers:							
Recommended types for output voltages of: 5V	MR860/MR870		1N3909/MR860/MR870*		MR860/MR870*		
10V	1N3900/1N3910		1N3910/MR861/MR871		MR861/MR871		
20V	1N3891/1N3901		1N3901/1N3911		1N3901/1N3911		
50V	MR836/MR856/MR916		MR836/MR1366		MR826/MR1366/MR1376		

[1] To be introduced 3rd Quarter 1977

* More than one device per leg, matched